

**PHILIPS**

Data handbook



Electronic  
components  
and materials

# Integrated circuits

Part 1

March 1984

**Bipolar ICs for radio and audio equipment**





# INTEGRATED CIRCUITS

PART 1 - MARCH 1984

## BIPOLAR ICs FOR RADIO AND AUDIO EQUIPMENT

FUNCTIONAL AND NUMERICAL INDEX  
MAINTENANCE TYPE LIST

GENERAL

PACKAGE OUTLINES

DEVICE DATA





## DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

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## ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

- T1 Tubes for r.f. heating**
- T2a Transmitting tubes for communications, glass types**
- T2b Transmitting tubes for communications, ceramic types**
- T3 Klystrons, travelling-wave tubes, microwave diodes**
- ET3 Special Quality tubes, miscellaneous devices (will not be reprinted)**
- T4 Magnetrons**
- T5 Cathode-ray tubes**  
Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6 Geiger-Müller tubes**
- T7 Gas-filled tubes**  
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories
- T8 Picture tubes and components**  
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display
- T9 Photo and electron multipliers**  
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates
- T10 Camera tubes and accessories, image intensifiers**
- T11 Microwave semiconductors and components**

## SEMICONDUCTORS (RED SERIES)

The red series of data handbooks is comprised of the following parts:

- S1 Diodes**  
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
- S2 Power diodes, thyristors, triacs**  
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
- S3 Small-signal transistors**
- S4a Low-frequency power transistors and hybrid modules**
- S4b High-voltage and switching power transistors**
- S5 Field-effect transistors**
- S6 R.F. power transistors and modules**
- S7 Microminiature semiconductors for hybrid circuits**
- S8 Devices for optoelectronics**  
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
- S9 Power MOS transistors**
- S10 Wideband transistors and wideband hybrid IC modules**

## INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks is comprised of the following parts:

- IC1** Bipolar ICs for radio and audio equipment
- IC2** Bipolar ICs for video equipment
- IC3** ICs for digital systems in radio, audio and video equipment
- IC4** Digital integrated circuits  
CMOS HE4000B family
- IC5** Digital integrated circuits – ECL  
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
- IC6** Professional analogue integrated circuits
- IC7** Signetics bipolar memories
- IC8** Signetics analogue circuits
- IC9** Signetics TTL logic
- IC10** Signetics Integrated Fuse Logic (IFL)
- IC11** Microprocessors, microcomputers and peripheral circuitry

## COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks is comprised of the following parts:

- C1 Assemblies for industrial use**  
PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs
- C2 Television tuners, video modulators, surface acoustic wave filters**
- C3 Loudspeakers**
- C4 Ferroxcube potcores, square cores and cross cores**
- C5 Ferroxcube for power, audio/video and accelerators**
- C6 Synchronous motors and gearboxes**
- C7 Variable capacitors**
- C8 Variable mains transformers**
- C9 Piezoelectric quartz devices**  
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements
- C10 Connectors**
- C11 Non-linear resistors**  
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
- C12 Variable resistors and test switches**
- C13 Fixed resistors**
- C14 Electrolytic and solid capacitors**
- C15 Film capacitors, ceramic capacitors**
- C16 Permanent magnet materials**
- C17 Stepping motors and electronics**
- C18 D.C. motors**
- C19 Piezoelectric ceramics**





FUNCTIONAL AND NUMERICAL INDEX  
MAINTENANCE TYPE LIST





## SELECTION GUIDE BY FUNCTION

type number	description	package code	pins
<b>AM channels</b>			
TDA1072	AM receiver circuit	SOT-38	16
TEA5550	AM car radio receiver circuit	SOT-38	16
TEA5570	AM/FM radio receiver circuit	SOT-38	16
<b>FM channels</b>			
TDA1571T	balanced mixer/modulator/demodulator	SOT-109A (SO-16)	16
TDA1576	FM/IF amplifier	SOT-102HE	18
TDA7000	FM radio circuit	SOT-102HE	18
TDA7010T	FM radio circuit	SOT-109A (SO-16)	16
TEA5560	FM/IF system	SOT-142	9
TEA5570	AM/FM radio receiver circuit	SOT-38	16
TEA6000	FM/IF system and microcomputer-based tuning interface	SOT-102HE	18
<b>AM/FM combined channels</b>			
TDA1571T	balanced mixer/modulator/demodulator	SOT-109A (SO-16)	16
TEA5570	AM/FM radio receiver circuit	SOT-38	16
<b>Stereo decoders</b>			
TDA1005A	frequency multiplex PLL stereo decoder	SOT-38	16
TDA1005AT	frequency multiplex PLL stereo decoder	SOT-109A (SO-16)	16
TDA1578A	time multiplex PLL stereo decoder	SOT-102HE	18
TEA5580	PLL stereo decoder	SOT-38	16
<b>Interference suppressors</b>			
TDA1001B	interference and noise suppression circuit for FM receivers	SOT-38	16
TDA1001BT	interference and noise suppression circuit for FM receivers	SOT-109A (SO-16)	16
<b>Tuning circuits</b>			
SAA1057	radio tuning PLL frequency synthesizer	SOT-102HE	18
SAA1300	tuner switching circuit	SOT-142B	9
TDA1574	FM tuner	SOT-102HE	18
<b>D.C. controlled audio circuits</b>			
TCA730A	d.c. volume and balance stereo control circuit	SOT-38	16
TCA740A	d.c. treble and bass stereo control circuit	SOT-38	16
TDA1029	signal-sources switch (4 x two channels)	SOT-38	16
TDA1074A	dual tandem electronic potentiometer circuit	SOT-102CS	18
TDA1524A	stereo-tone volume control circuit	SOT-102CS	18

# INDEX

## SELECTION GUIDE BY FUNCTION (continued)

type number	description	package code	pins
<b>Audio power amplifiers</b>			
TDA1010A	6 W audio power amplifier in car and 10 W audio power amplifier in mains-fed applications	SOT-110B	9
TDA1011	2 to 6 W audio power amplifier	SOT-110B	9
TDA1011A	2 to 6 W audio power amplifier with inverted input/output	SOT-110B	9
TDA1013A	4 W audio power amplifier with d.c. volume control	SOT-110B	9
TDA1015	1 to 4 W audio power amplifier	SOT-110B	9
TDA1020	12 W car radio power amplifier	SOT-110B	9
TDA1510	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1512	12 to 20 W hi-fi audio power amplifier	SOT-131B	9
TDA1512Q	12 to 20 W hi-fi audio power amplifier	SOT-157B	9
TDA1515	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1520	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520A	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520AQ	20 W hi-fi audio power amplifier	SOT-157A	9
TDA1520Q	20 W hi-fi audio power amplifier	SOT-157A	9
TDA2611A	5 W audio power amplifier	SOT-110B	9
<b>Recorder (cassette) amplifiers/control circuits</b>			
TDA1002A	recording and playback amplifier	SOT-38	16
TDA1012	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1016	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1508	auto-reverse car radio cassette deck steering circuit	SOT-102CS	18
TDA1522	stereo cassette head preamplifier and equalizer	SOT-142	9
<b>Motor speed control circuits</b>			
TDA1059B	motor speed regulator with thermal shut-down	SOT-32	3
TDA1059C	motor speed regulator	SOT-32	3
TDA1506	motor regulator and function controller for car cassette systems	SOT-38	16
TDA1533	PLL motor speed control circuit for hi-fi applications	SOT-102CS	18
TDA1559A	motor speed regulator	SOT-32	3
<b>Display drivers</b>			
SAA1060	LED display/interface circuit	SOT-101A	24
SAA1062A	LCD display/interface circuit	SOT-117	28
SAA1062AT	LCD display/interface circuit	SOT-136A (SO-28)	28
SAA1063	fluorescent display/interface circuit	SOT-101A	24

type number	description	package code	pins
<b>Miscellaneous</b>			
OM200/S2	integrated amplifier for use in hearing aids	SOT-20	4
TAA263	low-level amplifier	SOT-18/17	4
TAA320	integrated MOST amplifier	SOT-18/13	3
TAA320A	integrated MOST level sensor	SOT-18/13	3
TDA1540D	14-bit DAC with 85 dB S/N ratio	SOT-135A	28
TDA1540P	14-bit DAC with 85 dB S/N ratio	SOT-117BE	28
TDA1589	traffic control messages and warning tone circuit	SOT-102HE	18



## NUMERICAL INDEX

type number	description	package code	pins
OM200/S2	integrated amplifier for use in hearing aids	SOT-20	4
SAA1057	radio tuning PLL frequency synthesizer	SOT-102HE	18
SAA1060	LED display/interface circuit	SOT-101A	24
SAA1062A	LCD display/interface circuit	SOT-117	28
SAA1062AT	LCD display/interface circuit	SOT-136A (SO-28)	28
SAA1063	fluorescent display/interface circuit	SOT-101A	24
SAA1300	tuner switching circuit	SOT-142B	9
TAA263	low-level amplifier	SOT-18/17	4
TAA320	integrated MOST amplifier	SOT-18/13	3
TAA320A	integrated MOST level sensor	SOT-18/13	3
TCA730A	d.c. volume and balance stereo control circuit	SOT-38	16
TCA740A	d.c. treble and bass stereo control circuit	SOT-38	16
TDA1001B	interference and noise suppression circuit for FM receivers	SOT-38	16
TDA1001BT	interference and noise suppression circuit for FM receivers	SOT-109A (SO-16)	16
TDA1002A	recording and playback amplifier	SOT-38	16
TDA1005A	frequency multiplex PLL stereo decoder	SOT-38	16
TDA1005AT	frequency multiplex PLL stereo decoder	SOT-109A (SO-16)	16
TDA1010A	6 W audio power amplifier in car and 10 W audio power amplifier in mains-fed applications	SOT-110B	9
TDA1011	2 to 6 W audio power amplifier	SOT-110B	9
TDA1011A	2 to 6 W audio power amplifier with inverted input/output	SOT-110B	9
TDA1012	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1013A	4 W audio power amplifier with d.c. volume control	SOT-110B	9
TDA1015	1 to 4 W audio power amplifier	SOT-110B	9
TDA1016	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1020	12 W car radio power amplifier	SOT-110B	9
TDA1029	signal-sources switch (4 x two channels)	SOT-38	16
TDA1059B	motor speed regulator with thermal shut-down	SOT-32	3
TDA1059C	motor speed regulator	SOT-32	3
TDA1072	AM receiver circuit	SOT-38	16
TDA1074A	dual tandem electronic potentiometer circuit	SOT-102CS	18

type number	description	package code	pins
TDA1506	motor regulator and function controller for car cassette systems	SOT-38	16
TDA1508	auto-reverse car radio cassette deck steering circuit	SOT-102CS	18
TDA1510	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1512	12 to 20 W hi-fi audio power amplifier	SOT-131B	9
TDA1512Q	12 to 20 W hi-fi audio power amplifier	SOT-157B	9
TDA1515	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1520	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520A	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520AQ	20 W hi-fi audio power amplifier	SOT-157A	9
TDA1520Q	20 W hi-fi audio power amplifier	SOT-157A	9
TDA1522	stereo cassette head preamplifier and equalizer	SOT-142	9
TDA1524A	stereo-tone volume control circuit	SOT-102CS	18
TDA1533	PLL motor speed control circuit for hi-fi applications	SOT-102CS	18
TDA1540D	14-bit DAC with 85 dB S/N ratio	SOT-135A	28
TDA1540P	14-bit DAC with 85 dB S/N ratio	SOT-117BE	28
TDA1559A	motor speed regulator	SOT-32	3
TDA1571T	balanced mixer/modulator/demodulator	SOT-109A (SO-16)	16
TDA1574	FM tuner	SOT-102HE	18
TDA1576	FM/IF amplifier	SOT-102HE	18
TDA1578A	time multiplex PLL stereo decoder	SOT-102HE	18
TDA1589	traffic control messages and warning tone circuit	SOT-102HE	18
TDA2611A	5 W audio power amplifier	SOT-110B	9
TDA7000	FM radio receiver circuit	SOT-102HE	18
TDA701QT	FM radio receiver circuit	SOT-109A (SO-16)	16
TEA5550	AM car radio receiver circuit	SOT-38	16
TEA5560	FM/IF system	SOT-142	9
TEA5570	AM/FM radio receiver circuit	SOT-38	16
TEA5580	PLL stereo decoder	SOT-38	16
TEA6000	FM/IF system and microcomputer-based tuning interface	SOT-102HE	18

## MAINTENANCE TYPE LIST

The types listed below are included in this handbook by two pages information. Detailed information will be supplied on request.

SAA1059  
TBA570A  
TBA570AQ  
TDA1006A  
TDA1008  
TDA1028  
TDA1524  
TDA1527  
TDA1580  
TDA1584  
TDA1594  
TDA5700  
TDA5700Q

successor type: TDA1524A





GENERAL

**Type designation**  
**Rating systems**





## PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

*THREE LETTERS FOLLOWED BY A SERIAL NUMBER*

### FIRST AND SECOND LETTER

#### 1. DIGITAL FAMILY CIRCUITS

The FIRST TWO LETTERS identify the FAMILY (see note 1).

#### 2. SOLITARY CIRCUITS

The FIRST LETTER divides the solitary circuits into:

- S : Solitary digital circuits
- T : Analogue circuits
- U : Mixed analogue/digital circuits

The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

#### 3. MICROPROCESSORS

The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

- MA : { Microcomputer
- } Central processing unit
- MB : Slice processor (see note 2)
- MD : Correlated memories
- ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

#### 4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The FIRST TWO LETTERS identify the following:

- NH : Hybrid circuits
- NL : Logic circuits
- NM : Memories
- NS : Analogue signal processing, using switched capacitors
- NT : Analogue signal processing, using CTDs
- NX : Imaging devices
- NY : Other correlated circuits

### Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.



# TYPE DESIGNATION

## THIRD LETTER

It indicates the operating ambient temperature range.  
The letters A to G give information about the temperature:

- A : temperature range not specified
- B : 0 to + 70 °C
- C : -55 to + 125 °C
- D : -25 to + 70 °C
- E : -25 to + 85 °C
- F : -40 to + 85 °C
- G : -55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

## SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

### *A VERSION LETTER*

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

- C : for cylindrical
- D : for ceramic DIL
- F : for flat pack
- L : for chip on tape
- P : for plastic DIL
- Q : for QIL
- T : for miniature plastic (mini-pack)
- U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

*FIRST LETTER:* General shape

- C : Cylindrical
- D : Dual-in-line (DIL)
- E : Power DIL (with external heatsink)
- F : Flat (leads on 2 sides)
- G : Flat (leads on 4 sides)
- K : Diamond (TO-3 family)
- M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
- Q : Quadruple-in-line (QIL)
- R : Power QIL (with external heatsink)
- S : Single-in-line
- T : Triple-in-line

*SECOND LETTER:* Material

- C : Metal-ceramic
- G : Glass-ceramic (cerdip)
- M : Metal
- P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

## RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

### DEFINITIONS OF TERMS USED

*Electronic device.* An electronic tube or valve, transistor or other semiconductor device.

#### Note

This definition excludes inductors, capacitors, resistors and similar components.

*Characteristic.* A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

*Bogey electronic device.* An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

*Rating.* A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

#### Note

Limiting conditions may be either maxima or minima.

*Rating system.* The set of principles upon which ratings are established and which determine their interpretation.

#### Note

The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

### ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

## DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

## DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.



PACKAGE OUTLINES



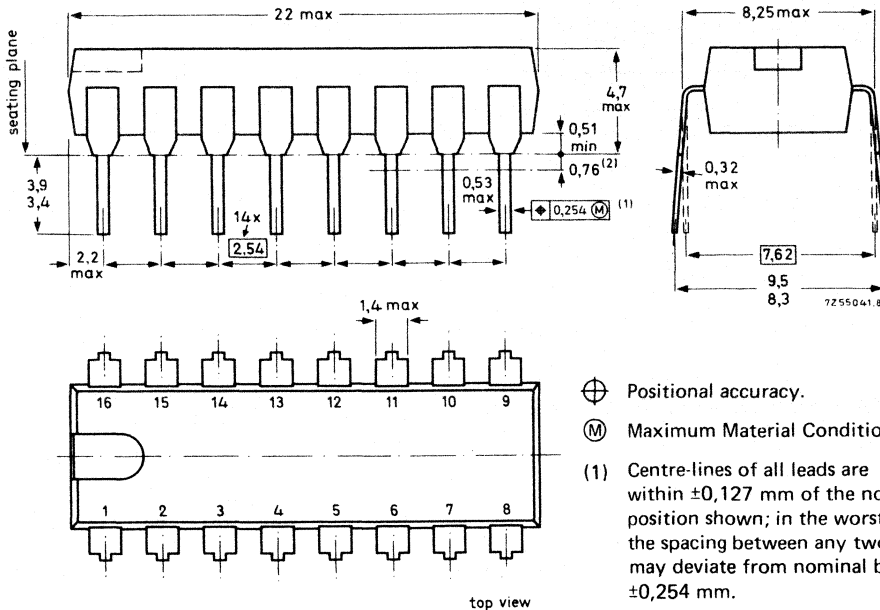
# PACKAGE OUTLINES

In this chapter the package outlines are given for the following types, except for those marked with an asterisk which are included in the device data sheet.

package code	standard description	type numbers
SOT-18/13 (TO-18)* SOT-18/17 (TO-72)* SOT-20* SOT-32*		TAA320; A TAA263 OM200/S2 TDA1059B; C TDA1559
SOT-38	16-lead dual in-line; plastic	TCA730A TCA740A TDA1001B TDA1002A TDA1005A TEA5550 TEA5570 TEA5580
SOT-38WE-2	16-lead dual in-line; plastic with internal heat spreader	TDA1012 TDA1016
SOT-101A	24-lead dual in-line; plastic	SAA1060 SAA1063
SOT-102CS	18-lead dual in-line; plastic	TDA1074A TDA1508 TDA1524A TDA1533
SOT-102HE	18-lead dual in-line; plastic	TDA1574 TDA1576 TDA1578A TDA1589 TDA7000 TEA6000
SO-16; SOT-109A	16-lead mini-pack; plastic	TDA1001BT TDA1005AT TDA1571T TDA7010T
SOT-110B	9-lead single in-line; plastic	TDA1010A TDA1011; A TDA1013A TDA1015 TDA1020 TDA2611A SAA1062A TDA1540P
SOT-117	28-lead dual in-line; plastic	TDA1512 TDA1520 TDA1540D SAA1062AT TDA1510
SOT-131A; B	9-lead single in-line; plastic power	TDA1512 TDA1520 TDA1540D SAA1062AT TDA1510
SOT-135A SO-28; SOT-136A SOT-141B	28-lead dual in-line; ceramic (cerdip) 28-lead mini-pack; plastic 13-lead sil-bent-to-dil; plastic power	TDA1515 SAA1300 TDA1522 TEA5560
SOT-142	9-lead single in-line; plastic	TDA1512Q TDA1520AQ TDA1520Q
SOT-157A; B	9-lead sil-bent-to-dil	



16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).

If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

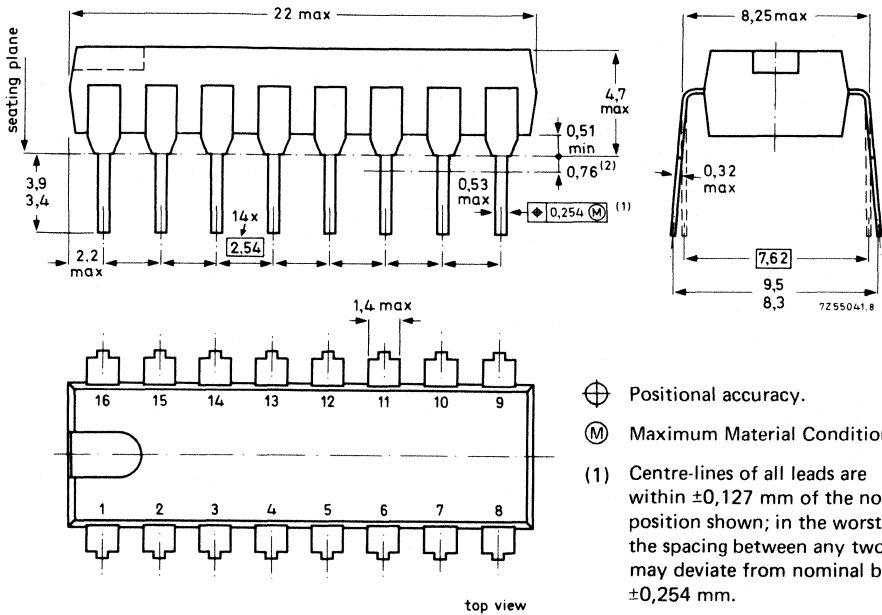
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.



16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER  
(SOT-38WE-2)



- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.
- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

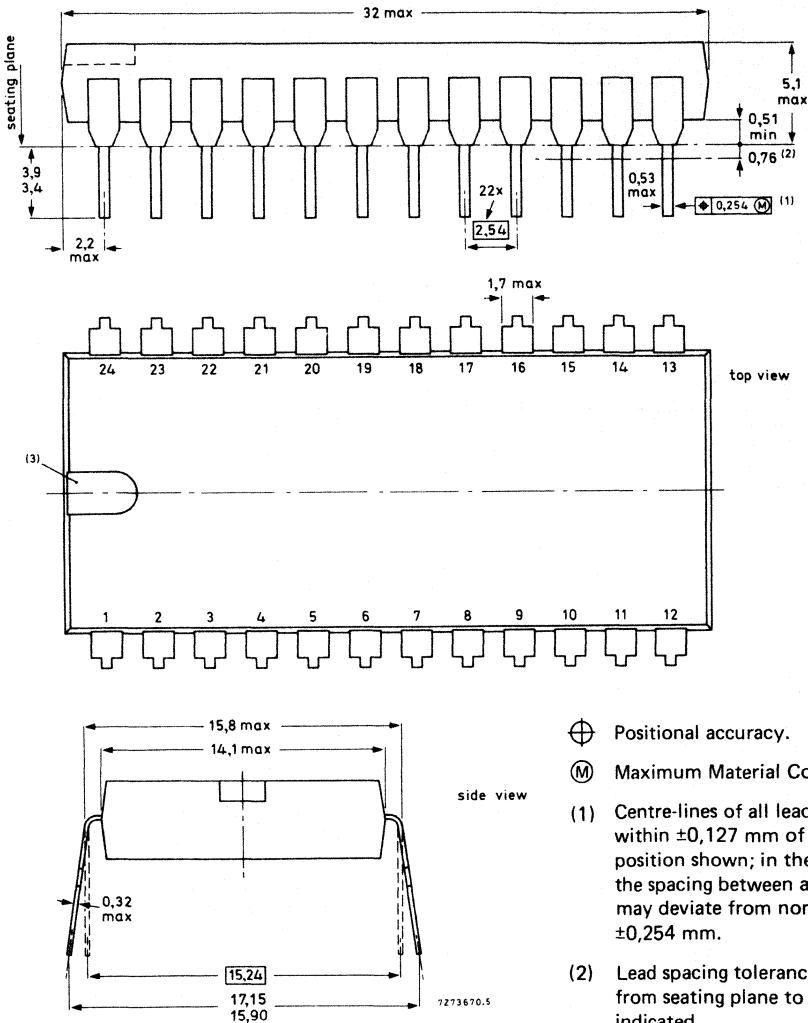
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)



⊕ Positional accuracy.

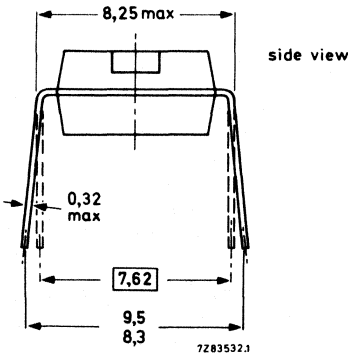
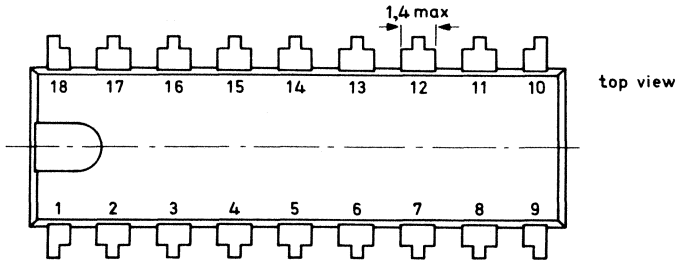
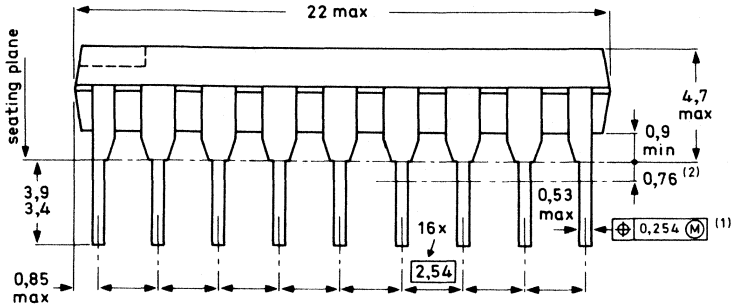
Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING see SOT-38

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS)



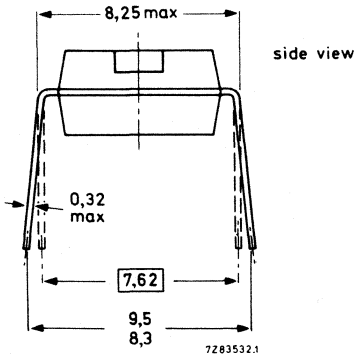
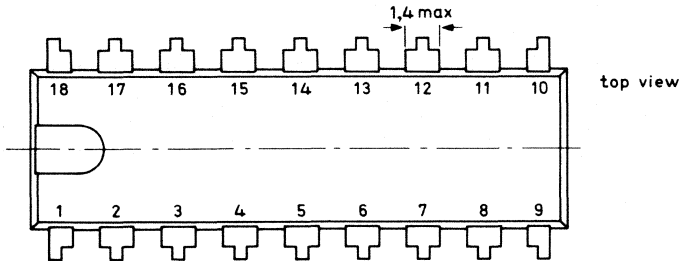
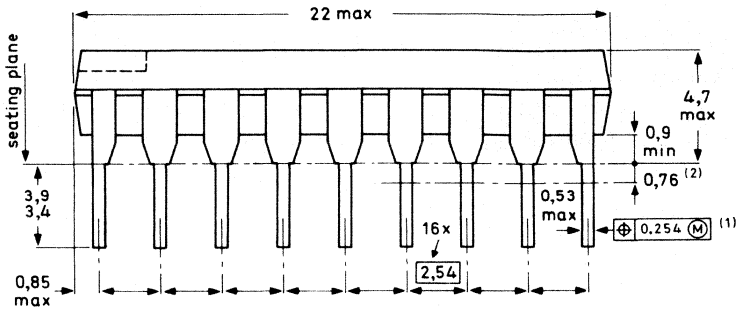
- $\oplus$  Positional accuracy.
- $\textcircled{M}$  Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING see SOT-38

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102HE)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

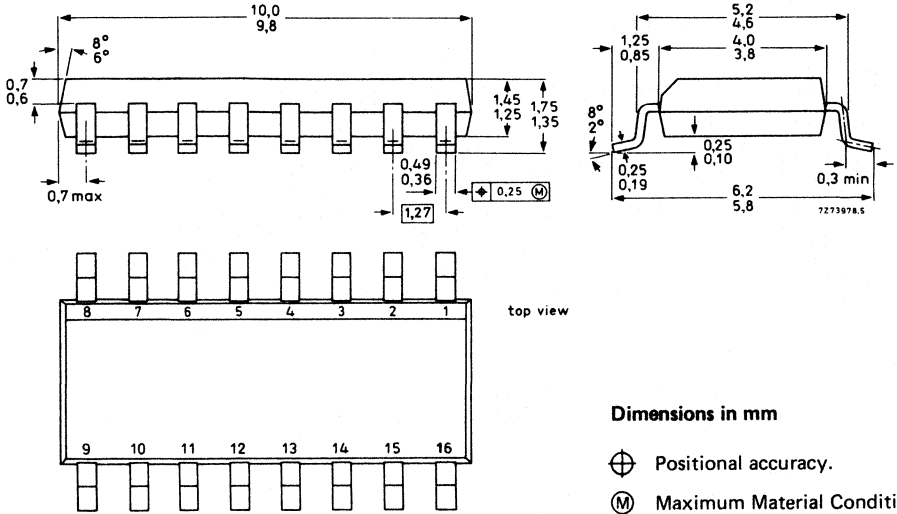
(1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING see SOT-38

16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)



SOLDERING

The reflow solder technique

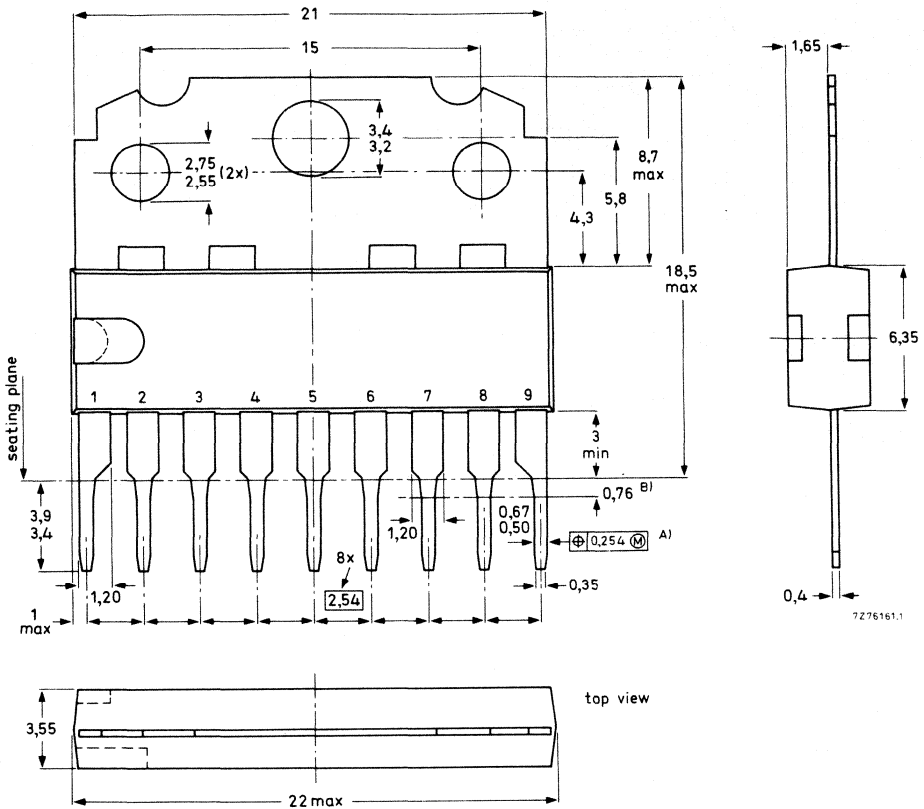
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid. After soldering, the substrate must be cleaned of any remaining flux.

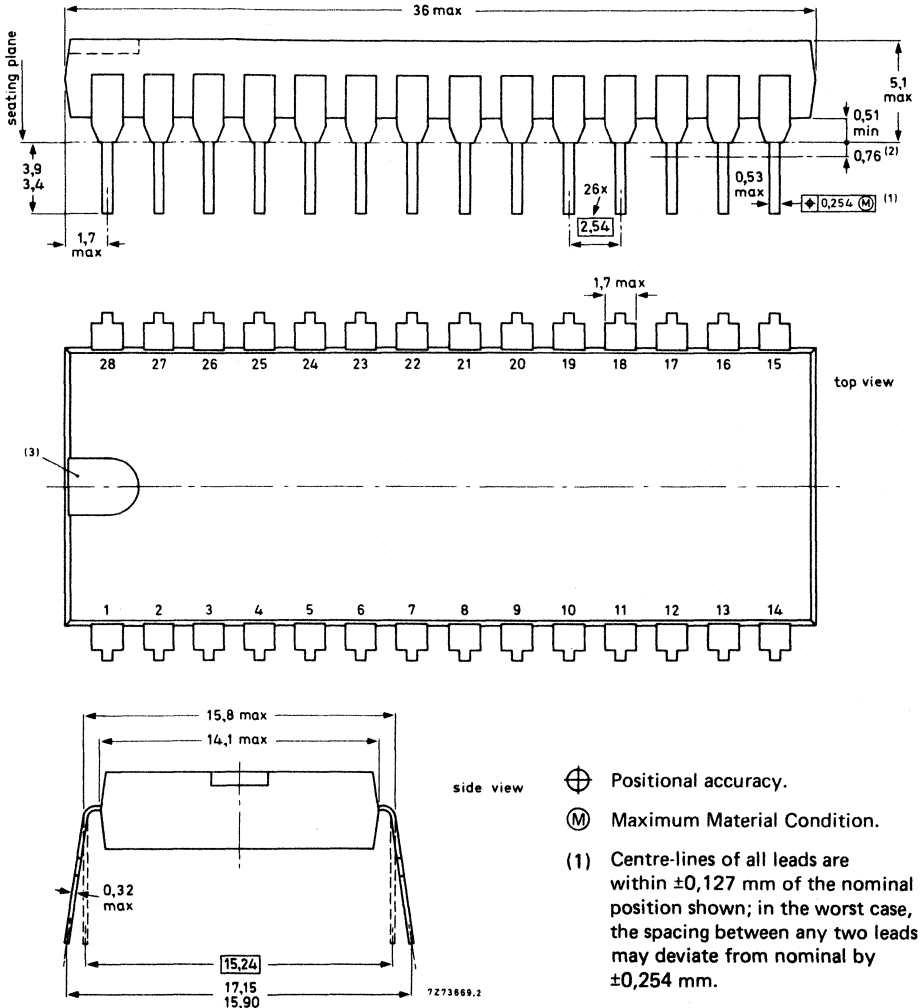
9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)



Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.
- A Centre-lines of all leads are within  $\pm 0.127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0.254$  mm.
- B Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



Dimensions in mm

SOLDERING see SOT-38

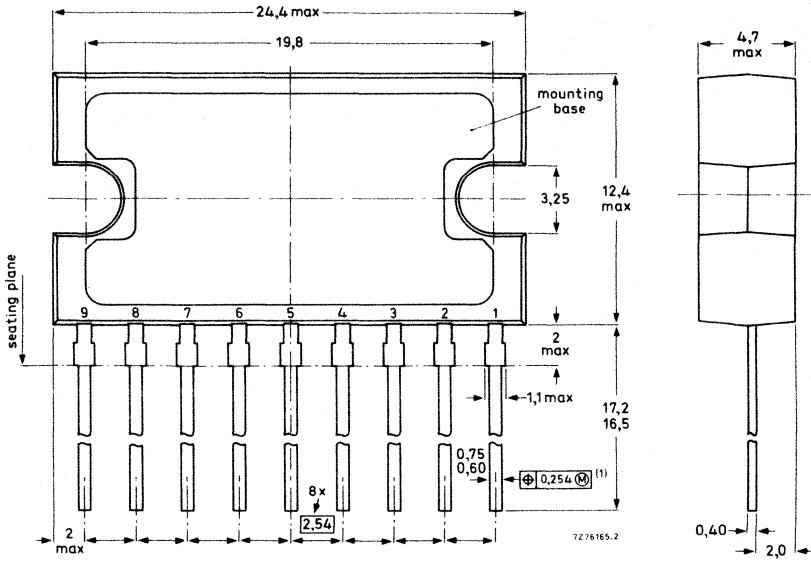
⊕ Positional accuracy.

(M) Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.



9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131A, B)



Dimensions in mm

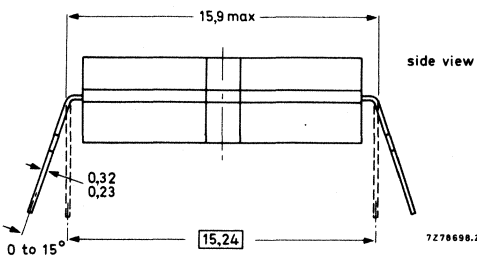
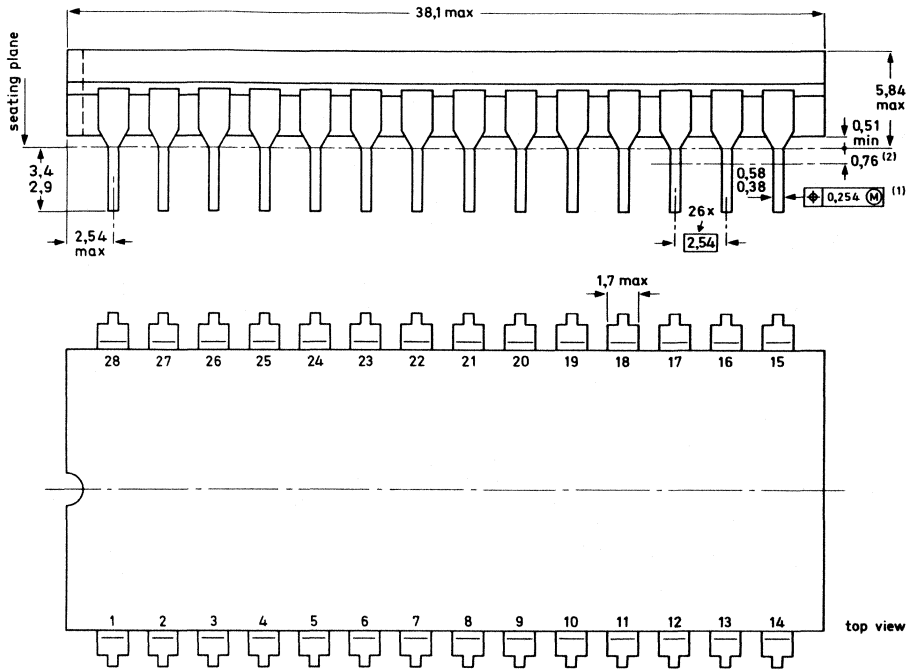
$\oplus$  Positional accuracy.

$\textcircled{M}$  Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.



28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-135A)

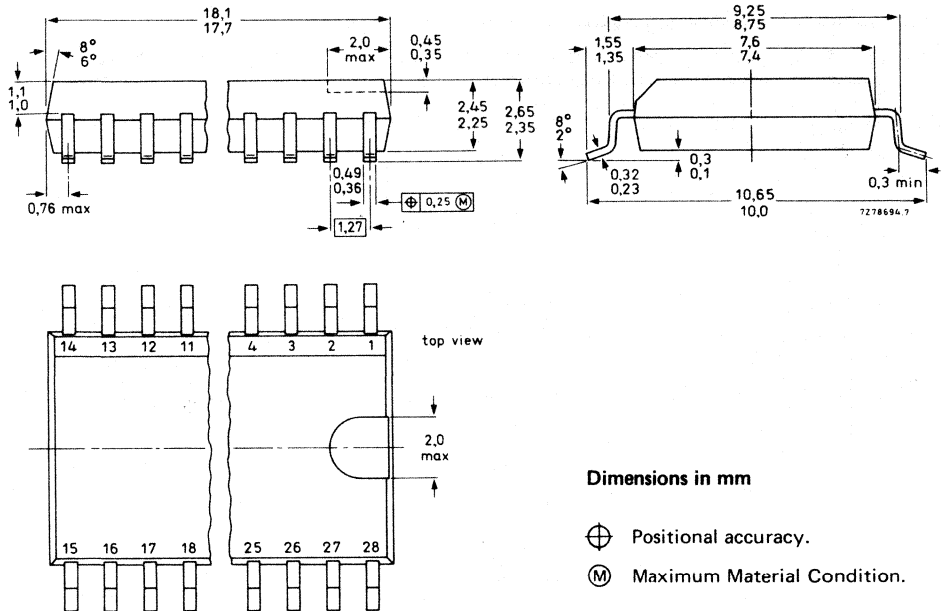


- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)



Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

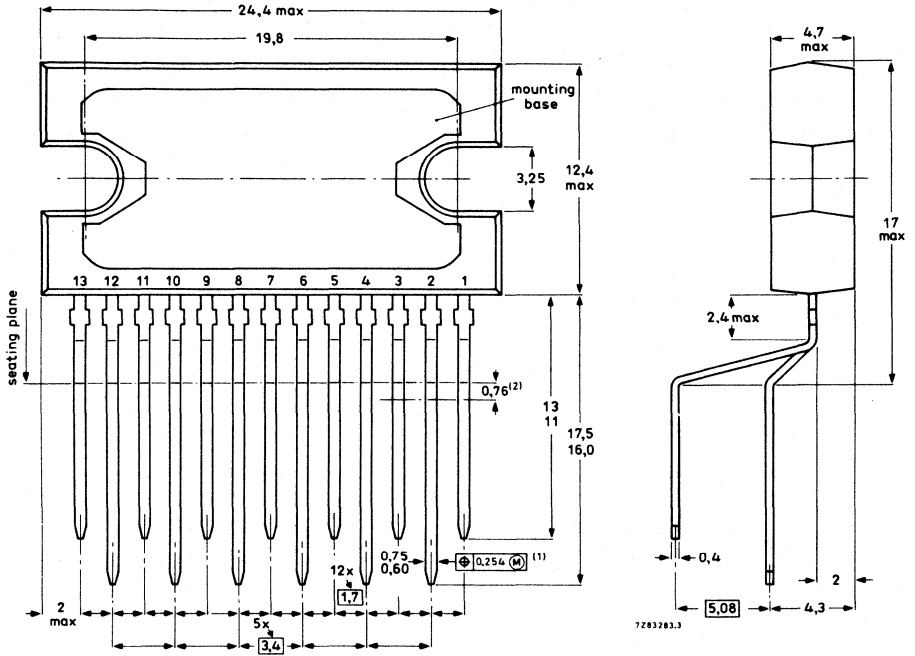
Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid. After soldering, the substrate must be cleaned of any remaining flux.



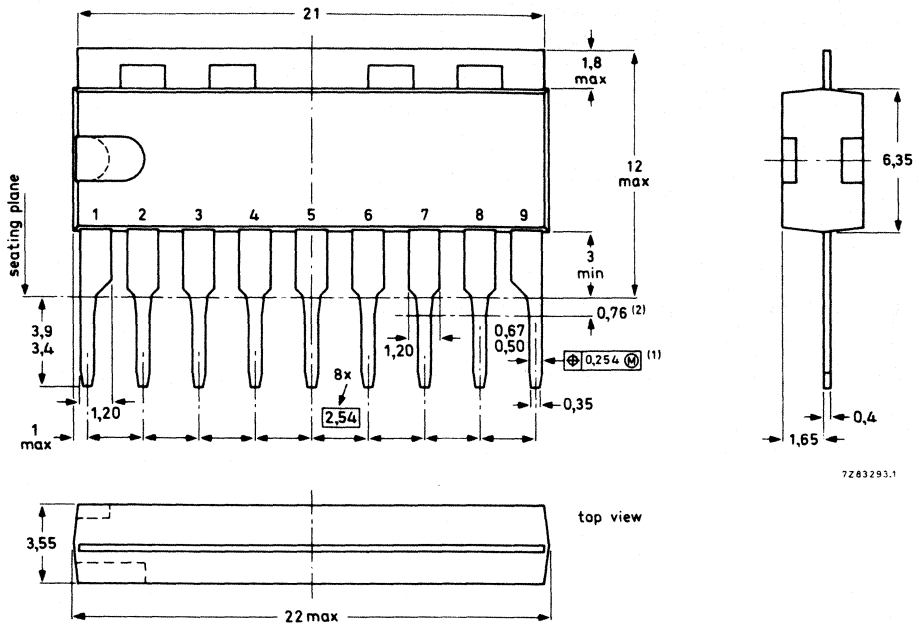
13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-141B)



Dimensions in mm

- ⊕ Positional accuracy.
  - Ⓜ Maximum Material Condition.
- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
  - (2) Lead spacing tolerances apply from seating plane to the line indicated.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-142)



7283293.1

Dimensions in mm

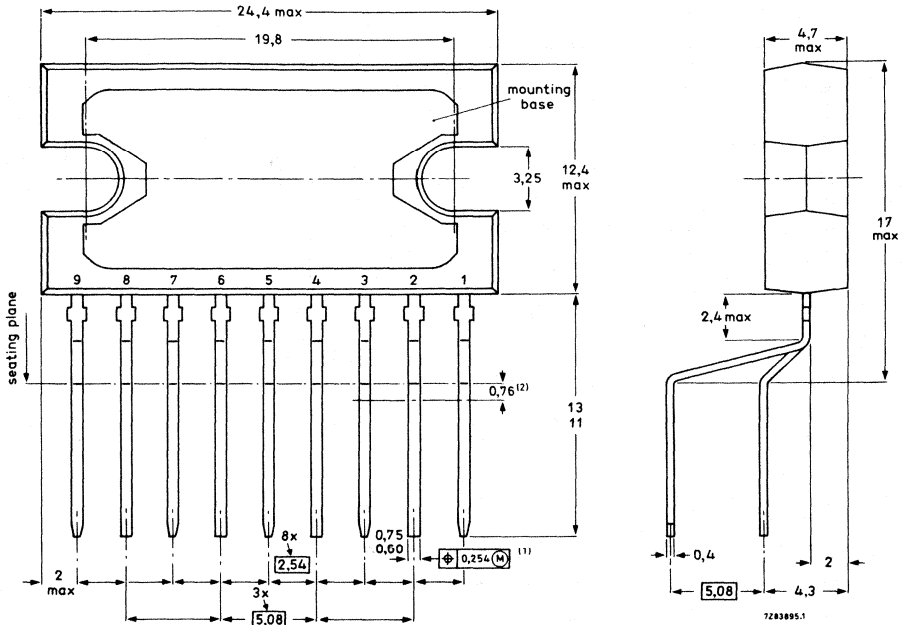
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.



9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-157A, B)



Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

**DEVICE DATA**







## INTEGRATED AMPLIFIER for use in ear hearing aids

Monolithic integrated circuit amplifier in a plastic envelope, primarily intended for use in ear hearing aids.

### QUICK REFERENCE DATA

For meaning of symbols see test circuit on page 3

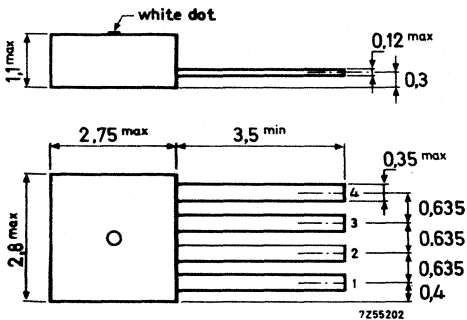
Supply voltage	$V_{1-3}$	max.	5 V
Supply current	$I_2$	max.	5 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	25 mW

The following data are measured in test circuit on page 3

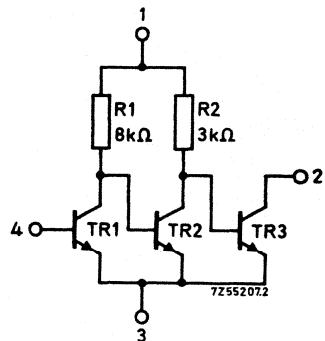
Total supply current	$I_{tot}$	typ.	1 mA
Transducer gain	$G_{tr}$	>	77 dB
		typ.	85 dB
Output power at $d_{tot} = 10\%$	$P_o$	>	0,2 mW
Cut-off frequency (-3 dB)	$f_c$	>	20 kHz

### PACKAGE OUTLINE (Dimensions in mm)

SOT-20



### CIRCUIT DIAGRAM



The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

For meaning of symbols test circuit on page 3.

Voltages

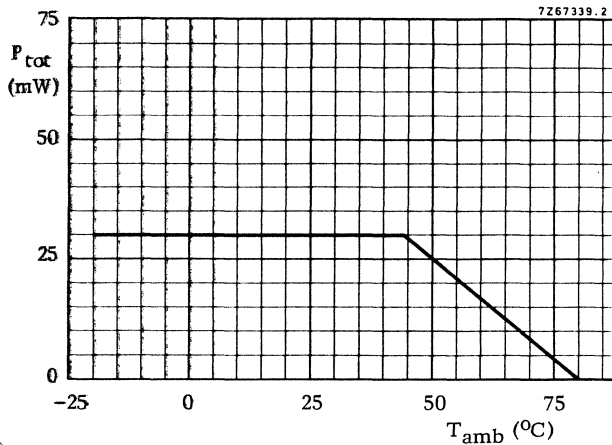
Supply voltage	$V_{1-3}$	max.	5 V
Output voltage	$V_{2-3}$	max.	5 V <sup>1)</sup>
Input voltage	$-V_{4-3}$	max.	5 V

Currents

Output current	$I_2$	max.	5 mA
Input current	$I_4$	max.	5 mA

Power dissipation

Power derating curve



Temperatures

Storage temperature	$T_{stg}$	-20 to +80 °C
Ambient temperature (see derating curve above)	$T_{amb}$	-20 to +80 °C

1) This value may be exceeded during inductive switch-off for transient energies < 10µWs.

**CHARACTERISTICS** at  $V_{1-3} = 1,3 \text{ V}$ ;  $I_2 = 0,7 \text{ mA}$  and  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Supply currents (no signal)

$I_{\text{tot}}$	<	1,1	mA
$I_1$	typ.	0,30	mA

Transducer gain at  $f = 1 \text{ kHz}$

$G_{\text{tr}}$	>	77	dB
	typ.	85	dB

Total distortion at  $f = 1 \text{ kHz}$

$P_o = 100 \text{ } \mu\text{W}$

$d_{\text{tot}}$	typ.	4	%
	<	6	%

$P_o = 200 \text{ } \mu\text{W}$

$d_{\text{tot}}$	<	10	%
------------------	---	----	---

Noise figure at  $R_S = 5 \text{ k}\Omega$

$B = 400 \text{ to } 3200 \text{ Hz}$

$F$	typ.	2,5	dB
	<	6	dB

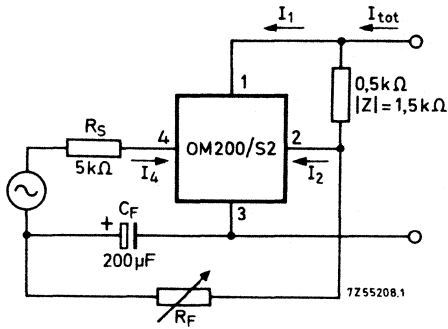
Cut-off frequency (-3 dB)

$f_c$	>	20	kHz
-------	---	----	-----

Value of  $R_F$  to adjust  $I_2$  at  $0,7 \text{ mA}$

$R_F$	170 to 1000	k $\Omega$
	typ.	400

Test circuit



Note

$I_2 = 0,7 \text{ mA}$ ; adjusted by means of  $R_F$   
 $V_{1-3} = 1,3 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

1) The transducer gain is defined as the ratio of the output power in the load  $|Z| = 1,5 \text{ k}\Omega$  and the available input power of the source with  $R_S = 5 \text{ k}\Omega$ .

$$G_{\text{tr}} = \frac{P_o}{V_i^2 / 4 R_S}$$

2) Due to special processing and pre-measuring, the flutter-noise level is extremely low.

**SOLDERING RECOMMENDATIONS**

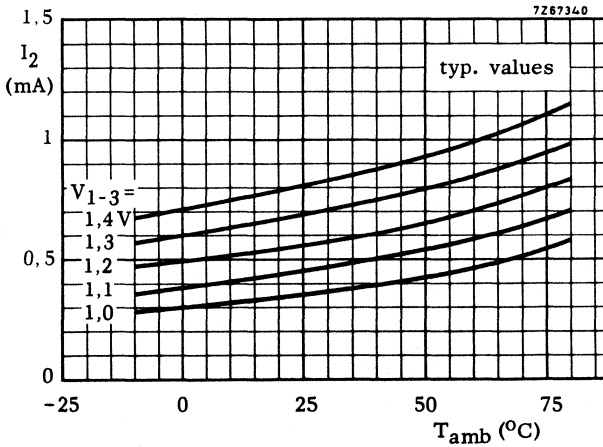
1. Iron soldering

At a maximum iron temperature of 300 °C the maximum permissible soldering time is 3 seconds, provided the solder spot is at least 0,5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

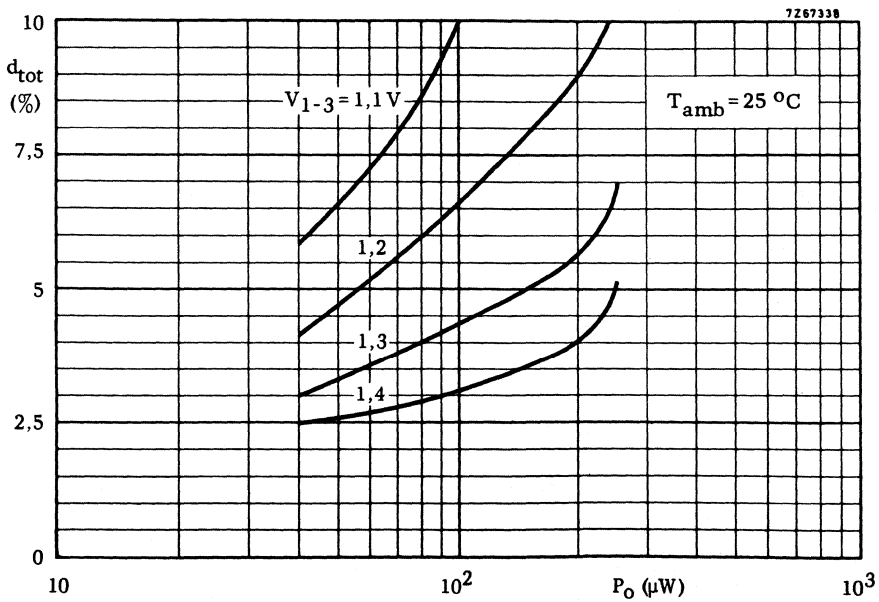
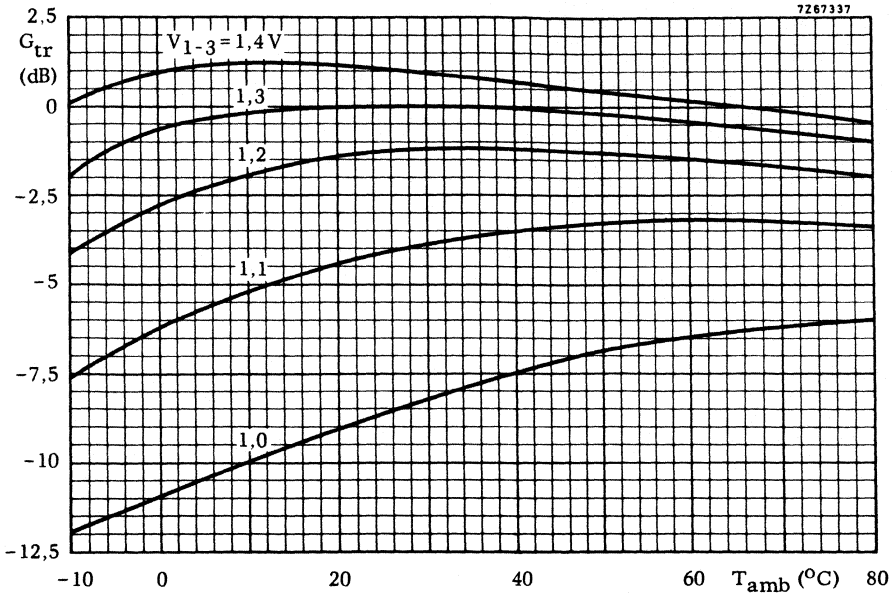
2. Dipsoldering

At a maximum solder temperature of 250 °C the maximum permissible soldering time is 3 seconds, provided the soldered spot is at least 0,5 mm from the seal.

**CHARACTERISTICS**



The graph applies to test circuit on previous page.





## RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in  $I^2L$  technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

### Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

### QUICK REFERENCE DATA

Supply voltage ranges	$V_{CC1}$	3,6 to 12 V
	$V_{CC2}$	3,6 to 12 V
	$V_{CC3}$	$V_{CC2}$ to 31 V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18 mA
	$I_{CC3}$	typ. 0,8 mA
Input frequency ranges		
at pin FAM	$f_{FAM}$	512 kHz to 32 MHz
at pin FFM	$f_{FFM}$	70 to 120 MHz
Maximum crystal input frequency	$f_{XTAL}$	> 4 MHz
Operating ambient temperature range	$T_{amb}$	-25 to +80 °C

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

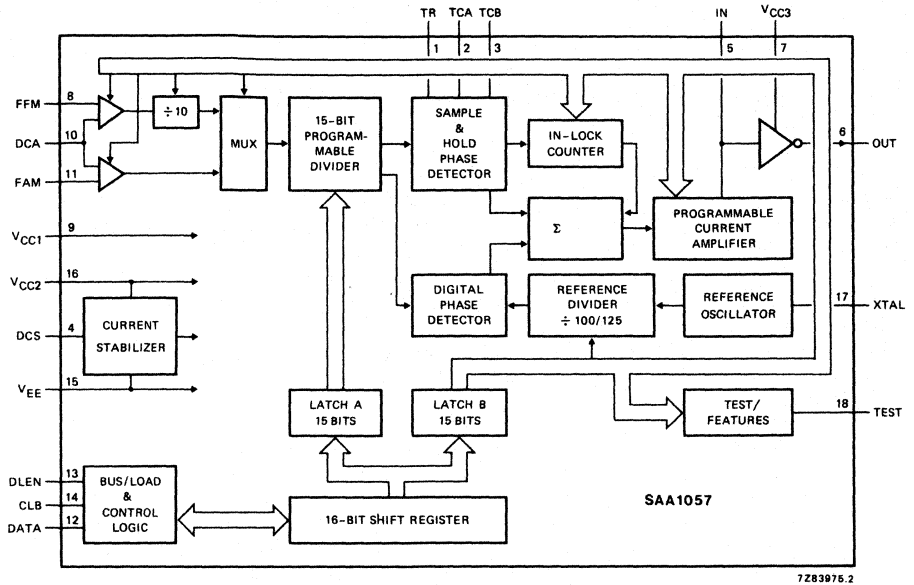


Fig. 1 Block diagram.

**GENERAL DESCRIPTION**

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges. The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.



**OPERATION DESCRIPTION****Control information**

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM FM/AM selection; '1' = FM, '0' = AM  
 REFH reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3 }  
 CP2 } control bits for the programmable current amplifier  
 CP1 } (see section Characteristics)  
 CP0 }

SB2 enables last 8 bits (SLA to T0) of data word B;  
 '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1 }  
 PDM0 } phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 test bit; must be programmed always '0'

T2 test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 test bit; must be programmed always '0'

T0 test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock



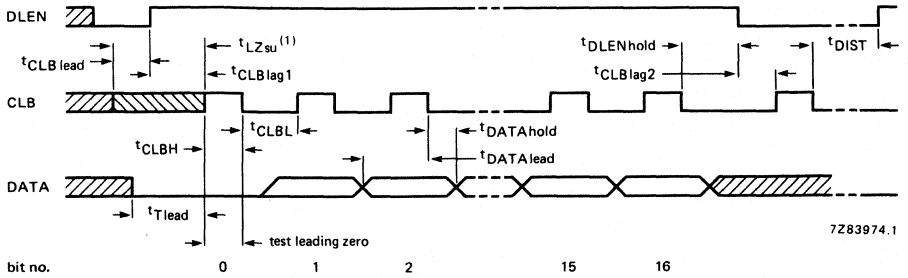


Fig. 2 BUS format.

(1) During the zero set-up time ( $t_{LZsu}$ ) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I<sup>2</sup>C bus is used for other devices on the same data and clock lines.

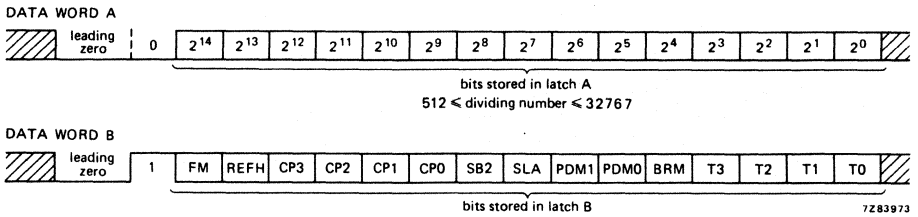


Fig. 3 Bit organization of data words A and B.



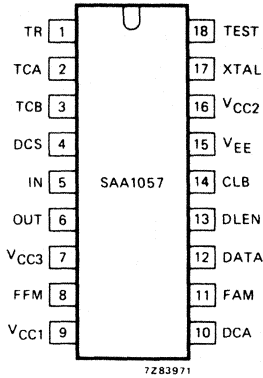


Fig. 4 Pinning diagram.

**PINNING**

1	TR	} resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V <sub>CC3</sub>	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V <sub>CC1</sub>	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	} BUS
13	DLEN	
14	CLB	
15	V <sub>EE</sub>	ground
16	V <sub>CC2</sub>	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V <sub>CC1</sub> ; V <sub>CC2</sub>	-0,3 to 13,2 V
Supply voltage; output amplifier	V <sub>CC3</sub>	V <sub>CC2</sub> to + 32 V
Total power dissipation	P <sub>tot</sub>	max. 800 mW
Operating ambient temperature range	T <sub>amb</sub>	-30 to + 85 °C
Storage temperature range	T <sub>stg</sub>	-65 to + 150 °C



## CHARACTERISTICS

 $V_{EE} = 0 \text{ V}; V_{CC1} = V_{CC2} = 5 \text{ V}; V_{CC3} = 30 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C};$  unless otherwise specified

	symbol	min.	typ.	max.	conditions
Supply voltages	$V_{CC1}$	3,6	5	12	V
	$V_{CC2}$	3,6	5	12	V
	$V_{CC3}$	$V_{CC2}$	—	31	V
Supply currents*					
AM mode	$I_{tot}$	—	16	—	mA
FM mode	$I_{tot}$	—	20	—	mA
	$I_{CC3}$	0,3	0,8	1,2	mA
Operating ambient temperature	$T_{amb}$	-25	—	+80	$^\circ\text{C}$
<b>RF inputs (FAM, FFM)</b>					
AM input frequency	$f_{FAM}$	512 kHz	—	32	MHz
FM input frequency	$f_{FFM}$	70	—	120	MHz
Input voltage at FAM	$V_i$ (rms)	30	—	500	mV
Input voltage at FFM	$V_i$ (rms)	10	—	500	mV
Input resistance at FAM	$R_i$	—	2	—	$\text{k}\Omega$
Input resistance at FFM	$R_i$	—	135	—	$\Omega$
Input capacitance at FAM	$C_i$	—	3,5	—	pF
Input capacitance at FFM	$C_i$	—	3	—	pF
Voltage ratio allowed between selected and non-selected input	$V_S/V_{ns}$	—	-30	—	dB
<b>Crystal oscillator (XTAL)</b>					see note 1
Maximum input frequency	$f_{XTAL}$	4	—	—	MHz
Crystal series resistance	$R_s$	—	—	150	$\Omega$
<b>BUS inputs (DLEN, CLB, DATA)</b>					
Input voltage LOW	$V_{IL}$	0	—	0,8	V
Input voltage HIGH	$V_{IH}$	2,4	—	$V_{CC1}$	V
Input current LOW	$-I_{IL}$	—	—	10	$\mu\text{A}$
Input current HIGH	$I_{IH}$	—	—	10	$\mu\text{A}$

 $I_{tot} = I_{CC1} + I_{CC2}$   
 in-lock: BRM = '1';  
 PDM = '0'  
 $I_{OUT} = 0$ 

\* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

## CHARACTERISTICS (continued)

 $V_{EE} = 0 \text{ V}; V_{CC1} = V_{CC2} = 5 \text{ V}; V_{CC3} = 30 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C};$  unless otherwise specified

	symbol	min.	typ.	max.	conditions
<b>BUS inputs timing</b> (DLEN, CLB, DATA)					see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	—	—	$\mu\text{s}$
Lead time for DATA to the first CLB pulse	$t_{Tlead}$	0,5	—	—	$\mu\text{s}$
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	—	—	$\mu\text{s}$
CLB pulse width HIGH	$t_{CLBH}$	5	—	—	$\mu\text{s}$
CLB pulse width LOW	$t_{CLBL}$	5	—	—	$\mu\text{s}$
Set-up time for DATA to CLB	$t_{DATAlead}$	2	—	—	$\mu\text{s}$
Hold time for DATA to CLB	$t_{DATAhold}$	0	—	—	$\mu\text{s}$
Hold time for DLEN to CLB	$t_{DLENhold}$	2	—	—	$\mu\text{s}$
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	—	—	$\mu\text{s}$
Busy time from load pulse to next start of transmission	$t_{DIST}$	5	—	—	$\mu\text{s}$
Busy time asynchronous mode	$t_{DIST}$	0,3	—	—	ms
Busy time synchronous mode	$t_{DIST}$	1,3	—	—	ms
					next transmission after word 'B' to other device or next transmission to SAA1057 after word 'A' (see also note 5)
<b>Sample and hold circuit</b> (TR, TCA, TCB)					see also notes 3; 4
Minimum output voltage	$V_{TCA}$ $V_{TCB}$	—	1,3	—	V
Maximum output voltage	$V_{TCA}$ $V_{TCB}$	—	—	$V_{CC2} - 0,7$	V
Capacitance at TCA (external)	$C_{TCA}$ $C_{TCA}$	—	—	2,2 2,7	nF
Discharge time at TCA	$t_{dis}$	—	—	5	$\mu\text{s}$
	$t_{dis}$	—	—	6,25	$\mu\text{s}$
Resistance at TR	$R_{TR}$	100	—	—	$\Omega$
Voltage at TR during discharge	$V_{TR}$	—	0,7	—	V
Capacitance at TCB	$C_{TCB}$	—	—	10	nF
Bias current into TCA, TCB	$I_{bias}$	—	—	10	nA
					external in-lock



**CHARACTERISTICS** (continued)

$V_{EE} = 0 \text{ V}; V_{CC1} = V_{CC2} = 5 \text{ V}; V_{CC3} = 30 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C};$  unless otherwise specified

	symbol	min.	typ.	max.	conditions	
<b>Programmable current amplifier (PCA)</b>						
Output current of the dig. phase detector	$\pm I_{dig}$	—	0,4	—	mA	
Current gain of PCA						
		CP3	CP2	CP1	CP0	
P1	Gp1	0	0	0	0	$V_{CC2} \geq 5 \text{ V}$ (only for P1)
P2	Gp2	0	0	0	1	
P3	Gp3	0	0	1	0	
P4	Gp4	0	1	1	0	
P5	Gp5	1	1	1	0	
Ratio between the output current of S/H into PCA and the voltage on $C_{TCB}$	$S_{TCB}$	—	1,0	—	$\mu\text{A/V}$	
Offset voltage on TCB	$\Delta V_{TCB}$	—	—	1	V	in-lock
<b>Output amplifier (IN,OUT)</b>						
Input voltage	$V_{IN}$	—	1,3	—	V	{ in-lock; equal to internal reference voltage
Output voltages						
minimum	$V_{OUT}$	—	—	0,5	V	$-I_{OUT} = 1 \text{ mA}$
maximum	$V_{OUT}$	$V_{CC3-2}$	—	—	V	$I_{OUT} = 1 \text{ mA}$
maximum	$V_{OUT}$	$V_{CC3-1}$	—	—	V	$I_{OUT} = 0,1 \text{ mA}$
Maximum output current	$\pm I_{OUT}$	5	—	—	mA	$V_{OUT} = \frac{1}{2} V_{CC3}$
<b>Test output (TEST)*</b>						
Output voltage LOW	$V_{TL}$	—	—	0,5	V	
Output voltage HIGH	$V_{TH}$	—	—	12	V	
Output current OFF	$I_{Toff}$	—	—	10	$\mu\text{A}$	$V_{TH}$
Output current ON	$I_{Ton}$	150	—	—	$\mu\text{A}$	$V_{TL}$
<b>Ripple rejection**</b>						
at $f_{ripple} = 100 \text{ Hz}$						
$\Delta V_{CC1}/\Delta V_{OUT}$		—	77	—	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		—	70	—	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		—	60	—	dB	$V_{OUT} \leq V_{CC3-3 \text{ V}}$

\* Open collector output.

\*\* Measured in Fig. 6.

## NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.

The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

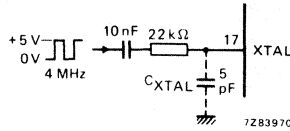


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically  $\frac{1}{2} V_{CC2} + 0,3 \text{ V}$  when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula  $\frac{1}{2} V_{CC2} + 0,3 \text{ V}$ .
4. Crystal oscillator frequency  $f_{XTAL} = 4 \text{ MHz}$ .
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057. When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time,  $5 \mu\text{s}$  will be sufficient.

## APPLICATION INFORMATION

## Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.

For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

## Synchronous/asynchronous operation

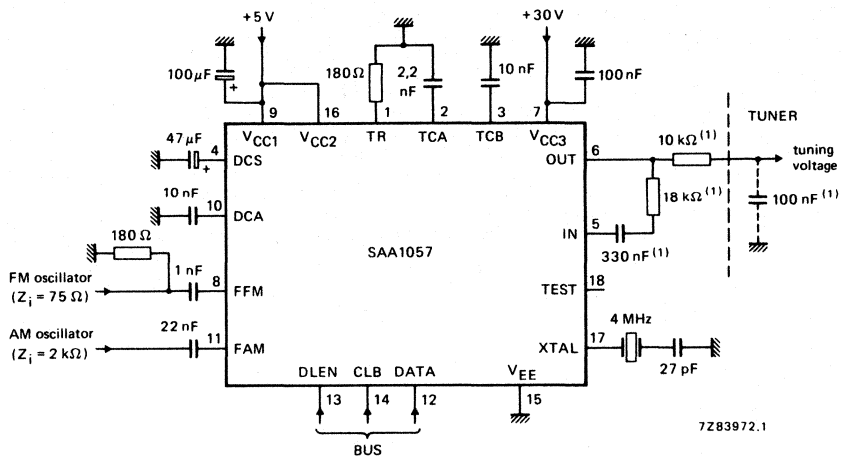
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

## Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage  $V_{CC2}$  is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

## Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced. ←



7Z83972.1

(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.



### 125 MHz AMPLIFIER AND DIVIDER-BY-32/33

The silicon monolithic integrated circuit SAA1059 is designed as a programmable-ratio divide-by-32/33 prescaler. It is intended for use in digital radio tuning systems and frequency counters in radio applications with an input frequency range from 0,5 to 125 MHz. The high-frequency inputs are differential inputs of a preamplifier for handling a.m. as well as f.m. oscillator signals. One output set provides complementary ECL levels by emitter followers and a second output buffer set is intended to drive MOS circuits by open collectors.

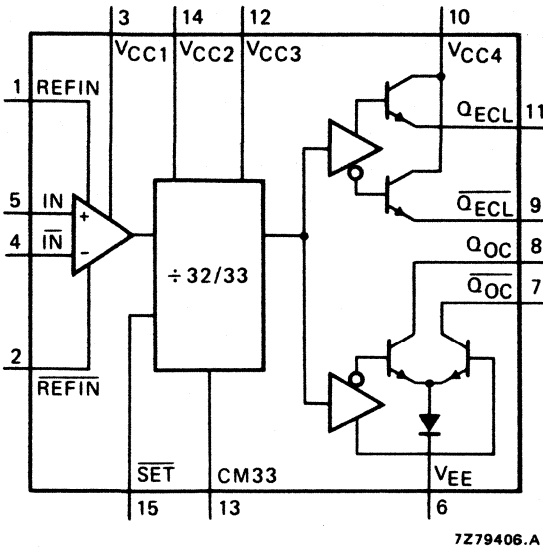


Fig. 1 Block diagram.

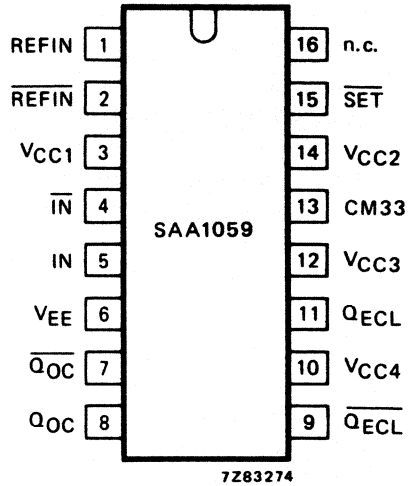


Fig. 2 Pin diagram.  
 VCC2 = 5 V (see Fig. 6)  
 VEE = 0 V (ground)  
 Pin 16 preferably connected to VEE

#### QUICK REFERENCE DATA

Supply voltage	V <sub>B</sub>	max.	14	V
	VCC2	typ.	5 ± 10%	V
Input frequency range	f <sub>i</sub>		0,5 to 125	MHz
Input voltage range	V <sub>i(rms)</sub>		5 to 100	mV
f = 0,5 to 30 MHz	V <sub>i(rms)</sub>		10 to 100	mV
f = 30 to 125 MHz	P <sub>tot</sub>	typ.	760	mW
Total power dissipation up to T <sub>amb</sub> = 60 °C				

#### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{CC2}$	max.	7 V
Output supply voltage (pins 7 and 8, $R_L = 470 \Omega$ )	$V_B$	max.	14 V
Input voltage	$V_I$		0 to $V_{CC}$
Total power dissipation up to $T_{amb} = 60^\circ\text{C}$	$P_{tot}$	max.	760 mW
Storage temperature	$T_{stg}$		-25 to +125 $^\circ\text{C}$
Operating ambient temperature	$T_{amb}$		-20 to +80 $^\circ\text{C}$

**CHARACTERISTICS** $V_{EE} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V}$ ;  $V_B = 9\text{ V}$ ;  $T_{amb} = 25^\circ\text{C}$ , unless otherwise specified.

Supply current ( $I_3 + I_{10} + I_{12} + I_{14}$ )*	$I_{CC}$	typ. <	110 mA 135 mA
Count input voltage*			
A.M. (0,5 MHz to 30 MHz) pin 5	$V_{i(rms)}$		5 to 100 mV
F.M. (30 MHz to 125 MHz) pin 4	$V_{i(rms)}$		10 to 100 mV
A.C. input impedance at 1 MHz	$Z_4, Z_5$	>	1 k $\Omega$
Count mode input (pin 13)			
input voltage for division-ratio 32	$V_{CML}$	<	2 V
input voltage for division-ratio 33	$V_{CMH}$	>	3 V
input impedance	$Z_{13}$		1 to 1,5 k $\Omega$
Set-up time changing the division-ratio from 32 to 33 or vice versa	$t_{su}$	typ.	50 ns
Reset (pin 15)			
input voltage reset	$V_{RL}$	<	2 V
input voltage no reset	$V_{RH}$	>	3 V
input impedance	$Z_{15}$		1,7 to 2,6 k $\Omega$
Emitter follower outputs (pins 9 and 11)			
output voltage; $R_L = 4,7\text{ k}\Omega$ to ground	$V_{OH}$ $V_{OL}$	> <	3,7 V 3,3 V
Open collector outputs (pins 7 and 8)			
$V_B = 11\text{ V}$ ; $R_L = 470\ \Omega$ ; $I_B \leq 20\text{ mA}$			
Output voltage HIGH	$V_{OH}$	>	9 V
Output voltage LOW	$V_{OL}$	<	2 V

\* See Fig. 6.

## LED DISPLAY/INTERFACE CIRCUIT

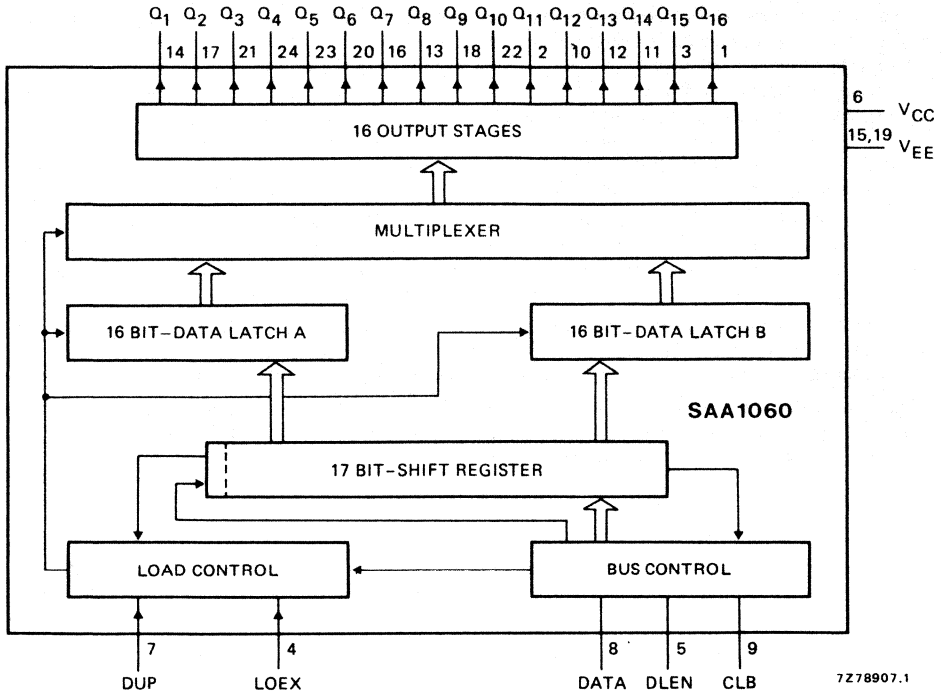
**Features**

Fig. 1 Block diagram.

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

**QUICK REFERENCE DATA**

Supply voltage range	$V_{CC}$	4 to 6 V
Operating ambient temperature range	$T_{amb}$	-20 to +80 °C
Maximum input frequency	$f_I$	typ. 50 kHz
Supply current	$I_{CC}$	typ. 60 mA
Output current	$I_Q$	< 40 mA
Output current ( $Q_8$ and $Q_{16}$ only)	$I_Q$	< 80 mA

**PACKAGE OUTLINE**

24-lead DIL; plastic (SOT-101A).

**GENERAL DESCRIPTION**

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q<sub>8</sub> and Q<sub>16</sub>) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

**OPERATION DESCRIPTION**

**Data inputs (DLEN, DATA)**

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

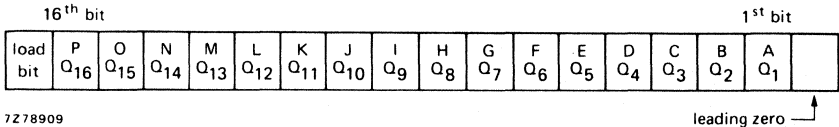


Fig. 2 Organization of a data word.

- Condition for 17th bit:
- 0 = load data latch B
  - 1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

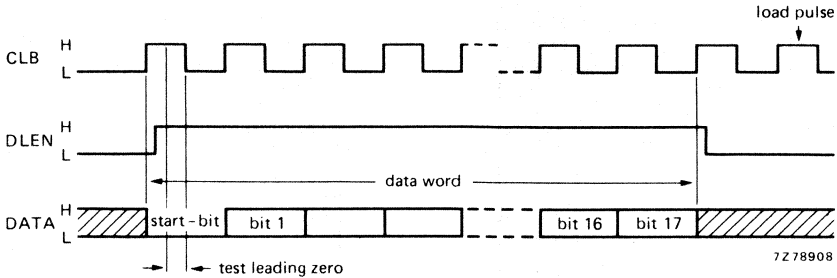


Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.

The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

**Data selection input (DUP)**

The logic states at input DUP determine which of the two latch contents can be found on the output.

- 0 = latch A contents
- 1 = latch B contents

**Load control input (LOEX)**

Input LOEX determines the operation mode in which the device is able to work.

- 0 = duplex mode, i.e. output synchronized with the duplex signal
- 1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.



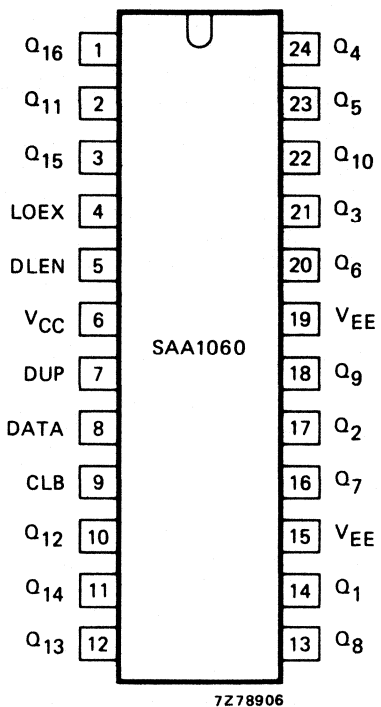


Fig. 4 Pinning diagram.

**RATINGS ( $V_{EE} = 0$ )**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_{CC}$	-0,3 to + 7 V
Total power dissipation	$P_{tot}$	max. 900 mW
Operating ambient temperature range	$T_{amb}$	-20 to + 80 °C
Storage temperature range	$T_{stg}$	-25 to + 125 °C

## CHARACTERISTICS

 $V_{EE} = 0$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

	$V_{CC}$ V	symbol	min.	typ.	max.	conditions
Supply voltage	—	$V_{CC}$	4	5	6	V
Supply current	5	$I_{CC}$	—	60	—	mA
Inputs DATA, CLB, DLEN, LOEX						
input voltage HIGH	5	$V_{IH}$	2	—	5	V
input voltage LOW	5	$V_{IL}$	—	—	1	V
input current LOW	5	$-I_{IL}$	—	—	20	$\mu\text{A}$
maximum input frequency	5	$f_i$	—	50	—	kHz
Input DUP						
input voltage HIGH	5	$V_{IH}$	0,8	—	12	V
input voltage LOW	5	$V_{IL}$	—6	—	0,4	V
input current HIGH	5	$I_{IH}$	0,01	—	12	mA
maximum input frequency	5	$f_i$	—	50	—	kHz
Outputs Q <sub>1</sub> to Q <sub>7</sub> , Q <sub>9</sub> to Q <sub>15</sub>						
output voltage HIGH	5	$V_{QH}$	—	—	16,8	V
output voltage LOW	5	$V_{QL}$	—	—	0,5	V
output current LOW duplex mode	5	$I_{QL}$	—	—	60	mA
d.c. mode	5	$I_{QL}$	—	20	40	mA
Outputs Q <sub>8</sub> and Q <sub>16</sub>						
output voltage HIGH	5	$V_{QH}$	—	—	16,8	V
output voltage LOW	5	$V_{QL}$	—	—	0,5	V
output current LOW duplex mode	5	$I_{QL}$	—	—	120	mA
d.c. mode	5	$I_{QL}$	—	40	80	mA





## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

SAA1062A  
SAA1062AT

# LCD DISPLAY/INTERFACE CIRCUIT

## GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an l.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

## Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

## QUICK REFERENCE DATA

Supply voltage range	$V_{CC}$	4,2 to 5,5 V	
Operating ambient temperature range	$T_{amb}$	-20 to +70 °C	
-----			
Maximum input frequency	$f_i$	typ.	50 kHz
Supply current	$I_{CC}$	typ.	3,5 mA
Output current ( $Q_1$ to $Q_{20}$ )	$I_Q$	>	60 $\mu$ A

## PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).

SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

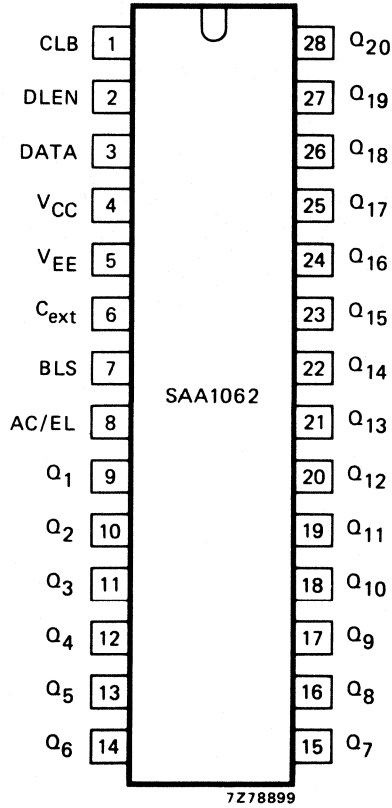


Fig. 1 Pinning diagram.



DEVELOPMENT SAMPLE DATA

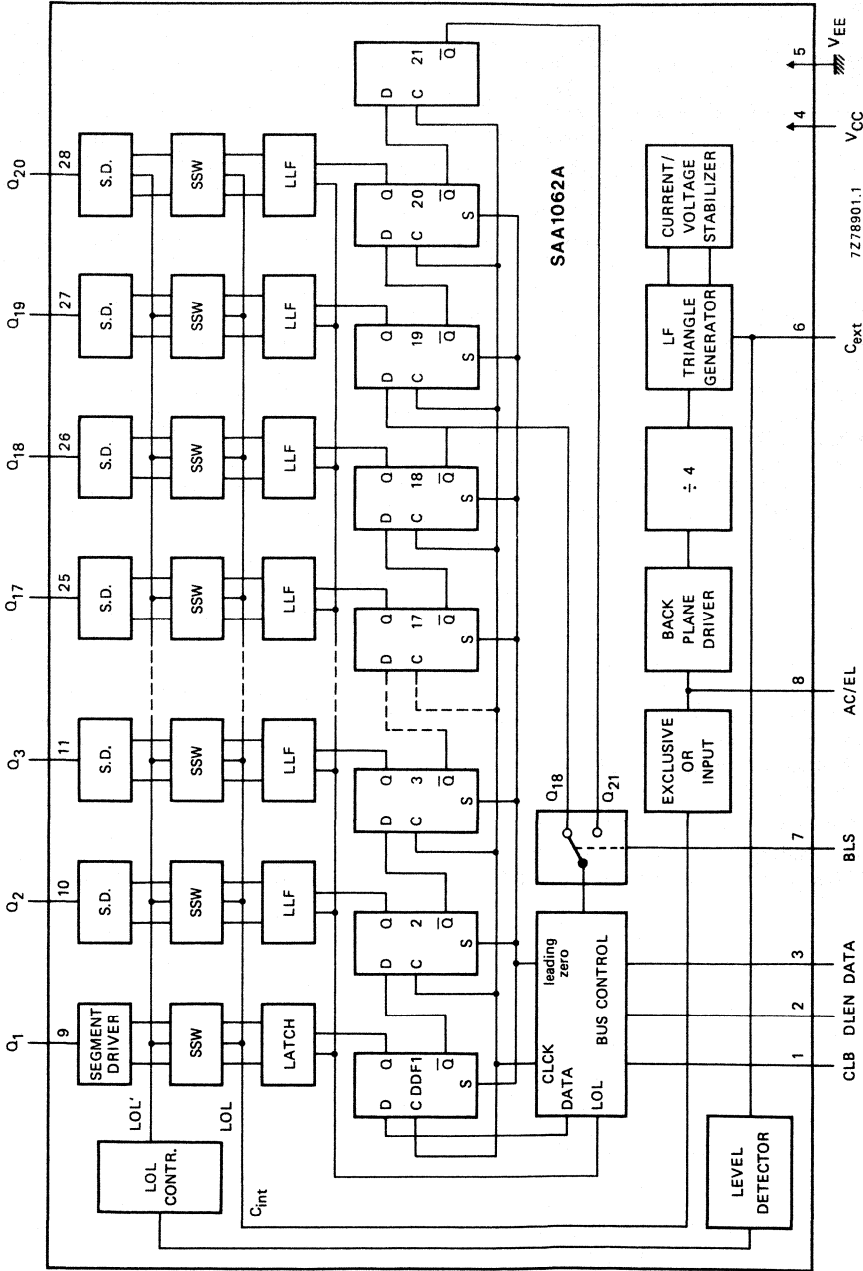


Fig. 2 Block diagram.



### OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting interferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The  $Q_n$  position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL).

This pulse enables the load control circuit to load the contents of the register into the output latch immediately. On the first edge of the backplane driver signal "AC out/EL in" following on this "LOL" pulse, the new information of this latch is transferred to the output driver which also contains a latch. With this ability it is possible to load the device with 20 bits and also to transfer this data to the segment outputs. Furthermore, the SR can be reloaded by a second complete load procedure without a load enable clock pulse. This causes the SR to contain 20 bits and the output latches another 20 bits of information.

The output driver also contains an EXCLUSIVE-OR which is driven by the backplane driver signal and the latch output. The segment driver output signal is in phase with the output of the backplane driver when the input data is HIGH ("1") and 180° out-of-phase when the input data is LOW ("0").

In the static or slave mode, the backplane output can be used as input by connecting pin 6 to ground or  $V_{CC}$ . The IC now can operate as a static driver or as a synchronized slave.

The l.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.



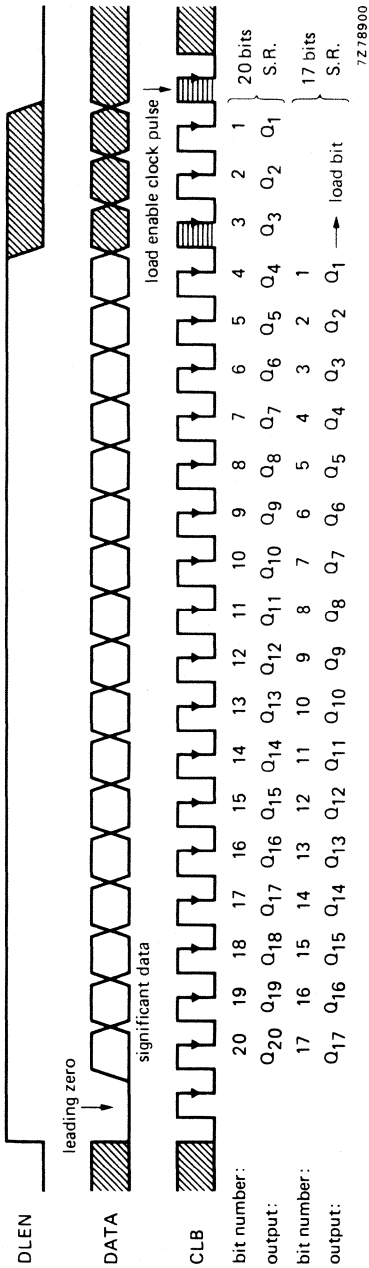


Fig. 3 Organization of 18 and 21 bit words; DATA = LOW means segment 'on'.



**RATINGS** ( $V_{EE} = 0$ )

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{CC}$	max.	6 V
Total power dissipation at $T_{amb} = 100\text{ }^{\circ}\text{C}$ derate linearly with 0,02 W/ $^{\circ}\text{C}$	$P_{tot}$	max.	500 mW
Operating ambient temperature range	$T_{amb}$	-25 to +125 $^{\circ}\text{C}$	
Storage temperature range	$T_{stg}$	-55 to +125 $^{\circ}\text{C}$	

**CHARACTERISTICS**

$V_{EE} = 0$ ;  $V_{CC} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified

	symbol	min.	typ.	max.	condition
Supply voltage	$V_{CC}$	4,2	5	5,5	V
Supply current	$I_{CC}$	-	3,5	-	mA
Inputs CLB, DLEN, DATA, BLS					
input voltage HIGH	$V_{IH}$	1,6	-	$V_{CC}$	V
input voltage LOW	$V_{IL}$	-1	-	+0,8	V
maximum input frequency	$f_i$	-	50	-	kHz
Input $C_{ext}$					
input voltage HIGH	$V_{IH}$	4,6	-	-	V
input voltage LOW	$V_{IL}$	-0,1	-	0,4	V
input current HIGH	$I_{IH}$	-	-	180	$\mu\text{A}$
input current LOW	$I_{IL}$	-	-	-40	$\mu\text{A}$
Input AC/EL (in slave mode)					
input voltage HIGH	$V_{IH}$	2,7	-	$V_{CC}$	V
input voltage LOW	$V_{IL}$	-0,4	-	2,3	V
Output $C_{ext}$ (oscillator mode)					
oscillator frequency	$f_{osc}$	120	240	360	Hz
Output stage backplane (AC/EL)					
output current sink/source	$I_O$	2,4	-	-	mA
Output $Q_1$ to $Q_2$					
output current sink/source	$I_O$	60	-	-	$\mu\text{A}$
d.c. rest voltage between pin 8 (AC/EL) and one of the segment drivers (see Fig. 4)					
segment 'on' situation		-	-	25	mV
segment 'off' situation		-	-	25	mV

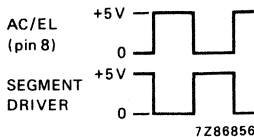


Fig. 4 AC/EL and segment driver pulses.  
The d.c. voltage for segment 'on' is about 5 V.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

SAA1063

# FLUORESCENT DISPLAY/INTERFACE CIRCUIT

## GENERAL DESCRIPTION

The SAA1063 is designed to drive the display unit of a digital tuning system. It contains a 17-bit shift register, latches, display multiplexers and output stages, capable of driving 4½ decades of a 7 segment fluorescent display in duplex mode. The decoding for the display is carried out in the data input (microcomputer).

### Features

- Driving 4½ decades of a seven segment display in duplex mode.
- Microcomputer compatible.
- 17-bit shift register.
- D.C. and duplex operation.

## QUICK REFERENCE DATA

Supply voltage range	$V_{CC}$		4 to 5,5	V
Operating ambient temperature range	$T_{amb}$		-20 to +80	°C
-----				
Maximum input frequency	$f_i$	min.	50	kHz
Supply current	$I_{CC}$	typ.	20	mA
Output current	$I_Q$	max.	1,5	mA
Maximum output voltage swing	$V_{Qmax}$	min.	34,5	V



## PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

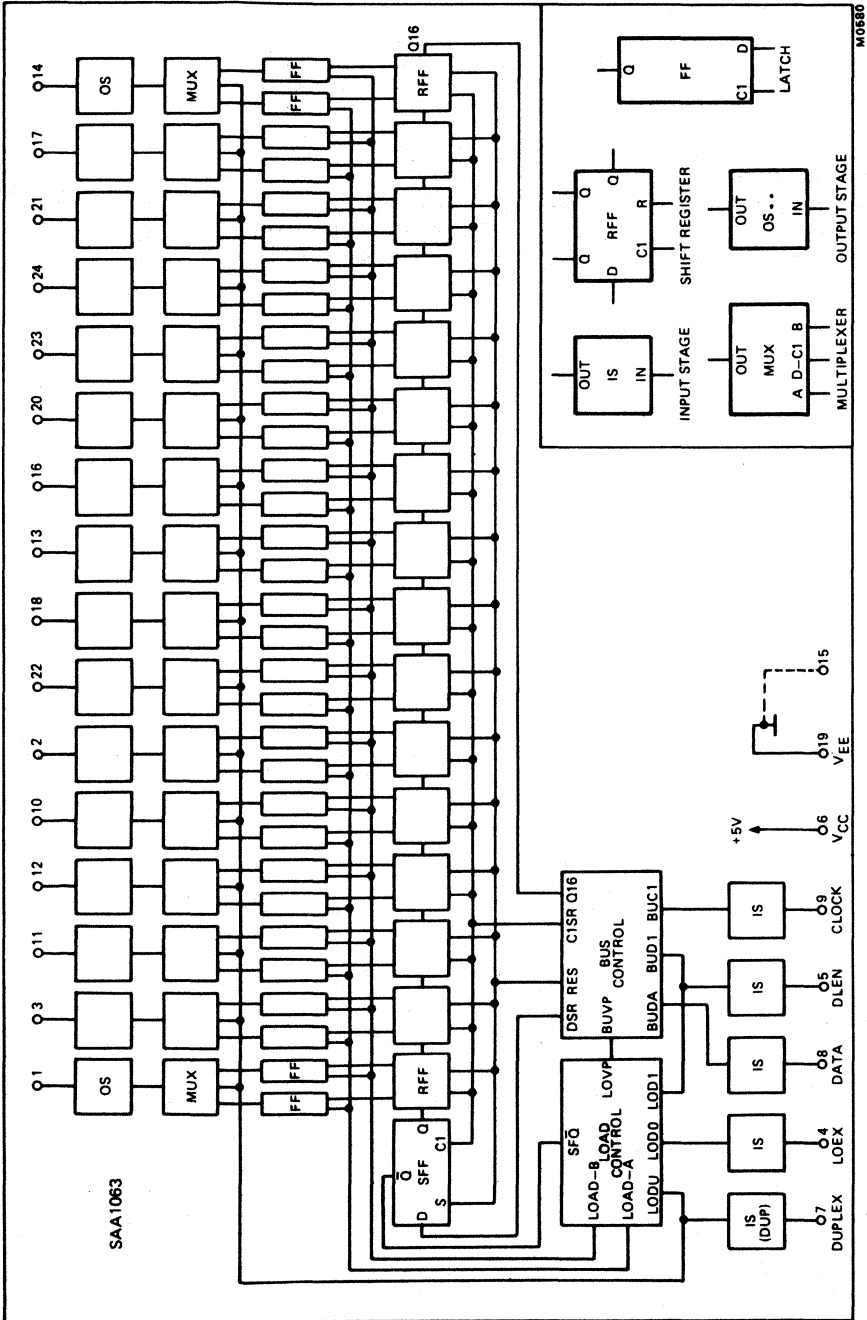


Fig. 1 Block diagram.  
Insert indicates structure of logic elements.



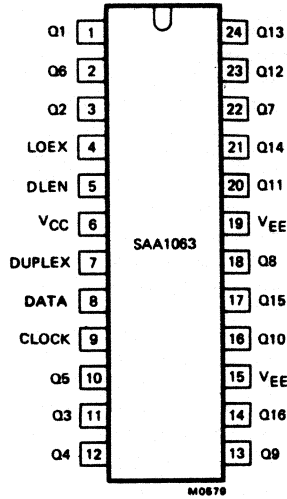


Fig. 2 Pinning diagram.

**PINNING**

- |           |                       |         |                       |
|-----------|-----------------------|---------|-----------------------|
| 1. Q1     |                       | 13. Q9  | segment drive outputs |
| 2. Q6     | segment drive outputs | 14. Q16 | segment drive outputs |
| 3. Q2     |                       | 15. VEE | ground                |
| 4. LOEX   | mode selection        | 16. Q10 |                       |
| 5. DLEN   | bus enable            | 17. Q15 | segment drive outputs |
| 6. VCC    | +5 V power supply     | 18. Q8  |                       |
| 7. DUPLEX | duplex input          | 19. VEE | ground                |
| 8. DATA   | data input            | 20. Q11 |                       |
| 9. CLOCK  | bus clock input       | 21. Q14 |                       |
| 10. Q5    |                       | 22. Q7  | segment drive outputs |
| 11. Q3    | segment drive outputs | 23. Q12 |                       |
| 12. Q4    |                       | 24. Q13 |                       |

DEVELOPMENT SAMPLE DATA



### OPERATION DESCRIPTION

The input information for this device consists of a data bus with 17 bit words, an external clock synchronized with the data bus and an enable signal. The data format of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is taken as to whether these signals are valid for this device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal HIGH, during the first HIGH period of the clock signal. During the HIGH period of the DLEN signal, the length control determines if the clock signal consists of 18 pulses. This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device accepting interference on the signal lines. If leading zero is detected the shift register is reset and then the data is written into this register. The reset position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input is correct. Incorrect length of the information is detected by checking the value of the last bit of the register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOVP). This pulse enables the load control circuit to load the contents of the register into one of the two latches. When the load bit of the data word is HIGH the register contents are loaded into latch A; when this load bit is LOW the register contents are loaded into latch B. When the data information is accepted this load bit is written into the first bit of the shift register.

In duplex mode the load pulse is synchronised by the duplex signal, to avoid current transients in the output stages during the loading of the latches. The duplex mode operates in one of two mode conditions. When LOEX (pin 4) is LOW the duplex mode condition is selected; when LOEX is HIGH the d.c. mode condition is selected. The output stages are switched to the contents of latch A and latch B respectively.

When the duplex input (pin 7) is LOW the contents of latch A can be found on the output, when this input is HIGH the contents of latch B are found on the output.

In the duplex mode condition the output stages are capable of driving 32 duplexed segments of a fluorescent display. However, in the d.c. mode condition the output stages can only drive 16 segments of the display and two SAA1063 devices are required to drive a 4½ decade display unit.



DEVELOPMENT SAMPLE DATA

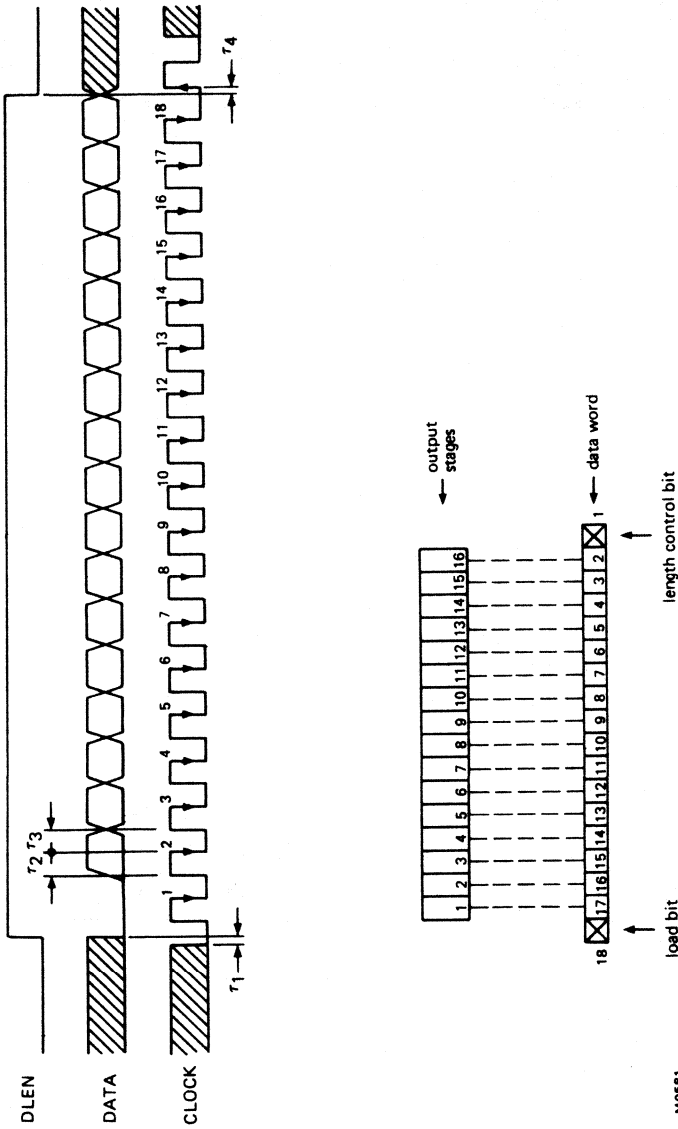


Fig. 3 Organisation of 18-bit data word.

Notes

1. The display segment is blanked by a HIGH data bit.
2. In duplex mode the period between the two data words must be greater than 21 ms.
3. Shaded timing periods are 'don't care' levels.
4.  $\tau_1 > 4 \mu s$  if a continuous clock is used.  $\tau_2$  and  $\tau_3 > 4 \mu s$ .  $\tau_4 > 2 \mu s$ .



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{CC}$	max.	6	V
Total power dissipation at $T_{amb} = 80\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	900	mW
Operating ambient temperature range	$T_{amb}$		-20 to +80	$^{\circ}\text{C}$
Storage temperature range	$T_{stg}$		-55 to +125	$^{\circ}\text{C}$

**CHARACTERISTICS**

$V_{EE} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

parameter	symbol	min.	typ.	max.		conditions
Supply voltage	$V_{CC}$	4	5	5,5	V	
Supply current	$I_{CC}$	-	20	-	mA	
<b>Inputs</b>						
LOEX, DLEN, DATA, CLOCK						
input voltage HIGH	$V_{IH}$	2	-	5	V	
input voltage LOW	$V_{IL}$	0	-	0,8	V	
input current	$-I_{IH}$	-	-	20	$\mu\text{A}$	$(V_I = 0\text{ V})$
max. input frequency	$f_i$	50	-	-	kHz	
<b>DUPLEX</b>						
input voltage HIGH	$V_{IH}$	0,8	-	20	V	
input voltage LOW	$V_{IL}$	-6	-	0,4	V	
input current HIGH	$I_{IH}$	0,01	-	12	mA	
input frequency	$f_i$	-	50	-	Hz	
<b>Outputs</b>						
Q1 to Q16						
output voltage HIGH	$-V_{OH}$	30	-	-	V	$I_O < 0,7\text{ }\mu\text{A}$
output voltage LOW	$V_{OL}$	4,5	-	-	V	$I_O = 1\text{ mA}$
output current	$I_{OL}$	-	-	1,5	mA	



## TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I<sup>2</sup>C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 100 mA in the ON state or sinking up to -100  $\mu$ A in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I<sup>2</sup>C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I<sup>2</sup>C bus. A subaddressing system allows the connection of up to three circuits on the same I<sup>2</sup>C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

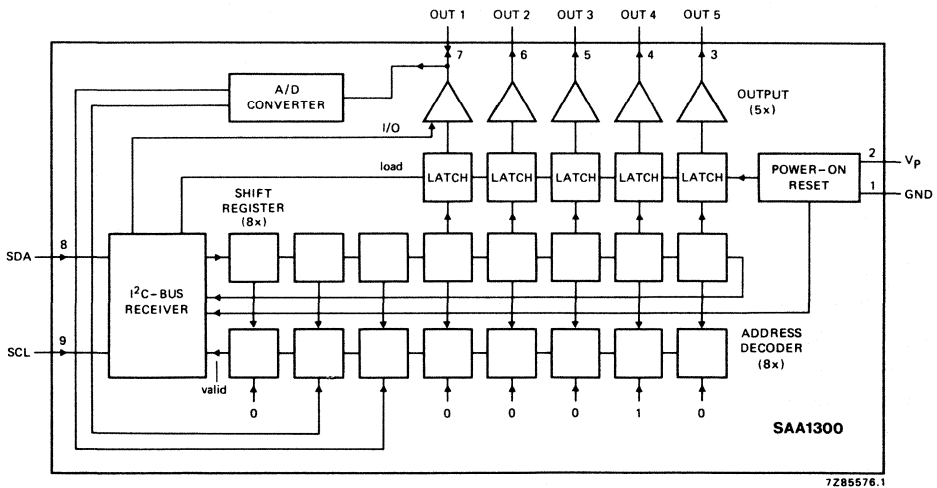


Fig. 1 Block diagram.

### PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142B).

## PINNING

pin no.	symbol	function
1	GND	ground
2	V <sub>p</sub>	positive supply
3	OUT 5	} outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line
9	SCL	serial clock line

} I<sup>2</sup>C bus

## I<sup>2</sup>C BUS INFORMATION\*

Address, first byte

0 1 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if V <sub>OUT 1</sub> = V <sub>OUT L</sub> (LOW)
1	0	OUT 1 = input	address accepted if V <sub>OUT 1</sub> = V <sub>OUT H</sub> (HIGH)
1	1	OUT 1 = input	address accepted if V <sub>OUT 1</sub> = V <sub>OUT M</sub> (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V <sub>p</sub>	max.	13,2 V
Input voltage range at SDA, SCL	V <sub>I</sub>		-0,5 to + 13,7 V
Input voltage range at OUT 1	V <sub>I</sub>		-0,5 to + 12,5 V
Output voltage range at OUT 1 to OUT 5	V <sub>O</sub>		-0,5 to + 12,5 V
Input current at SDA, SCL	I <sub>I</sub>	max.	20 mA
Input current at OUT 1	I <sub>I</sub>	max.	20 mA
Total power dissipation	P <sub>tot</sub>	max.	650 mW
Storage temperature range	T <sub>stg</sub>		-40 to + 125 °C
Operating ambient temperature range	T <sub>amb</sub>		-20 to + 80 °C

\* Detailed information is given in a separate data sheet.

## CHARACTERISTICS

 $V_P = 8\text{ V}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 2)</b>					
Supply voltage range	$V_P$	4	—	12	V
Supply current	$I_P$	—	10	—	mA
Power-on reset level output stage in "OFF" condition	$V_{PR}$	—	—	3,5	V
Maximum power dissipation*	$P_{\text{max}}$	—	650	—	mW
<b>Inputs SDA, SCL (pins 8 and 9)</b>					
Input voltage HIGH	$V_{IH}$	2,8	—	$V_P + 0,5$	V
Input voltage LOW	$V_{IL}$	0	—	1,8	V
Input current HIGH	$-I_{IH}$	—	—	50	$\mu\text{A}$
Input current LOW	$I_{IH}$	—	—	0,1	$\mu\text{A}$
Acknowledge sink current	$I_{ACK}$	2,5	—	—	mA
Maximum input frequency	$f_{i\text{max}}$	100	—	—	kHz
<b>Outputs OUT 1 to OUT 5 (pins 3 to 7)</b>					
Maximum output current; source: "ON"	$I_{Oso}$	+ 100	—	+ 150	mA
Maximum output current; source: "ON" $T_{\text{amb}} = 80\text{ }^\circ\text{C}$	$I_{Oso}$	60	—	—	mA
Output voltage HIGH at $I_{Oso}$	$V_{OH}$	—	—	$V_P - 2$	V
Output current; sink: "OFF"	$I_{Osi}$	-100	-300	—	$\mu\text{A}$
Output voltage LOW at $I_{Osi}$	$V_{OL}$	—	—	100	mV
Output voltage MEDIUM at $I_O = 12,5\text{ mA}$	$V_{OM}$	—	—	$V_P - 0,5$	V
<b>OUT 1 used as subaddressing input</b>					
Input voltage HIGH (code 1 0)	$V_{OUT\ 1H}$	0,72 $V_P$	—	$V_P$	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\ 1M}$	0,39 $V_P$	—	0,61 $V_P$	V
Input voltage LOW (code 0 1)	$V_{OUT\ 1L}$	0	—	0,28 $V_P$	V

\* Outputs must not be driven simultaneously at maximum source current.





## LOW-LEVEL AMPLIFIER

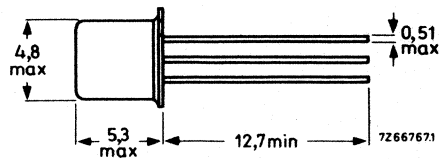
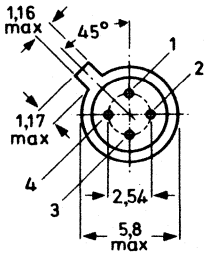
The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

### QUICK REFERENCE DATA

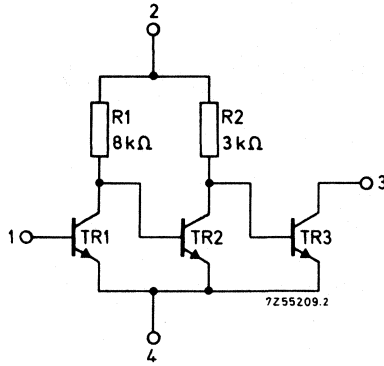
Supply voltage	$V_B$	max.	8 V
Output voltage	$V_{3-4}$	max.	7 V
Output current	$I_3$	max.	25 mA
Transducer gain at $P_o = 10$ mW $R_L = 150 \Omega$ ; $f = 1$ kHz	$G_{tr}$	typ.	77 dB
Operating ambient temperature	$T_{amb}$	-20 to +100	$^{\circ}C$

### PACKAGE OUTLINE TO-72 (SOT-18/17)

Dimensions in mm



**CIRCUIT DIAGRAM**



**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

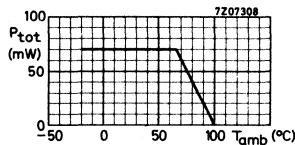
Supply voltage	$V_B$	max.	8 V
Output voltage	$V_{3-4}$	max.	7 V
Input voltage	$-V_{1-4}$	max.	5 V

Currents

Output current	$I_3$	max.	25 mA
Input current	$I_1$	max.	10 mA

Power dissipation

Total power dissipation up to $T_{amb} = 65^\circ\text{C}$	$P_{tot}$	max.	70 mW
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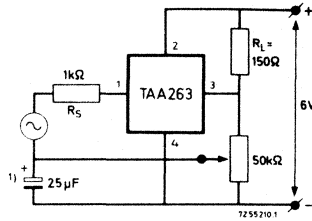
Temperatures

Storage temperature	$T_{stg}$	-55 to +125	$^\circ\text{C}$
Operating ambient temperature (see derating curve above)	$T_{amb}$	-20 to +100	$^\circ\text{C}$

## CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$

Test circuit:



### Currents

Output current	$I_3$	typ.	12 mA
Total current drain (no signal)	$I_2 + I_3$	<	16 mA

### Over-all small signal current gain

$f = 1\text{ kHz}$	$h_{f\text{ tot}}$	typ.	$5 \cdot 10^5$
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### Transducer gain

$f = 1\text{ kHz}; P_o = 10\text{ mW}$	$G_{tr}$	>	70 dB
		typ.	77 dB

<u>Output power</u> at $f = 1\text{ kHz}; d_{tot} = 10\%$	$P_o$	>	10 mW
$d_{tot} = 5\%$	$P_o$	>	8 mW

### Noise figure

$f = 400\text{ Hz to } 6\text{ kHz}$	$F$	typ.	5 dB
		<	10 dB
$f = 450\text{ kHz}; \Delta f = 5\text{ kHz}$	$F$	typ.	2.7 dB

<sup>1)</sup>  $Z \leq 10\text{ }\Omega$  at  $f = 1\text{ kHz}$

**CHARACTERISTICS** (continued)

$T_{amb} = 25\text{ }^{\circ}\text{C}$

y parameters (point 4 common connection)

$V_B = 6\text{ V}; I_3 = 3\text{ mA}; V_{3-4} = 4.2\text{ V}$

$f = 1\text{ kHz}$

Input admittance	$y_i = g_i$	typ.	20 $\mu\Omega^{-1}$
Transfer admittance	$y_f = g_f$	typ.	11 $\Omega^{-1}$
Output admittance	$y_o = g_o$	typ.	60 $\mu\Omega^{-1}$

$f = 450\text{ kHz}$

Input conductance	$g_i$	typ.	15 $\mu\Omega^{-1}$
Input capacitance	$C_i$	typ.	14 pF
Transfer admittance	$ y_f $	typ.	9.4 $\Omega^{-1}$
Phase angle of transfer admittance	$\varphi_f$	typ.	125 $^{\circ}$
Output conductance	$g_o$	typ.	20 $\mu\Omega^{-1}$
Output capacitance	$C_o$	typ.	13 pF



## INTEGRATED MOST AMPLIFIER

The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.

The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).

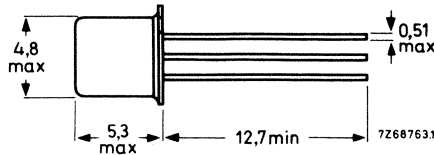
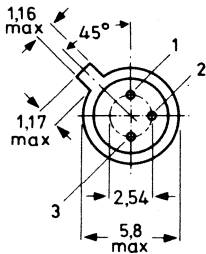
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

### QUICK REFERENCE DATA

Drain-source voltage ( $V_{GS} = 0$ )	$-V_{DSS}$	max.	20 V
Drain current	$-I_D$	max.	25 mA
Gate-source voltage $-I_D = 10 \text{ mA}; -V_{DS} = 10 \text{ V}$	$-V_{GS}$	typ.	11 V
Gate-source resistance $-V_{GS}$ up to 20 V; $T_j$ up to 125 °C	$r_{GS}$	>	100 G $\Omega$
Transfer admittance at $f = 1 \text{ kHz}$ $-I_D = 10 \text{ mA}; -V_{DS} = 10 \text{ V}$	$ y_{fs} $	typ.	75 m $\Omega^{-1}$

### PACKAGE OUTLINE TO-18 (SOT-18/13)

Dimensions in mm

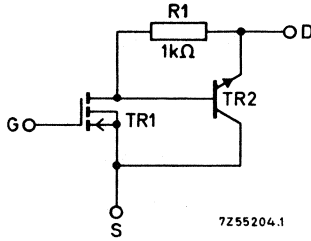


- 1 = drain
- 2 = gate
- 3 = source

Source connected to the case

Accessories supplied on request: 56246, 56263

## CIRCUIT DIAGRAM



**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

### Voltages

Drain-source voltage ( $V_{GS} = 0$ )  $-V_{DSS}$  max. 20 V

Gate-source voltage ( $I_D = 0$ )  $-V_{GSO}$  max. 20 V

Non repetitive peak gate-source voltage ( $t \leq 10$  ms)  $-V_{GSM}$  max. 100 V

### Current

Drain current  $-I_D$  max. 25 mA

### Power dissipation

Total power dissipation up to  $T_{amb} = 25^\circ\text{C}$   $P_{tot}$  max. 200 mW

### Temperatures

Storage temperature  $T_{stg}$   $-55$  to  $+125$   $^\circ\text{C}$

Operating ambient temperature  
(see derating curve on page 8)  $T_{amb}$   $-20$  to  $+125$   $^\circ\text{C}$

### **THERMAL RESISTANCE**

From junction to ambient in free air  $R_{th\ j-a} = 0.5$   $^\circ\text{C}/\text{mW}$

**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specifiedDrain current $-V_{DS} = 20\text{ V}; V_{GS} = 0$ 

$-I_{DSS}$	typ.	5 nA
	<	1 $\mu\text{A}$

Gate-source voltage <sup>1)</sup> $-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$ 

$-V_{GS}$	typ.	11 V
	9 to	14 V

Gate-source resistance $-V_{GS}$  up to 20 V;  $T_j$  up to 125  $^\circ\text{C}$ 

$r_{GS}$	>	100 G $\Omega$
----------	---	----------------

Equivalent noise voltage

$-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$   
 $B = 50\text{ Hz to }15\text{ kHz}$

$v_n$	typ.	25 $\mu\text{V}$
-------	------	------------------

y parameters at  $f = 1\text{ kHz}$  $-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$ 

Transfer admittance

$ y_{fs} $	typ.	75 $\text{m}\Omega^{-1}$
	40 to	120 $\text{m}\Omega^{-1}$

Input capacitance

$C_{is}$	typ.	8 pF
----------	------	------

Feedback capacitance

$-C_{rs}$	typ.	1.5 pF
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Output conductance

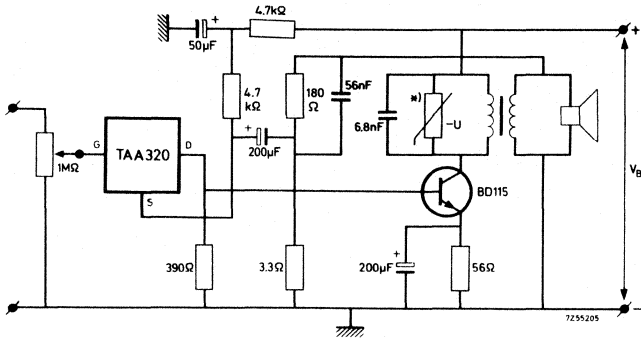
$g_{os}$	typ.	0.65 $\text{m}\Omega^{-1}$
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**NOTE**

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

1)  $-V_{GS}$  decreases about 6 mV/ $^\circ\text{C}$  with increasing ambient temperature at a constant  $-I_D$ .

## APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115



\* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

Supply voltage	$V_B$	=	100 V
Collector current of BD115	$I_C$	typ.	50 mA
Drain current of TAA320	$-I_D$	typ.	9.5 mA
Primary d.c. resistance of output transformer			140 $\Omega$
Primary inductance of output transformer			2.7 H
A.C. collector load for BD115			1.8 k $\Omega$

Performance at  $f = 1$  kHz; feedback = 16 dB

Output power at $d_{tot} = 10\%$ (on primary of the output transformer)	$P_O$	typ.	2.6 W
Input voltage for $P_O = 50$ mW	$V_{i(rms)}$	typ.	13.5 mV
Input voltage for $P_O = 2$ W	$V_{i(rms)}$	typ.	86 mV
Total distortion at $P_O = 2$ W	$d_{tot}$	typ.	3.6 %
Minimum frequency response (-3 dB)			60 Hz to 20 kHz
Signal-noise ratio at $P_O = 2$ W		typ.	73 dB

### Mounting instruction for BD115

Proper continuous operation is ensured up to  $T_{amb} = 50$  °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 cm<sup>2</sup> with a clamping washer of type 56218.

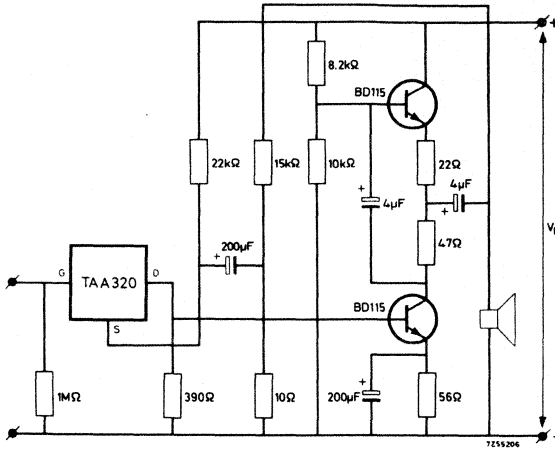
If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 cm<sup>2</sup>.

Recommended diameter of hole in heatsink: 7.7 mm.



## APPLICATION INFORMATION (continued)

4 W audio amplifier with TAA320 and 2 transistors of type BD115.

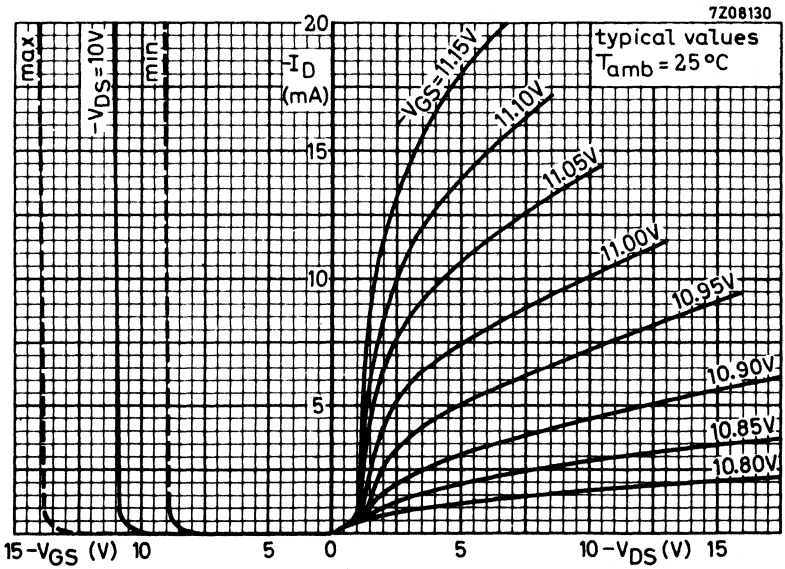
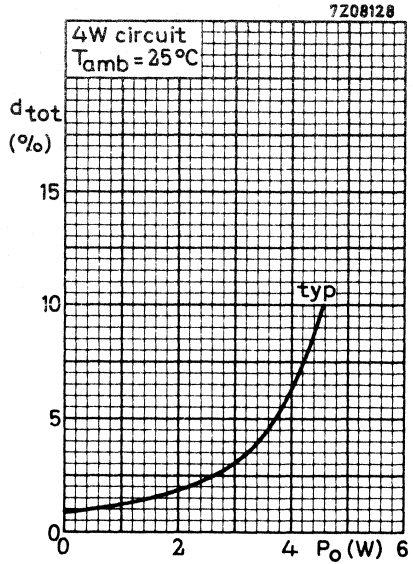
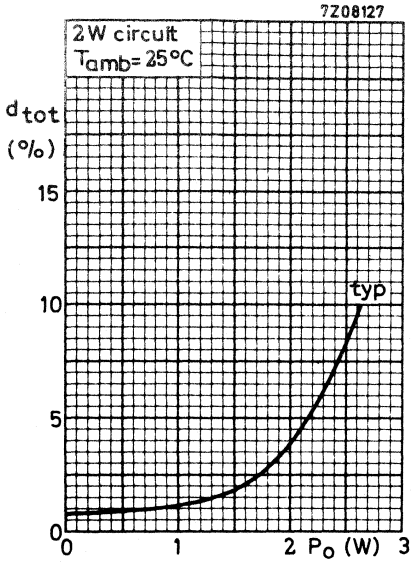


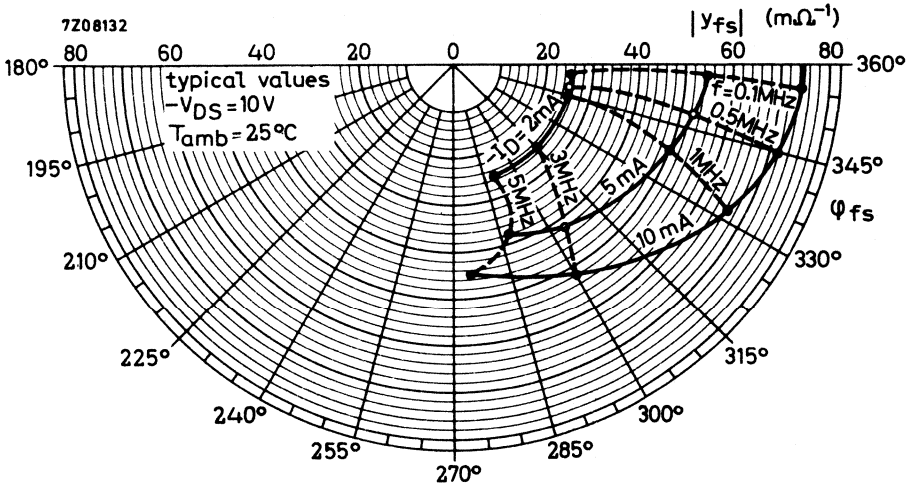
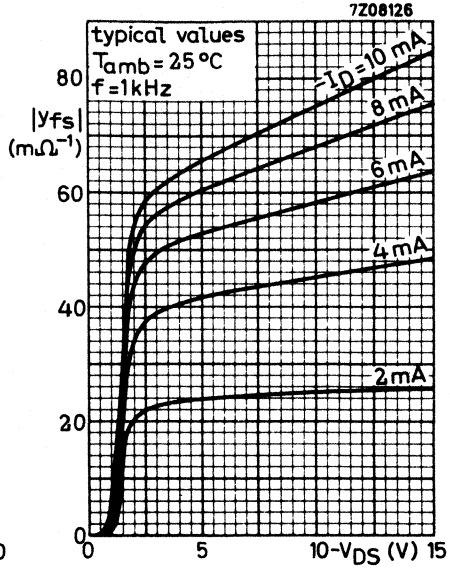
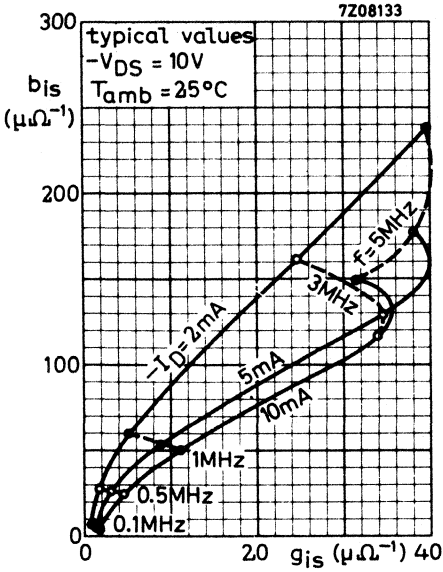
Supply voltage	$V_B$	=	200 V
Collector current of a BD115	$I_C$	typ.	52 mA
Drain current of TAA320	$-I_D$	typ.	8.6 mA

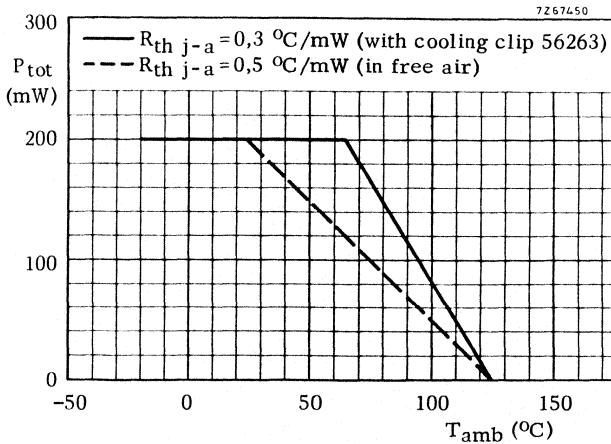
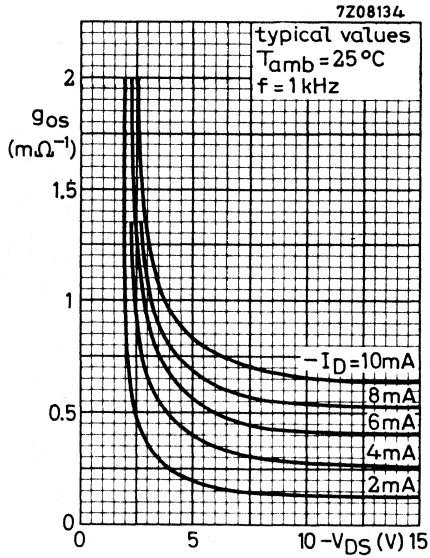
Performance at  $f = 1$  kHz; feedback = 12 dB

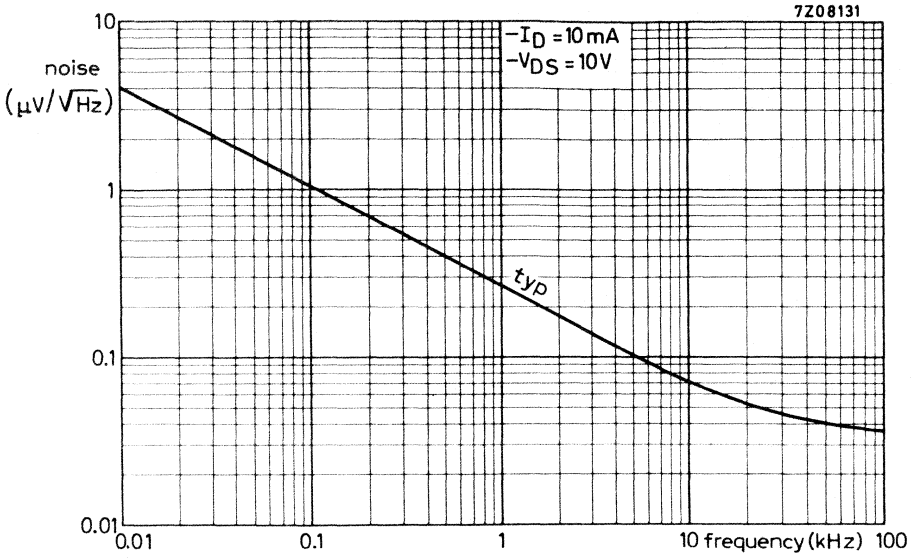
Output power at $d_{tot} = 10\%$	$P_O$	typ.	4.5 W
Input voltage for $P_O = 50$ mW	$V_i(\text{rms})$	typ.	7.5 mV
Input voltage for $P_O = 4$ W	$V_i(\text{rms})$	typ.	67 mV
Total distortion at $P_O = 4$ W	$d_{tot}$	typ.	6 %
Minimum frequency response (-3 dB)			50 Hz to 20 kHz
Signal-noise ratio at $P_O = 4$ W		typ.	73 dB

Mounting instruction for BD115 see page 4











## INTEGRATED MOST LEVEL SENSOR

The TAA320A is a silicon monolithic integrated circuit, consisting of a p-channel enhancement type MOS transistor and an n-p-n transistor, in a TO-18 metal envelope. The device is intended for level sensors with a very high input resistance (e.g. timing circuits, thermostats, liquid level sensors, flame control circuits).

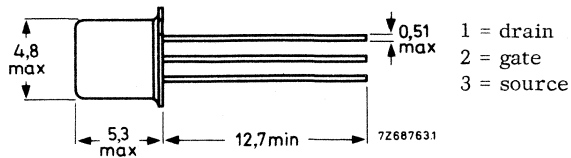
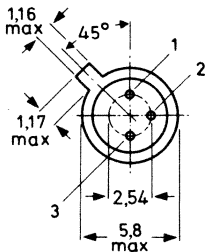
### QUICK REFERENCE DATA

Drain-source voltage ( $V_{GS} = 0$ )	$-V_{DSS}$	max.	20	V
Drain current	$-I_D$	max.	60	mA
Gate-source voltage <sup>1)</sup>				
$-I_D = 10 \text{ mA}; -V_{DS} = 10 \text{ V}$	group 1: $-V_{GS}$	typ.	10,6	V
			10,0 to 11,2	V
	group 2: $-V_{GS}$	typ.	11,3	V
			10,7 to 11,9	V
	group 3: $-V_{GS}$	typ.	12,0	V
			11,4 to 12,6	V
	group 4: $-V_{GS}$	typ.	12,7	V
			12,1 to 13,3	V
Gate cut-off current at $T_{amb} = 25 \text{ }^\circ\text{C}$				
$-V_{GS} = 20 \text{ V}; I_D = 0$	$-I_{GSO}$	typ.	1	pA
$-V_{GS} = 20 \text{ V}; V_{DS} = 0$	$-I_{GSS}$	typ.	1	pA

### PACKAGE OUTLINE

Dimensions in mm

TO-18 (SOT-18/13)

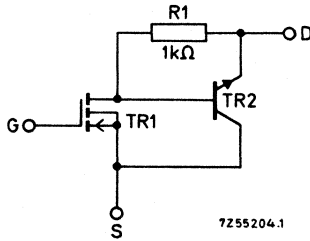


source connected to the case

Accessories supplied on request: 56246; 56263

<sup>1)</sup> For explanation of the group codefication see note b on page 81.

## CIRCUIT DIAGRAM



**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

### Voltages

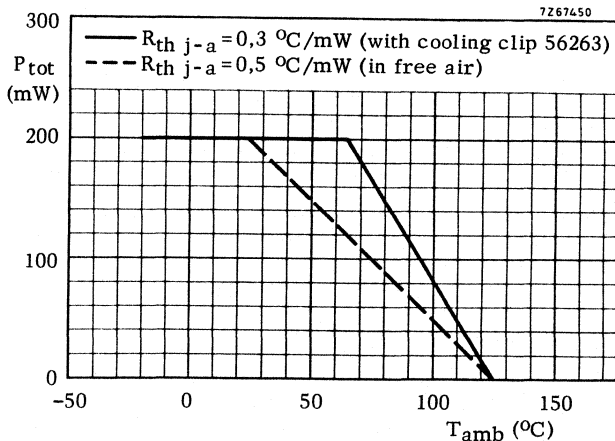
Drain-source voltage ( $V_{GS} = 0$ )	$-V_{DSS}$	max.	20 V
Gate-source voltage ( $I_D = 0$ )	$-V_{GSO}$	max.	20 V
Non-repetitive peak gate-source voltage ( $t \leq 10$ ms)	$\pm V_{GSM}$	max.	100 V

### Current

Drain current	$-I_D$	max.	60 mA
Peak drain current ( $t < 200$ ms; $\delta 0,001$ )	$-I_{DM}$	max.	100 mA

### Temperatures

Storage temperature	$T_{stg}$	-65 to +125	$^{\circ}\text{C}$
Operating ambient temperature (see curve below)	$T_{amb}$	-20 to +125	$^{\circ}\text{C}$





**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain current

$-V_{DS} = 20\text{ V}; V_{GS} = 0$	$-I_{DSS}$	typ.	5	nA
		<	1	$\mu\text{A}$

Drain-source voltage <sup>1)</sup>

$-I_D = 10\text{ mA}; -V_{GS} = 20\text{ V}$	$-V_{DS}$	<	1	V
$-I_D = 60\text{ mA}; -V_{GS} = 20\text{ V}$	$-V_{DS}$	<	1,5	V

Gate-source voltage (see note b)

$-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$	group 1: $-V_{GS}$	typ.	10,6	V
			10,0 to 11,2	V
	group 2: $-V_{GS}$	typ.	11,3	V
			10,7 to 11,9	V
	group 3: $-V_{GS}$	typ.	12,0	V
			11,4 to 12,6	V
	group 4: $-V_{GS}$	typ.	12,7	V
			12,1 to 13,3	V

Gate cut-off current

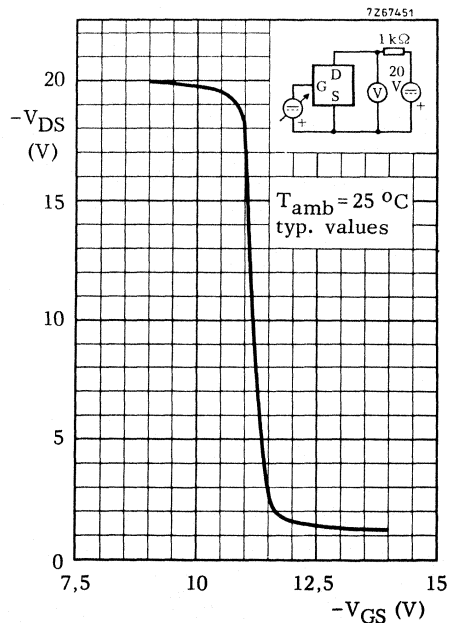
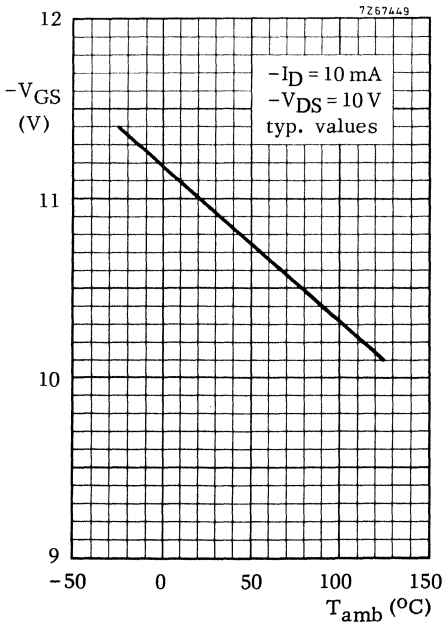
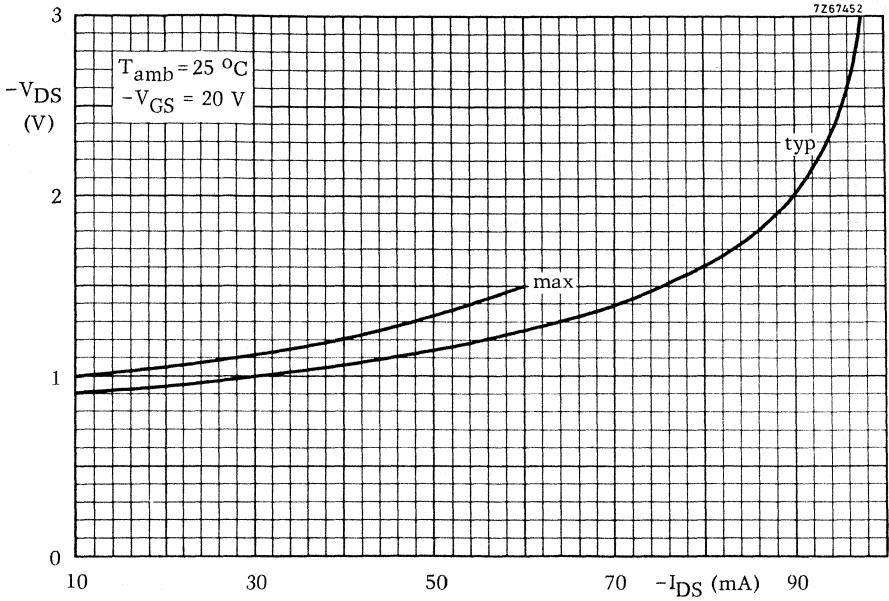
$-V_{GS} = 20\text{ V}; I_D = 0$	$-I_{GSO}$	typ.	1	$\text{pA}^2)$
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	typ.	1	$\text{pA}^2)$

**NOTES**

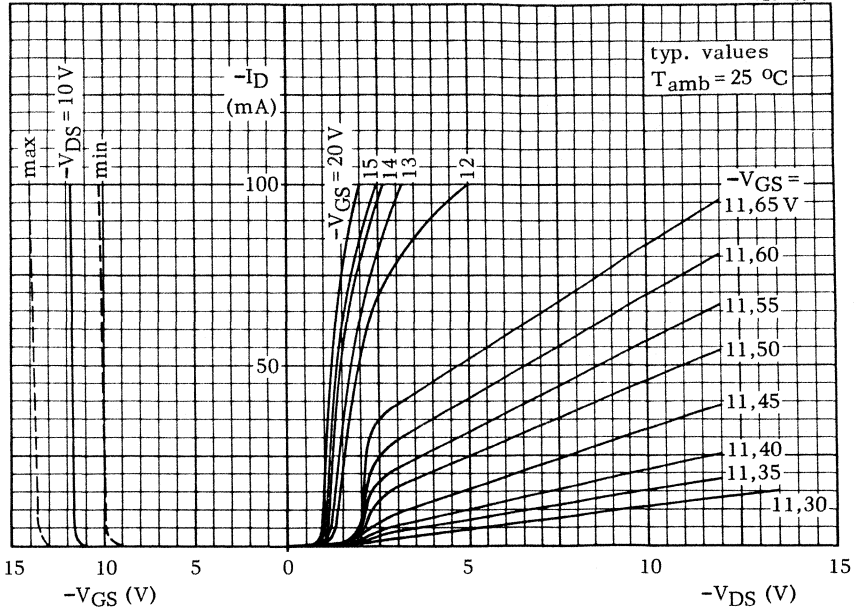
- a. The leads are short-circuited by a clip to protect the oxide layer against damage due to accumulation (or build-up) of electrostatic charge on the high resistance gate electrode. The clip should not be removed until after the device is mounted.
- b. As a service to the customer the  $-V_{GS}$  group to which a device belongs is identified by a numerical suffix (1, 2, 3 or 4), however, individual groups cannot be ordered separately.



- 1. See also upper graph on page 82.
- 2. Being dependent on handling and ambient humidity, the quoted value applies only up to the time of shipping.  
Efficient drying treatment is advised before the device is mounted, provided the application requires this low current.



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## INTEGRATED AM/FM RADIO RECEIVER CIRCUIT

The TBA570A is for use in small low-cost a.m. portable receivers as well as in high-quality battery or mains-fed a.m. and a.m./f.m. receivers. The IC incorporates: a.m. mixer, oscillator, i.f. amplifier, a.g.c. amplifier, a.m. detector and capacitor, f.m./i.f. limiting amplifier and stable base bias for f.m. front-end, and an audio preamplifier and driver.

The unique integrated audio part has an internally limited bandwidth (18 kHz) and negligible h.f. radiation back to the ferrite rod. This makes the TBA570A ideally suitable for small size a.m. receivers because print layout is not critical. The driver stage can directly drive complementary output stages ( $P_o = 6\text{ W max.}$ ), or operate as a post amplifier ( $V_o = 500\text{ mV}$ ).

In its standard applications, the TBA570A can replace the TBA570.

### QUICK REFERENCE DATA

Applicable supply voltage range of receiver	$V_S$	2,7 to 18 V
Supply voltage range (pin 8)	$V_P$	3,6* to 5,4 V
-----		
Ambient temperature	$T_{amb}$	25 °C
Supply voltage (pin 8)	$V_P$	nom. 5,4 V
Total quiescent current except output stages, driver stage TR30 and f.m. front-end	$I_{tot}$	typ. 9 mA
<b>A.M. performance (at pin 2)</b>		
Sensitivity ( $V_o$ at pin 5; $V_i$ at pin 2) for $V_o = 30\text{ mV}$ range 1**	$V_i$	3,0 to 12 $\mu\text{V}$
range 2**	$V_i$	5,5 to 12 $\mu\text{V}$
R.F. input voltage for S/N = 26 dB for $P_o = 50\text{ mW}$ (adjustable)	$V_i$	typ. 18 $\mu\text{V}$
	$V_i$	typ. 2 $\mu\text{V}$
A.G.C. range; change of r.f. input voltage for 10 dB expansion in audio range		typ. 65 dB
R.F. signal handling; $d_{tot} = 10\%$ ; $m = 0,8$		typ. 150 mV
<b>F.M. performance (at pin 2)</b>		
R.F. input voltage; 3 dB before limiting	$V_i$	typ. 50 $\mu\text{V}$
<b>Audio performance</b>		
Output driver current (peak value)	$I_{11M}$	< 100 mA
Input impedance (at pin 12)	$ Z_{12-16} $	typ. 100 k $\Omega$

\* Minimum supply voltage for guaranteed oscillator operation:  $V_P = 2,5\text{ V}$ .

\*\* There are two ranges of sensitivity measured, and indicated by either '1' or '2' on the package. Ordering a specific range is not possible.

### PACKAGE OUTLINES

TBA570A: 16-lead DIL; plastic (SOT-38).

TBA570AQ: 16-lead QIL; plastic (SOT-58).

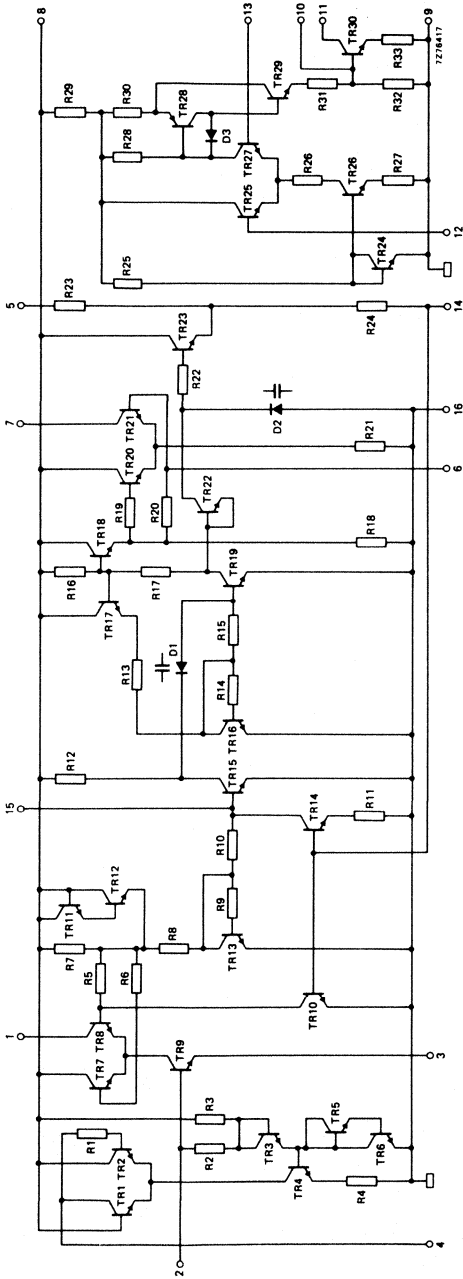


Fig. 1 Circuit diagram.

## D.C. VOLUME AND BALANCE STEREO CONTROL CIRCUIT

The TCA730A is a monolithic integrated circuit for controlling volume and balance in stereo amplifiers by means of a d.c. voltage.

Features:

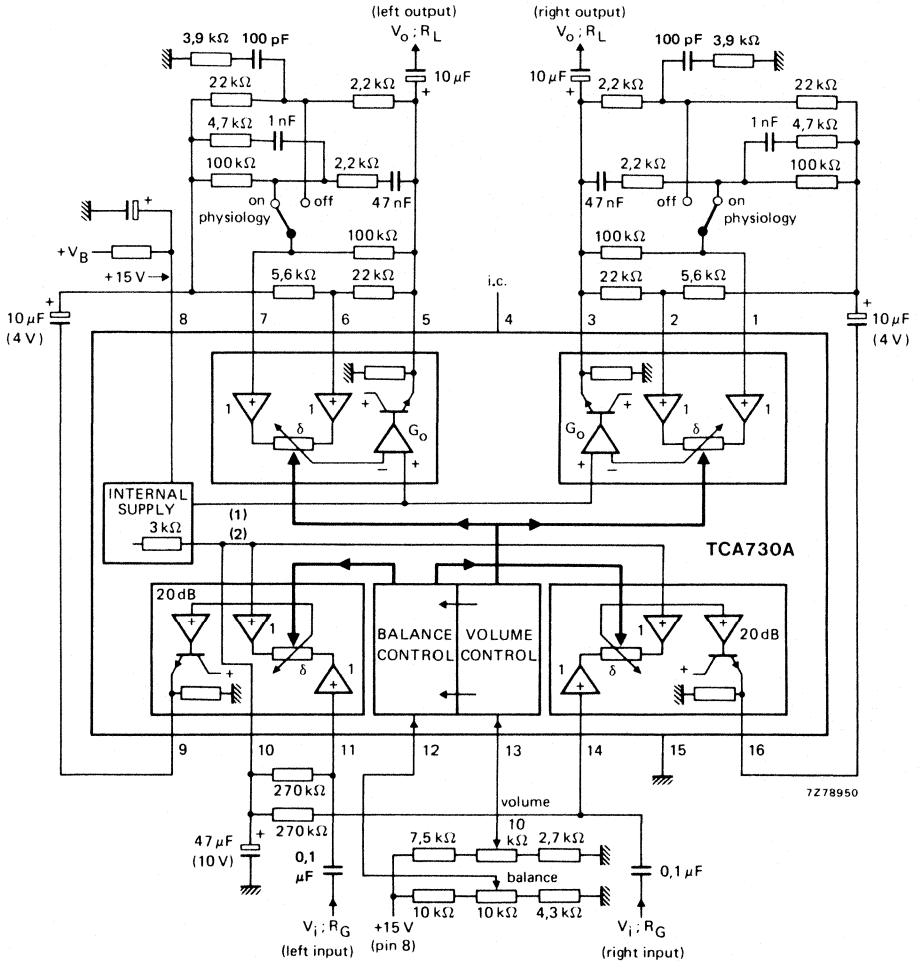
- physiological volume control
- balance control
- internal amplifier
- high-ohmic signals inputs
- internal supply voltage stabilization
- converter for the control voltage

## QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P$	typ. 15 V
Supply current (pin 8)	$I_P$	typ. 35 mA
Input voltage range (r.m.s. value)	$V_{i(rms)}$	0,1 to 1,7 V
Nominal input voltage; $m = 1$ (r.m.s. value)	$V_{i(rms)}$	typ. 0,5 V
Input resistance	$R_i$	typ. 250 k $\Omega$
Output voltage at nominal output power (r.m.s. value)	$V_{O(rms)}$	typ. 1 V
Volume control range	$G_V$	+20 to -80 dB
Channel balance	$\Delta G_V$	typ. 1 dB
Balance control range	$G_V$	+5 to -7 dB
Total distortion at $V_{O(rms)} = 1$ V	$d_{tot}$	typ. 0,1 %
Channel separation	$\alpha$	typ. 55 dB
Signal-to-noise ratio	S/N	typ. 67 dB
Frequency response (-1 dB)		20 Hz to 20 kHz
Volume control voltage range	$V_{13-15}$	2 to 9,5 V
Balance control voltage range	$V_{12-15}$	2,5 to 9,0 V
Supply voltage range (pin 8)	$V_P$	13,5 to 16,5 V
Ambient temperature range	$T_{amb}$	-30 to +80 $^{\circ}C$

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



- (1)  $6,6 V_{BE}; V_1 = 4,6 V$
- (2)  $0,35 V_P + 0,65 V_{BE}; V_2 = 5,7 V.$

Fig. 1 Block diagram with external circuitry.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_p$	max. 18 V
Input voltages	$V_{11-15}; V_{14-15}$	min. 0 V
		max. $V_p$ V
Control voltages	$V_{12-15}; V_{13-15}$	min. -5 V
		max. 12 V
Total power dissipation	$P_{tot}$	max. 900 mW
Storage temperature range	$T_{stg}$	-55 to +150 °C
Operating ambient temperature range	$T_{amb}$	-30 to +80 °C

**CHARACTERISTICS**

$V_p = 15$  V;  $T_{amb} = 25$  °C; measured in Fig. 1; balance control in mid-position ( $V_{12-10} = 0$ ); physiology switch off;  $f = 1$  kHz;  $R_G = 22$  k $\Omega$ ;  $R_L = 5,6$  k $\Omega$ ; unless otherwise specified.

Supply voltage range (pin 8)	$V_p$	13,5 to 16,5 V
Supply current	$I_p$	typ. 35 mA 25 to 43 mA

**Control range**

Voltage gain range	$G_v$	0 to 20 dB
Voltage gain at $V_{13-15} = 9,5$ V (0,63 $V_p$ )	$G_v$	typ. 20 dB
		18 to 22 dB
Voltage attenuation range	$G_v$	0 to -80 dB
		> -75 dB
Voltage attenuation at $V_{13-15} = 3$ V (0,2 $V_p$ )	$G_v$	typ. -80 dB
		+5 to -7 dB
Balance control range at $G_v = -10$ dB		

**Control inputs**

Recommended control voltage range			
	balance	$V_{12-15}$	2,5 to 9,0 V
Control voltage for $G_v = -10$ dB; $V_{12-10} = 0$		$V_{13-15}$	6,7 to 7,1 V*
Control voltage for balance 0 dB; $V_{13-15} = 6,9$ V		$V_{12-10}$	typ. $0 \pm 0,2$ V
Internal supply voltage (0,35 $V_p + 0,65 V_{BE}$ )		$V_{10-15}$	typ. 5,9 V
			5,7 to 6,1 V
Output resistance (pin 10)	$R_{o10}$	typ. 3 k $\Omega$	
Control current		$I_{13}$	typ. 15 $\mu$ A
			< 50 $\mu$ A
balance ( $V_{12-15} = 5,9$ V)		$I_{12}$	typ. 8 $\mu$ A
			< 25 $\mu$ A
Input resistance		$R_{i13}$	typ. 500 k $\Omega$
			$R_{i12}$

\* Typical value 6,9 V.

## CHARACTERISTICS (continued)

## Signal processing

Frequency response (-1 dB)	f	20 Hz to 20 kHz
Input resistance; $R_{11-10} = R_{14-10} = 270 \text{ k}\Omega$ (pins 11; 14)	$R_{i11;14}$	typ. 250 $\text{k}\Omega$
Output resistance (pins 3; 5)	$R_{o3;5}$	typ. 10 $\Omega$
Maximum input voltage; $V_{o(rms)} < 1 \text{ V}$ ; $d_{tot} = 0,7\%$ (r.m.s. value)	$V_{i(rms)}$	$> 1,3 \text{ V}$ typ. 1,7 V
Maximum output voltage; $V_{i(rms)} < 1 \text{ V}$ ; $d_{tot} = 0,7\%$ (r.m.s. value)	$V_{o(rms)}$	$> 1,8 \text{ V}$ typ. 2,0 V
Nominal input voltage; $m = 1$ (r.m.s. value)	$V_{i(rms)}$	typ. 0,5 V
Nominal output voltage at nominal output power (r.m.s. value)	$V_{o(rms)}$	typ. 1 V
Total distortion		
$V_{o(rms)} = 1 \text{ V}$ ; $G_V = \text{maximum}$	$d_{tot}$	typ. 0,07 % $< 0,2 \%$
$V_{o(rms)} = 1 \text{ V}$ ; $V_{i(rms)} = 1 \text{ V}$	$d_{tot}$	typ. 0,2 %
$V_{o(rms)} = 50 \text{ mV}$ ; $V_{i(rms)} = 150 \text{ mV}$	$d_{tot}$	typ. 0,03 % $< 0,1 \%$
$V_{o(rms)} = 50 \text{ mV}$ ; $V_{i(rms)} = 1 \text{ V}$	$d_{tot}$	typ. 0,2 %
Output noise voltage; $f = 20 \text{ Hz to } 20 \text{ kHz}$ signal plus noise voltage (r.m.s. value)		
$G_V = -60 \text{ dB}$	$V_{no(rms)}$	typ. 6 $\mu\text{V}$
$G_V = -10 \text{ dB}$	$V_{no(rms)}$	typ. 15 $\mu\text{V}$
$G_V = \text{maximum (+20 dB)}$	$V_{no(rms)}$	typ. 100 $\mu\text{V}$
noise voltage; weighted conform DIN45405 (peak value)		
$G_V = -60 \text{ dB}$	$V_{no(m)}$	typ. 15 $\mu\text{V}$
$G_V = -10 \text{ dB}$	$V_{no(m)}$	typ. 35 $\mu\text{V}$ $< 80 \mu\text{V}$
$G_V = \text{maximum (+20 dB)}$	$V_{no(m)}$	typ. 230 $\mu\text{V}$ $< 350 \mu\text{V}$
Channel separation; $G_V = \pm 20 \text{ dB}$ ; $V_i = V_o < 1 \text{ V}$		
$f = 250 \text{ Hz to } 12,5 \text{ kHz}$	$\alpha$	$> 52 \text{ dB}$ typ. 53 dB
$f = 40 \text{ Hz to } 16 \text{ kHz}$	$\alpha$	$> 46 \text{ dB}$ typ. 50 dB
Channel balance		
$G_V = +15 \text{ to } -50 \text{ dB}$	$\Delta G_V$	typ. 1 dB $< 2 \text{ dB}$
$G_V < 50 \text{ dB}$	$\Delta G_V$	typ. 2 dB

**Amplifier characteristics**

Input resistance (pins 11 and 14)	$R_{i11;14}$	>	3 M $\Omega$
D.C. output voltages (0,35 V <sub>P</sub> - 1,35 V <sub>BE</sub> )	V <sub>3-15</sub> ; V <sub>16-15</sub>	typ.	4,2 V
(6,6 V <sub>BE</sub> )	V <sub>3-15</sub> ; V <sub>16-15</sub>	typ.	4,6 V
Quiescent input currents (pins 1,2,6,7,11,14)	I <sub>1</sub> ; I <sub>2</sub> ; I <sub>6</sub> ; I <sub>7</sub> ; I <sub>11</sub> ; I <sub>14</sub>	typ.	0,5 $\mu$ A
		<	2 $\mu$ A
Input resistance (pins 1,2,6 and 7) of physiology; without external circuitry	$R_{i1;2;6;7}$	>	1 M $\Omega$
Internal load resistance at outputs (pins 3,5,9,16)	R <sub>3-15</sub> ; R <sub>5-15</sub> ; R <sub>9-15</sub> ; R <sub>10-15</sub>	typ.	2 k $\Omega$
Maximum gain; no load	G <sub>3-1</sub> ; G <sub>3-2</sub> ; G <sub>5-6</sub> ; G <sub>5-7</sub>	>	40 dB
		typ.	43 dB

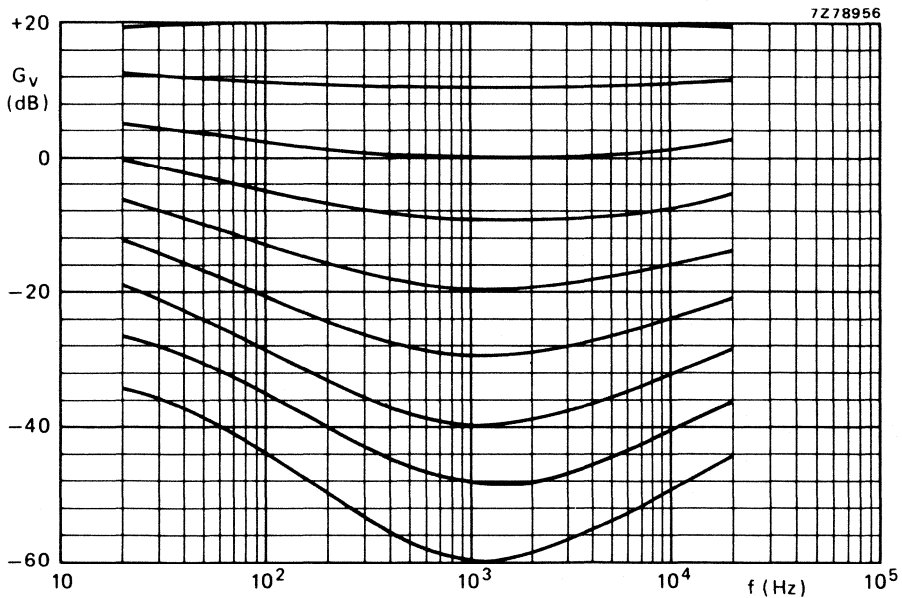


Fig. 2 Frequency response volume control with physiology.

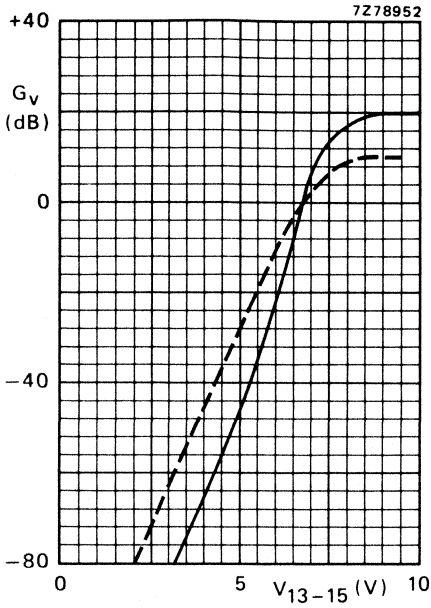


Fig. 3 Volume control curves; without physiology; balance = 0;  $V_{12-10} = 0$ .

—  $G_{v \text{ tot}}$ ;  $G_{v \text{ 5-11}}$ ;  $G_{v \text{ 3-14}}$   
 - - -  $G_{v \text{ 9-11}}$ ;  $G_{v \text{ 16-14}}$

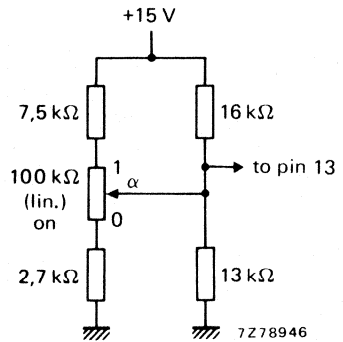
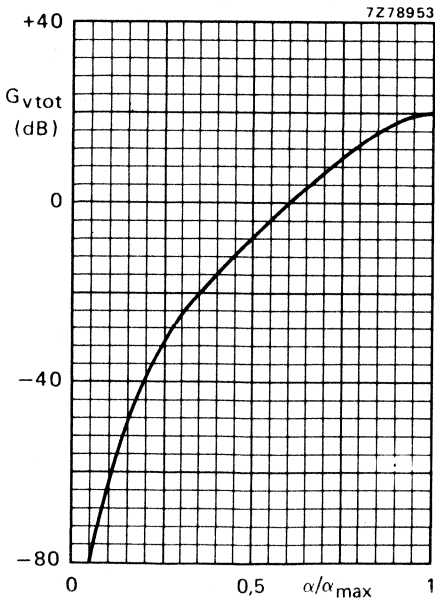


Fig. 4 Volume adjustment curve; balance = 0;  $V_{12-10} = 0$ .

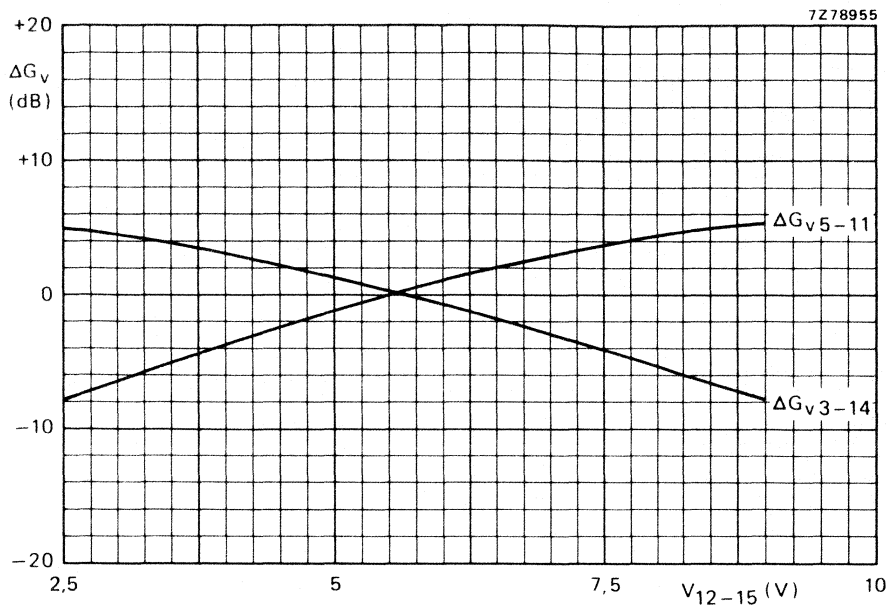


Fig. 5 Balance control curves;  $G_{v\text{tot}} = -10$  dB ( $V_{13-15} = 6,9$  V); for balance = 0.

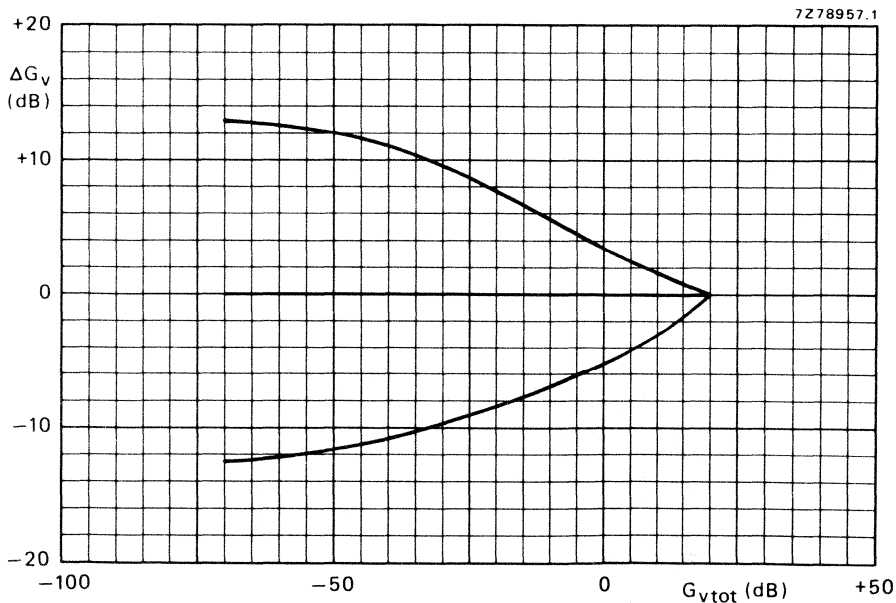
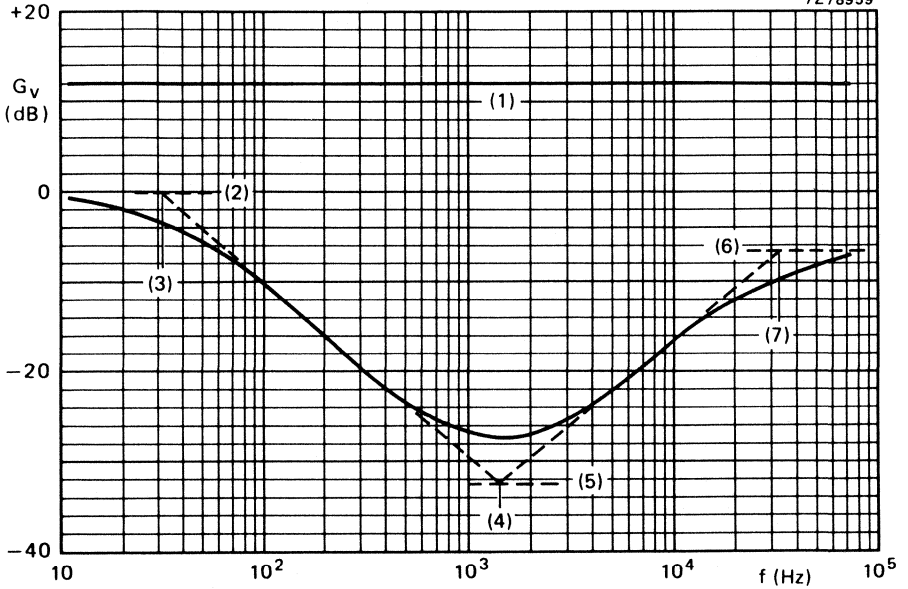


Fig. 6 Balance control range;  $V_{12-15} = 2,5$  to  $9,0$  V.



- (1)  $G_v = R_2/R_1$
- (2)  $G_v = R_{42}/R_{31}$
- (3)  $G_v = 1/2\pi \cdot R_{42} \cdot C_{42}$
- (4)  $G_v = 1/2\pi \cdot R_{41} \cdot C_{31} = 1/2\pi \cdot R_{31} \cdot C_{31}$
- (5)  $G_v \approx R_{41}/R_{32}$
- (6)  $G_v \approx R_{41}/R_{32}$
- (7)  $G_v = 1/2\pi \cdot R_{32} \cdot C_{31}$

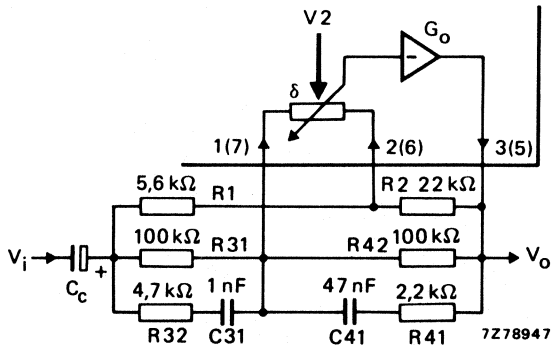


Fig. 7 Frequency response of the physiology part.

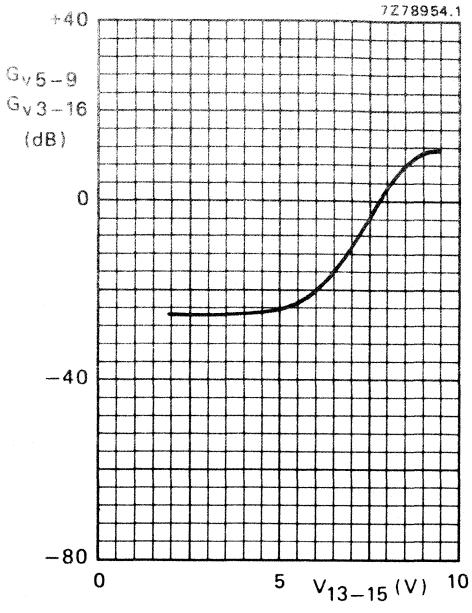


Fig. 8 Physiology control curve; f = 1 kHz; balance = 0; V<sub>12.15</sub> = 0.



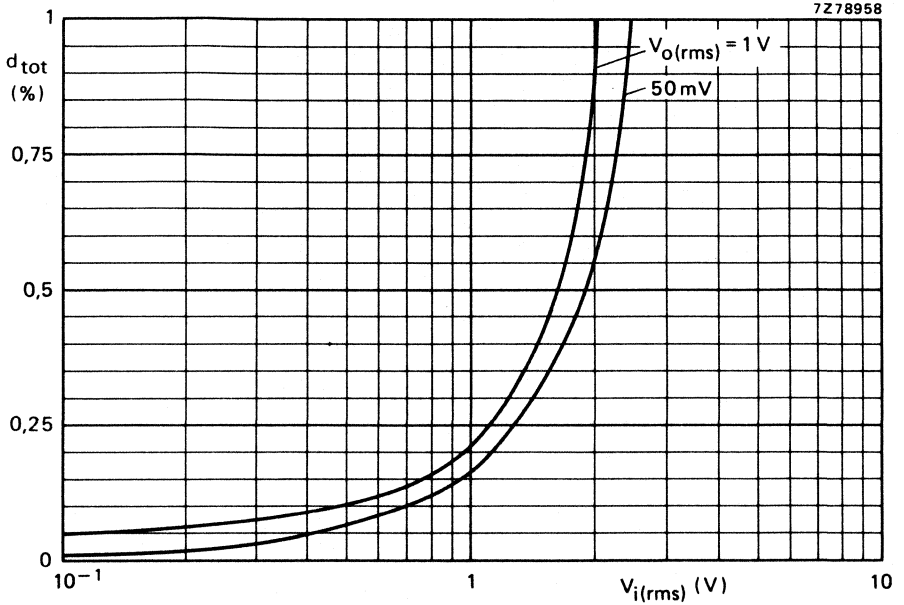


Fig. 9 Total distortion as a function of r.m.s. input voltage;  $f = 1\text{ kHz}$ ;  $R_L = 5,6\text{ k}\Omega$ .

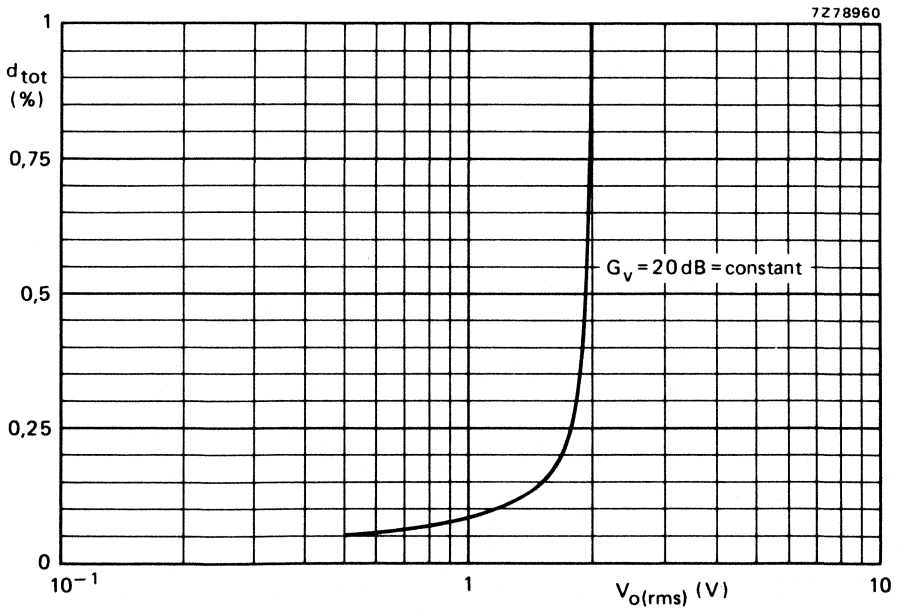


Fig. 10 Total distortion as a function of r.m.s. output voltage;  $f = 1\text{ kHz}$ ;  $R_L = 5,6\text{ k}\Omega$ .



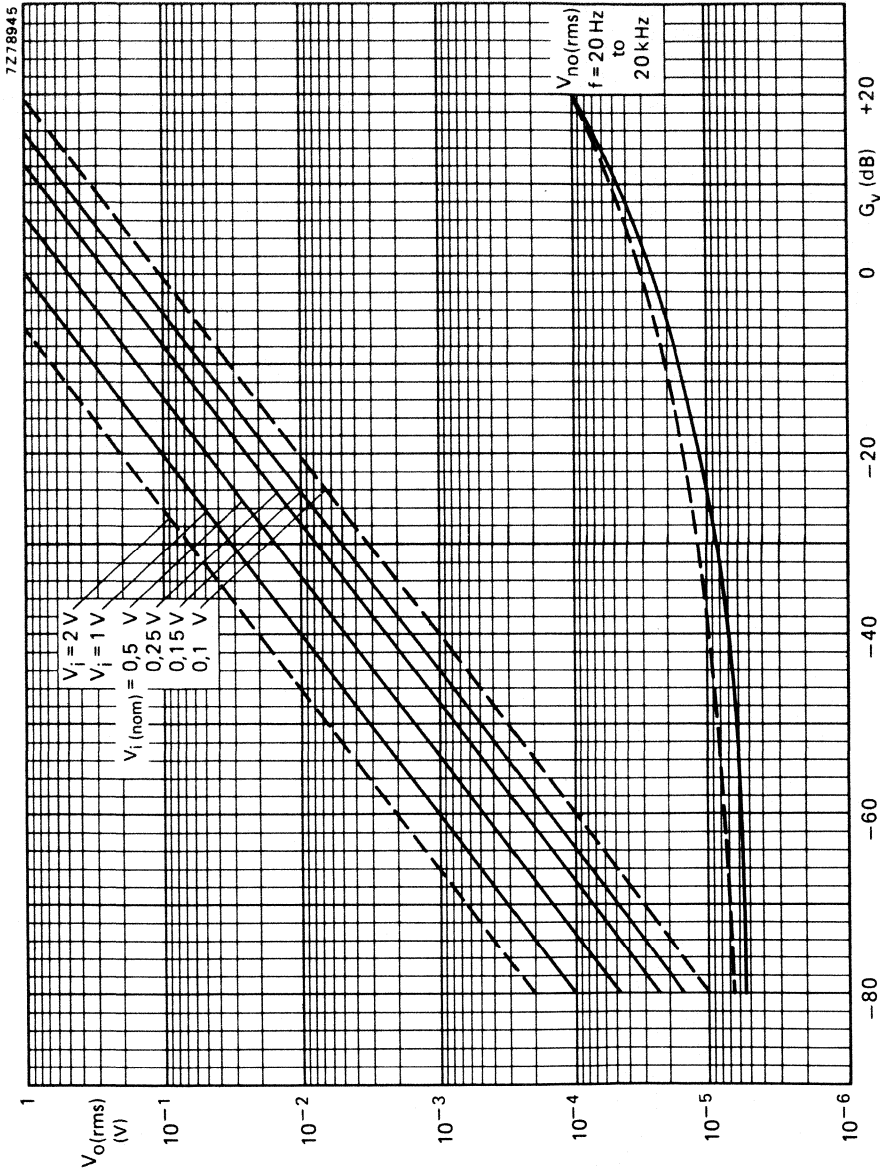
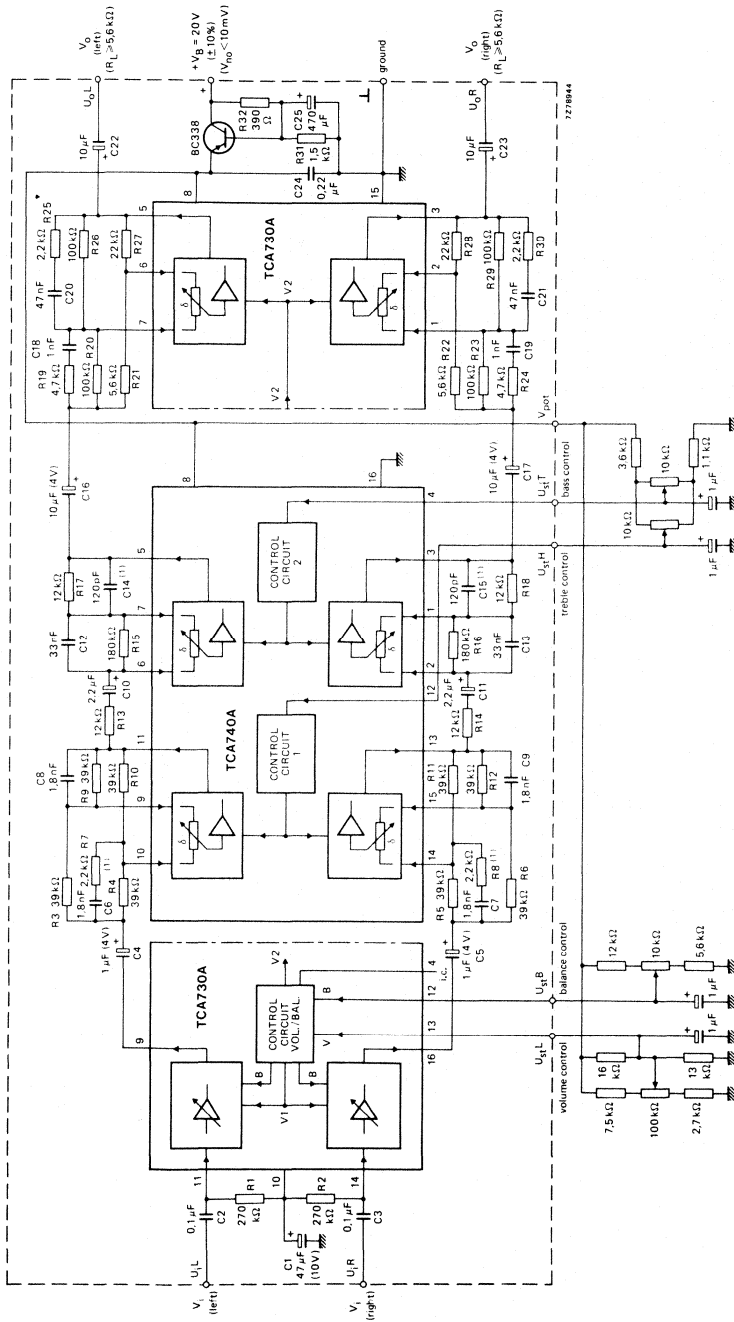


Fig. 11 The r.m.s. output voltage as a function of voltage gain;  $P_o(\text{nom})$  relative to  $V_o(\text{rms}) = 1\text{ V}$ .  
 — without physiological volume control; - - - with physiological volume control.

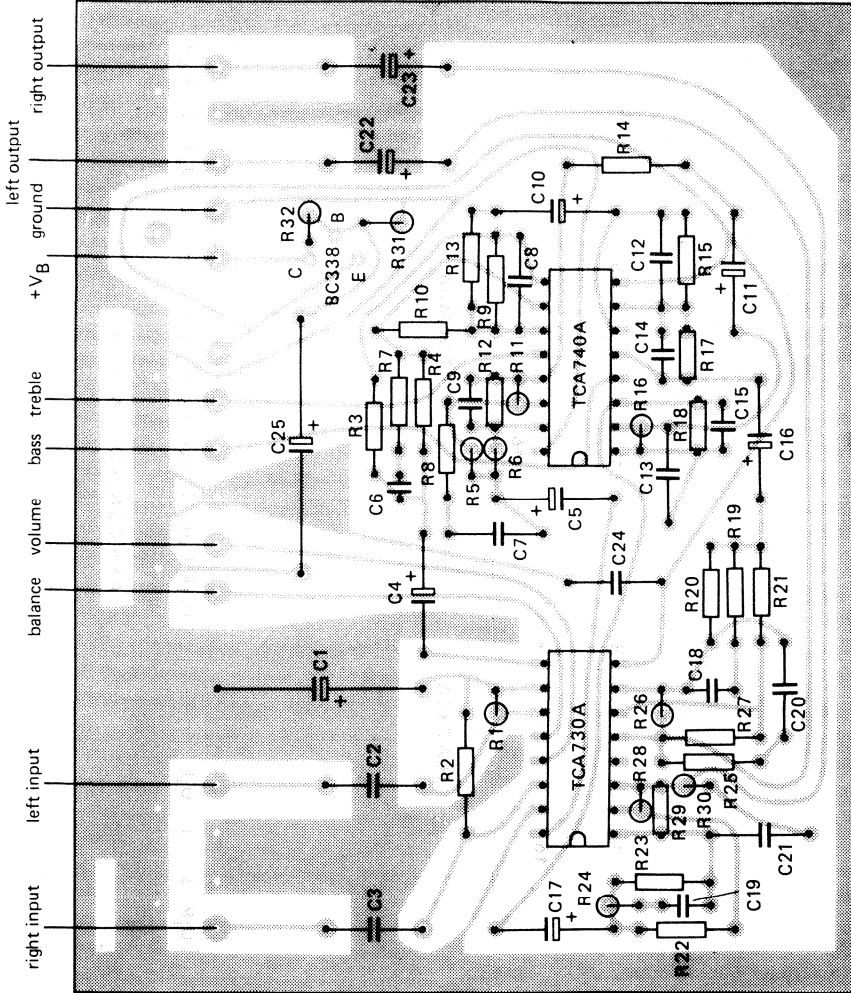


APPLICATION INFORMATION



(1) RC network for limiting treble boost (linear:  $f_{-3\text{dB}} = 100\text{ kHz}$ ).

Fig. 12 Application diagram for TCA730A and TCA740A. For printed-circuit board see Fig. 13.

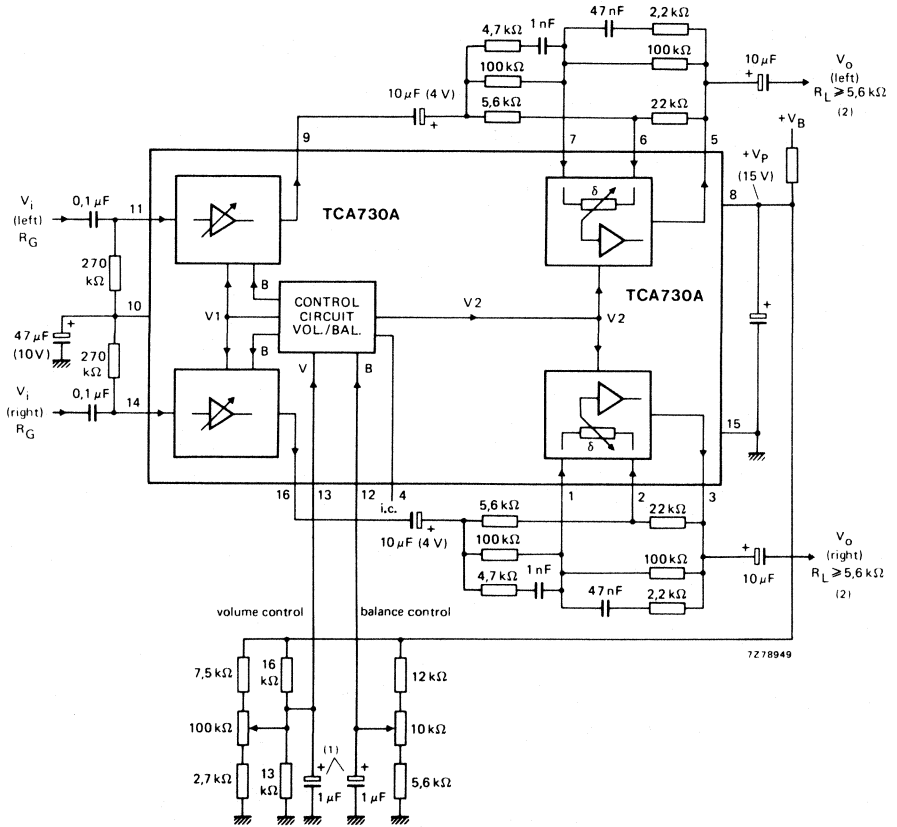


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Fig. 13 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 12.



APPLICATION INFORMATION (continued)



- (1) C<sub>13-15</sub> = C<sub>12-15</sub> = 1 μF are intended for suppression of the noise when adjusting the mechanical potentiometers.
- (2) For rejecting noise, caused by switching on or off, corresponding muting switches can be used before or in the output power stage.

Fig. 14 Application example of TCA730A used for volume and balance control.

## D.C. TREBLE AND BASS STEREO CONTROL CIRCUIT

The TCA740A is a monolithic integrated circuit for controlling treble and bass in stereo amplifiers by means of a d.c. voltage.

**Features:**

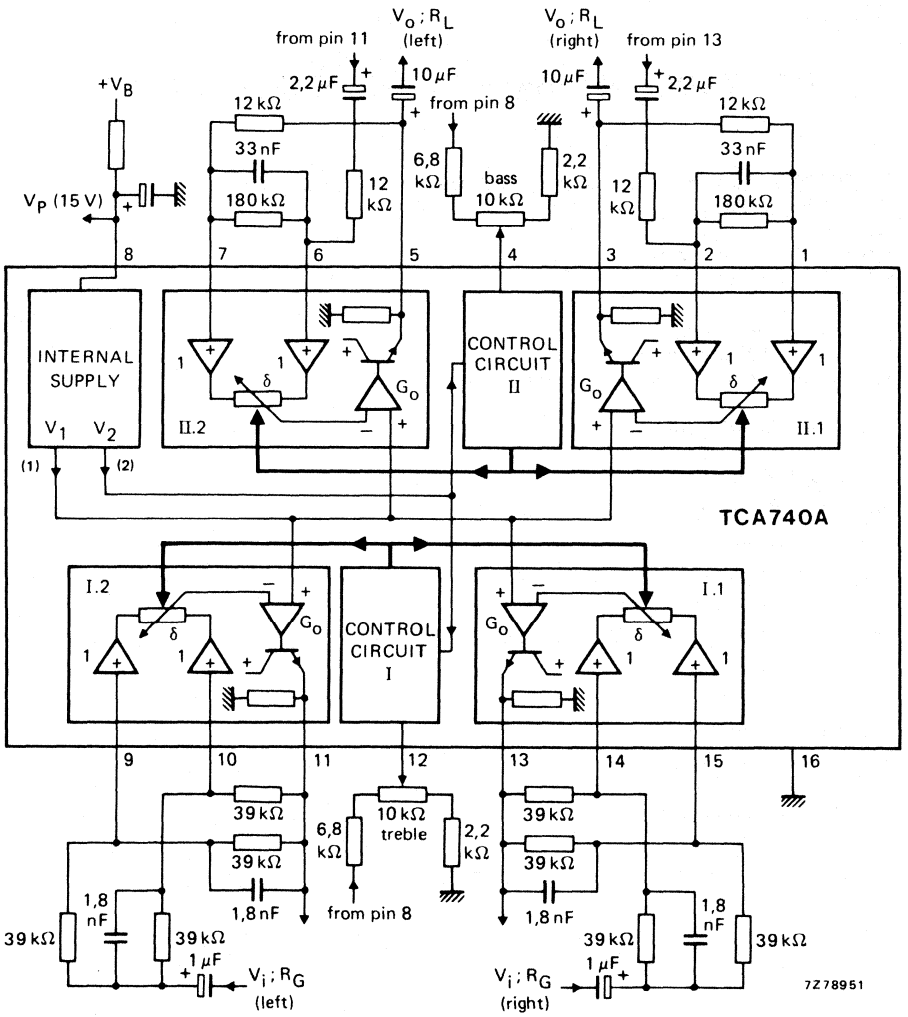
- two double potentiometer circuits
- feedback control
- internal amplifier
- high-ohmic signal inputs
- converter for the control voltages
- low-ohmic and short-circuit protected signal outputs

### QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_p$	typ.	15 V
Supply current (pin 8)	$I_p$	typ.	35 mA
Bass boost and cut at 40 Hz (ref. 1 kHz)		typ.	$\pm 16$ dB
Treble boost and cut at 16 kHz (ref. 1 kHz)		typ.	$\pm 16$ dB
Input/output voltage at $d_{tot} = 0,7\%$ (r.m.s. value)	$V_{i,o(rms)}$	typ.	2 V
Total distortion at $V_{o(rms)} = 1$ V; linear frequency response	$d_{tot}$	typ.	0,1 %
Channel separation	$\alpha$	typ.	70 dB
Output signal plus noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	45 $\mu$ V
Frequency response (-1 dB)	f		20 Hz to 20 kHz
Treble/bass control voltage range	$V_{12-16}; V_{4-16}$		1,8 to 9,5 V
-----			
Supply voltage range (pin 8)	$V_p$		13,5 to 16,5 V
Ambient temperature range	$T_{amb}$		-30 to + 80 °C

### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



- (1)  $6,6 V_{BE}; V_1 = 4,6 V$
- (2)  $0,31 V_p + 1,4 V_{BE}; V_2 = 5,6 V$

Fig. 1 Block diagram with external circuitry.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_p$	max.	18 V
Control voltages (pins 4 and 12)	$V_{4-16}$	max.	12 V
	$-V_{4-16}$	max.	5 V
	$V_{12-16}$	max.	12 V
	$-V_{12-16}$	max.	5 V
Total power dissipation	$P_{tot}$	max.	900 mW
Storage temperature range	$T_{stg}$		-55 to +150 °C
Operating ambient temperature range	$T_{amb}$		-30 to +80 °C

## CHARACTERISTICS

 $V_p = 15$  V;  $T_{amb} = 25$  °C; measured in Fig. 1; in position 'linear' ( $V_{4-16} = V_{12-16} = 5,6$  V); $R_G = 60$   $\Omega$ ;  $R_L = 5,6$  k $\Omega$ ;  $f = 1$  kHz; unless otherwise specified

Supply voltage range (pin 8)	$V_p$		13,5 to 16,5 V
Supply current (pin 8)	$I_p$	typ.	34 mA 25 to 45 mA

## Signal processing

Voltage gain at linear frequency response	$G_v$	typ.	0 dB
Frequency response (-1 dB)	$f$		20 Hz to 20 kHz
Maximum gain variation at $f = 1$ kHz at maximum bass/treble boost or cut	$\Delta G_v$	<	$\pm 1,5$ dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{4-16} = 9,2$ V		>	15 dB typ. 16 dB
Bass cut at 40 Hz (ref. 1 kHz) $V_{4-16} = 2$ V		>	15 dB typ. 16 dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{12-16} = 9,2$ V		>	15 dB typ. 16 dB
Treble cut at 16 kHz (ref. 1 kHz) $V_{12-16} = 2$ V		>	15 dB typ. 16 dB
Total distortion			
$V_{o(rms)} = 100$ mV; $f = 1$ kHz	$d_{tot}$	typ.	0,03 %
$V_{o(rms)} = 100$ mV; $f = 40$ Hz to 16 kHz	$d_{tot}$	typ.	0,1 %
$V_{o(rms)} = 1$ V; $f = 1$ kHz	$d_{tot}$	typ.	0,07 %
$V_{o(rms)} = 1$ V; $f = 40$ Hz to 16 kHz	$d_{tot}$	<	0,2 % typ. 0,2 %
Input/output voltage at $d_{tot} = 0,7$ % (r.m.s. value)	$V_i(rms) = V_o(rms)$	>	1,6 V typ. 2 V
Output signal plus noise voltage (r.m.s. value) $f = 20$ Hz to 20 kHz	$V_{no(rms)}$	typ.	40 $\mu$ V
Output noise voltage; weighted conform DIN45405; peak value	$V_{no(m)}$	typ.	90 $\mu$ V < 160 $\mu$ V

**CHARACTERISTICS** (continued)

**Channel separation**

f = 1 kHz	$\alpha$	typ.	72 dB
f = 250 Hz to 12,5 kHz	$\alpha$	typ.	68 dB
f = 40 Hz to 16 kHz	$\alpha$	>	50 dB
		typ.	58 dB

**Control voltages**

Recommended control voltage range  
treble/bass

$V_{4-16} = V_{12-16}$	>	0 V
		2 to 9,2 V
	<	0,66 V <sub>p</sub> V
		typ. 5,6 V

Control voltage at linear frequency response

$V_{4-16} = V_{12-16}$		5,4 to 5,8 V
		(0,31 V <sub>p</sub> to 1,4 V <sub>BE</sub> ) V

Quiescent input current

$V_{4-16} = V_{12-16} = 2$ to 9,2 V	$I_4 = I_{12}$	typ.	6 $\mu$ A
		<	25 $\mu$ A

Input resistance (pins 4 and 12)

$V_{4-16} = V_{12-16} = 5,6$ V	$R_{i4;12}$	typ.	800 k $\Omega$
--------------------------------	-------------	------	----------------

**Amplifier characteristics**

Quiescent input currents;  $V_i = 4,6$  V  
(pins 1, 2, 6, 7, 9, 10, 14 and 15)

$I_{1;2;6;7;9;10;14;15}$	typ.	0,6 $\mu$ A
	<	2 $\mu$ A

Input resistance (pins 1,2,6,7,9,10,14 and 15)

$R_{i1;2;6;7;9;10;14;15}$	>	1 M $\Omega$
---------------------------	---	--------------

Internal emitter resistance at outputs

$R_{3-16}; R_{5-16}; R_{11-16}; R_{13-16}$	typ.	2 k $\Omega$
--	------	--------------

Output resistance (pins 3,5,11 and 13)

$R_{o3;5;11;13-16}$	typ.	10 $\Omega$
---------------------	------	-------------

Maximum gain; no load

$G_v$	>	40 dB
	typ.	43 dB

D.C. output voltages

$V_{4-16} = V_{12-16} = 5,6$ V (pins 3,5,11 and 13)	$V_{3-16}; V_{5-16}; V_{11-16}; V_{13-16}$	typ.	4,6 V
			4,3 to 4,9 V
			(6,6 V <sub>BE</sub> ) V





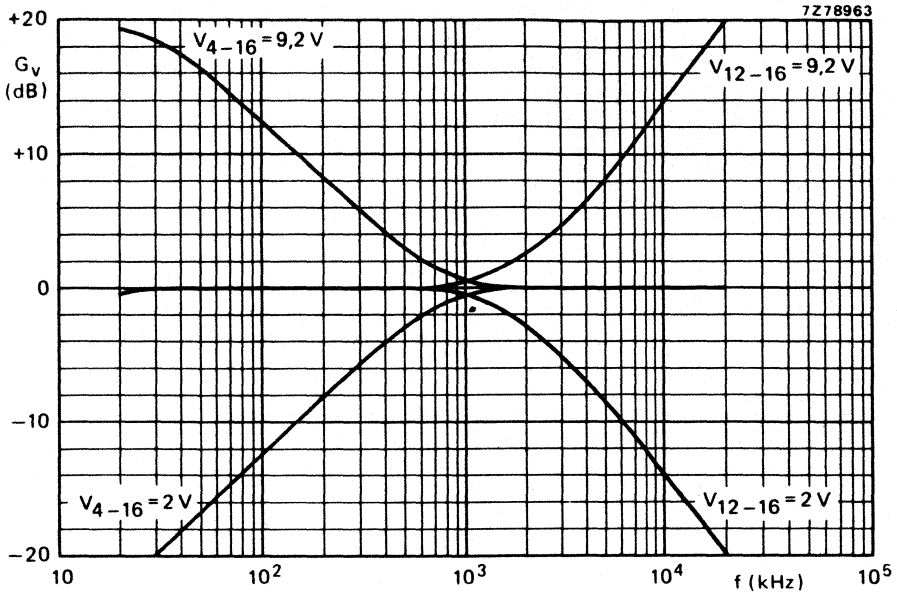


Fig. 2 Frequency response.

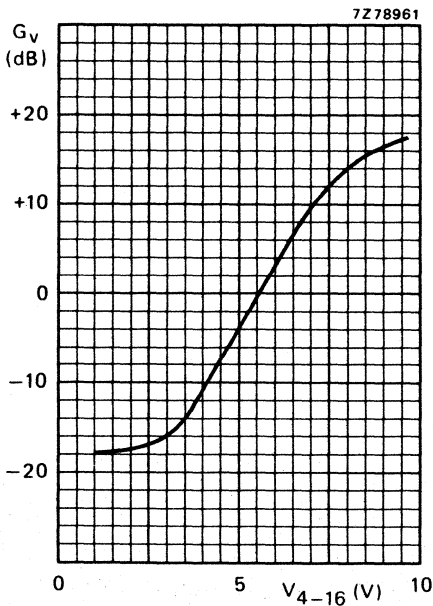


Fig. 3 Bass control curve at  $f = 40\text{ Hz}$ .

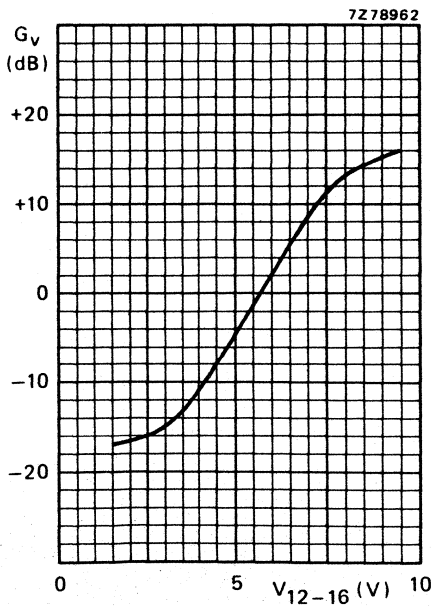


Fig. 4 Treble control curve at  $f = 16\text{ kHz}$ .

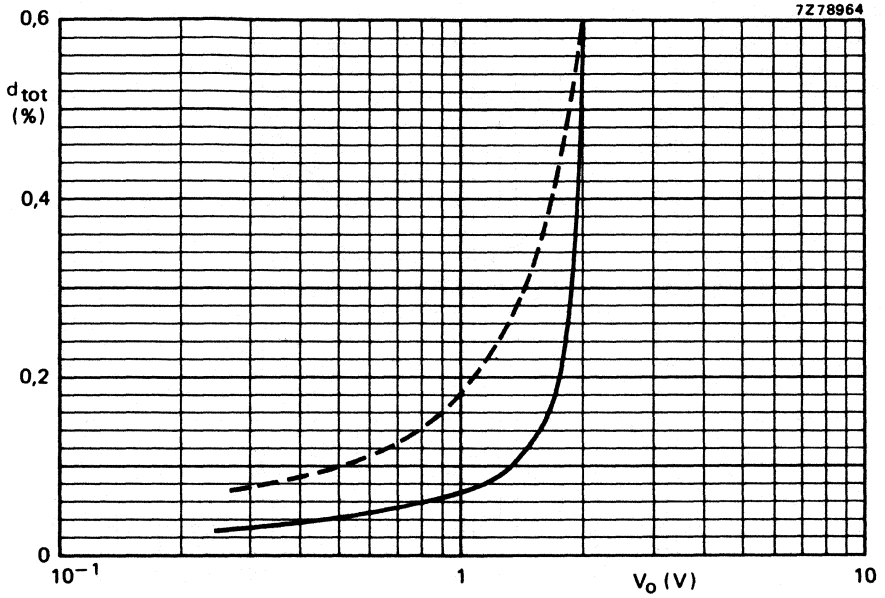
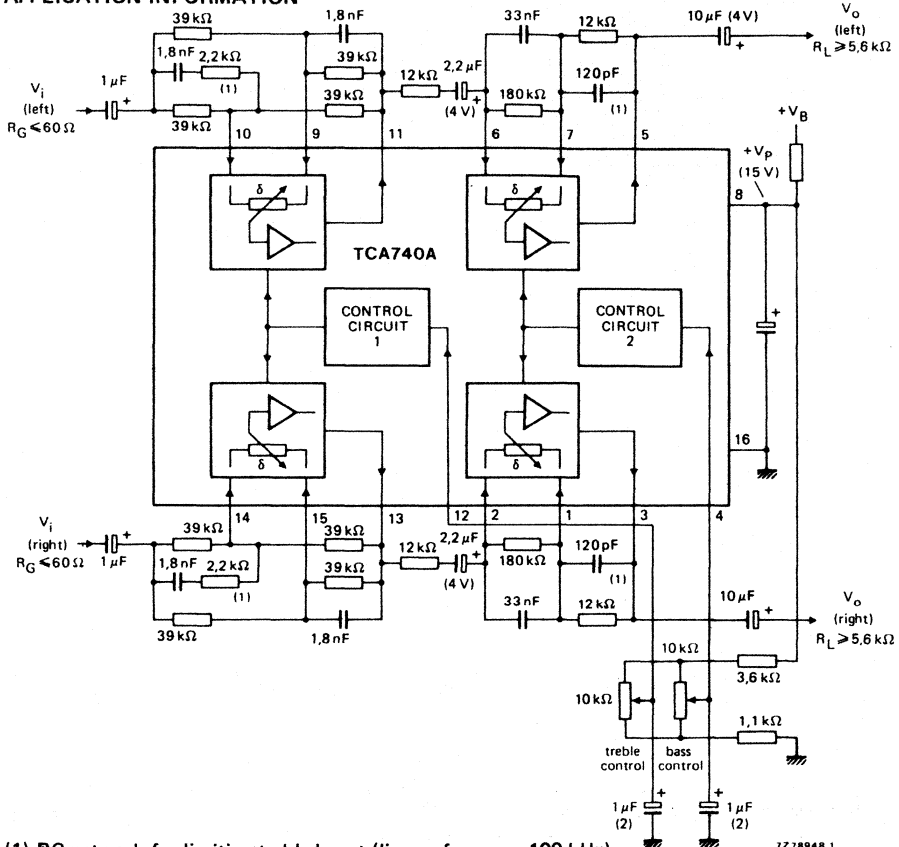


Fig. 5 Total distortion as a function of output voltage;  $V_{4-16} = V_{12-16} = 5,6$  V (linear,  $G_{V\ tot} = 1$ );  
 —  $f = 1$  kHz; ---  $f = 40$  Hz to 16 kHz.

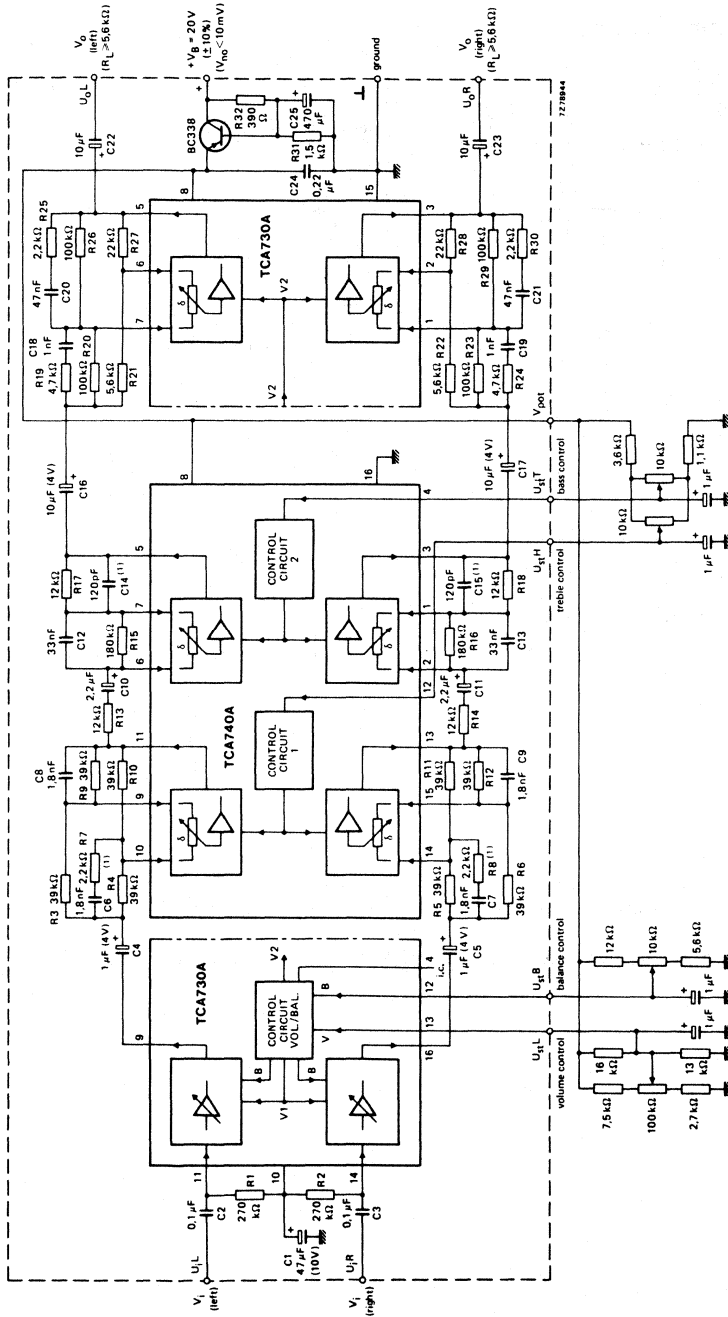


APPLICATION INFORMATION



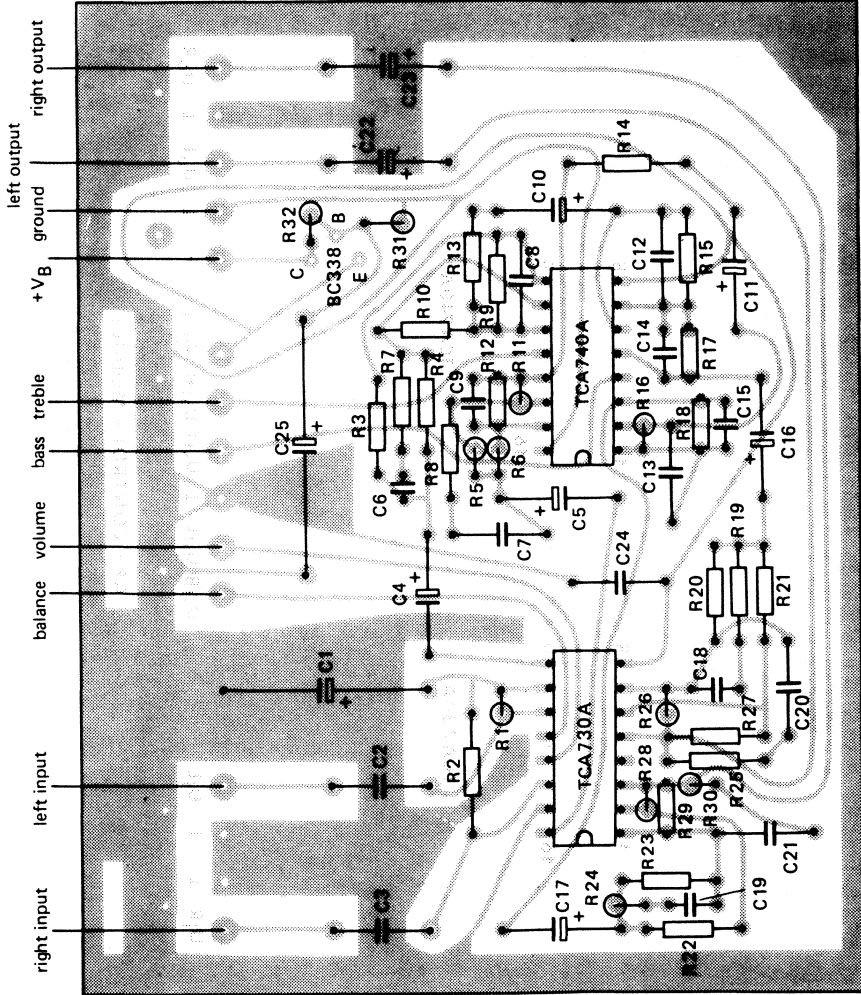
- (1) RC network for limiting treble boost (linear:  $f_{-3 \text{ dB}} = 100 \text{ kHz}$ ).
- (2) Capacitors are intended for suppression of the noise when adjusting the mechanical potentiometers.

Fig. 6 Application example of TCA740A used for treble and bass control.



(1) RC network for limiting treble boost (linear:  $f-3 \text{ dB} = 100 \text{ kHz}$ ).

Fig. 7 Application diagram for TCA730A and TCA740A. For printed-circuit board see Fig. 8.



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Fig. 8 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 7.





## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1001B  
TDA1001BT

# INTERFERENCE AND NOISE SUPPRESSION CIRCUIT FOR FM RECEIVERS

## GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

### Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

## QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_P$	typ.	12 V
Supply current (pin 9)	$I_P$	typ.	14 mA
A.F. input signal handling (pin 1) (peak-to-peak value)	$V_{i(p-p)}$	typ.	1 V
Input resistance (pin 1)	$R_i$	min.	35 k $\Omega$
Voltage gain ( $V_{1-16}/V_{6-16}$ )	$G_V$	typ.	0,5 dB
Total harmonic distortion	THD	typ.	0,25 %
Bandwidth	B	typ.	70 kHz
Suppression pulse threshold voltage (peak value); $R_{13} = 0$	$V_{i(tr)OM}$	typ.	19 mV
Suppression pulse duration	$t_s$	typ.	27 $\mu$ s
Supply voltage range (pin 9)	$V_P$		7,5 to 16 V
Operating ambient temperature range	$T_{amb}$		-30 to +80 $^{\circ}$ C

## PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT-38).

TDA1001BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

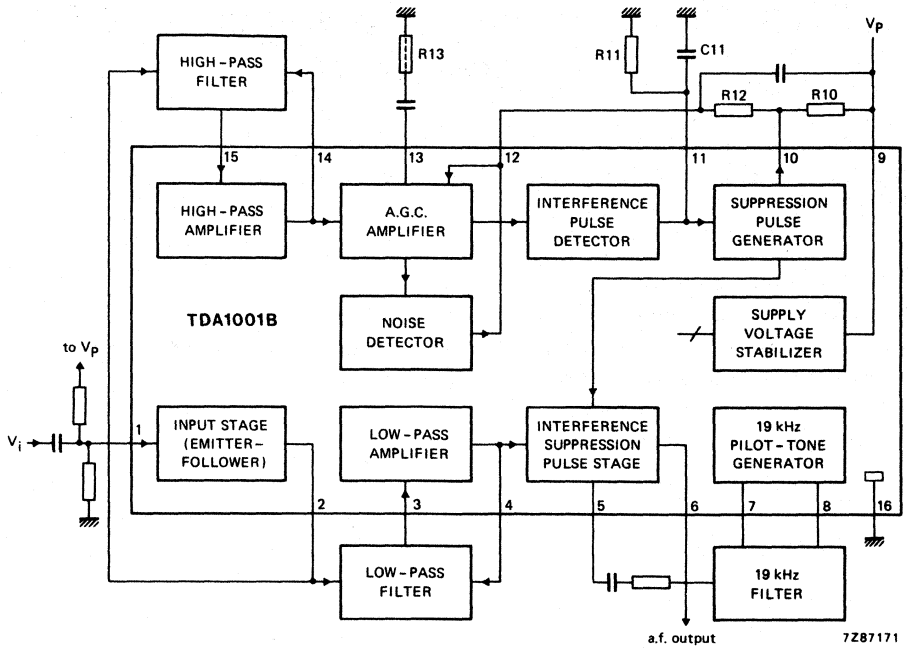


Fig. 1 Block diagram.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_p$	max.	18 V
Input voltage (pin 1)	$V_{1-16}$	max.	$V_p$ V
Output current (pin 6)	$I_6$	max.	1 mA
	$-I_6$	max.	15 mA
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	$T_{stg}$	-65 to +150 °C	
Operating ambient temperature range	$T_{amb}$	-30 to +80 °C	

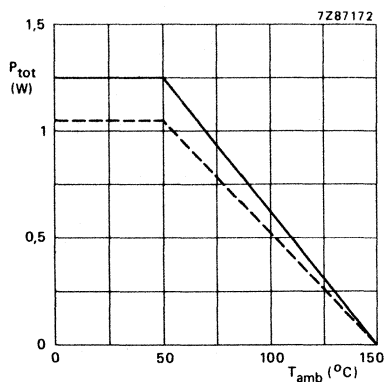


Fig. 2 Power derating curves.

- in plastic DIL (SOT-38) package (TDA1001B)
- - - - - in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.



**CHARACTERISTICS**

$V_p = 12\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Input stage</b>					
Input impedance (pin 1) f = 40 kHz	$ Z_{i1} $	—	45	—	k $\Omega$
Input resistance (pin 1) with pin 2 not connected	$R_{i1}$	—	600	—	k $\Omega$
Input bias current (pin 1) $V_{1-16} = 4,8\text{ V}$	$I_{i1}$	—	6	15	$\mu\text{A}$
Output resistance (pin 2) unloaded	$R_{o2}$	low-ohmic			
Internal emitter resistance	$R_{2-16}$	—	5,6	—	k $\Omega$
<b>Low-pass amplifier</b>					
Input resistance (pin 3)	$R_{i3}$	10	—	—	M $\Omega$
Input bias current (pin 3)	$I_{i3}$	—	—	7	$\mu\text{A}$
Output resistance (pin 4)	$R_{o4}$	—	—	5	$\Omega$
Voltage gain ( $V_4/V_3$ )	$G_{v4/3}$	—	1,1	—	
<b>Suppression pulse stage</b>					
Input offset current at pin 5 during the suppression time $t_s$	$I_{io5}$	—	50	200	nA
<b>Output stage</b>					
Output resistance (pin 6)	$R_{o6}$	low-ohmic			
Internal emitter resistance	$R_{6-16}$	—	6	—	k $\Omega$
Current gain ( $I_5/I_6$ )	$G_{i5/6}$	—	85	—	dB
<b>Pilot tone generation (19 kHz)</b>					
Input impedance (pin 8)	$ Z_{i8} $	—	—	1	$\Omega$
Output impedance (pin 7) pin 8 open	$ Z_{o7} $	150	—	—	k $\Omega$
Output bias current (pin 7)	$I_{o7}$	0,7	1	1,3	mA
Current gain ( $I_7/I_8$ )	$G_{i7/8}$	—	3	—	
<b>High-pass amplifier</b>					
Input resistance (pin 15)	$R_{i15}$	10	—	—	M $\Omega$
Input bias current (pin 15)	$I_{i15}$	—	—	7	$\mu\text{A}$
Output resistance (pin 14)	$R_{o14}$	—	—	5	$\Omega$
Voltage gain ( $V_{14}/V_{15}$ )	$G_{v14/15}$	—	1,4	—	

parameter	symbol	min.	typ.	max.	unit
<b>A.G.C. amplifier; interference and noise detectors</b>					
Internal resistance (pins 13 and 14)	$R_{13-14}$	1,5	2,0	2,5	$k\Omega$
Operational threshold voltage (uncontrolled); peak value (pin 14) of the interference pulse detector	$\pm V_{14int\ m}$	—	15	—	mV
of the noise detector	$\pm V_{14n\ m}$	—	6,5	—	mV
Output voltage (peak value; pin 11)	$V_{11-16M}$	5,2	5,8	6,4	V
Output control current (pin 12) (peak value)	$I_{12M}$	150	200	250	$\mu A$
Output bias current (pin 12)	$I_{o12}$	—	2,5	6	$\mu A$
Input threshold voltage for onset of control (pin 12) ( $V_{i(tr)O} + 3\ dB$ )	$V_{12-9}$ or:	360 —	425 $0,66V_{BE}$	500 —	mV mV
<b>Suppression pulse generation (Schmitt trigger)</b>					
Switching threshold (pin 11)					
1: gate disabled	$V_{11-16}$	—	3,2	—	V
2: gate enabled	$V_{11-16}$	—	2,0	—	V
Switching hysteresis	$\Delta V_{11-16}$	—	1,2	—	V
Input offset current (pin 11)	$I_{io11}$	—	—	100	nA
Output current (pin 10) gate disabled; peak value	$I_{o10M}$	0,6	1	1,4	mA
Reverse output current (pin 10)	$I_{R10}$	—	—	2	$\mu A$
Sensitivity (pin 10)	$V_{10-16}$	2,5	—	—	V



**APPLICATION INFORMATION**

$V_p = 12\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $f = 1\text{ kHz}$ ; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 9)	$V_p$	7,5	12	16	V
Quiescent supply current (pin 9)	$I_p$	10	14	18	mA
<b>Signal path</b>					
D.C. input voltage (pin 1)	$V_{1-16}$	—	4,5	—	V
Input impedance (pin 1); $f = 40\text{ kHz}$	$ Z_{i1} $	35	—	—	$k\Omega$
D.C. output voltage (pin 6)	$V_{6-16}$	2,4	2,8	—	V
Output resistance (pin 6)	$R_{o6}$	low-ohmic			
Voltage gain ( $V_6/V_1$ )	$G_{v6/1}$	0	0,5	1	dB
—3 dB point of low-pass filter	$f_{(-3dB)}$	—	70	—	kHz
Sensitivity for THD < 0,5% (peak-to-peak value)	$V_{i(p-p)}$	1,2	1,8	—	V
Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M} = 100\text{ mV}$ ; (peak-to-peak value)	$V_{6-16(p-p)}$	—	—	3	mV
Interference suppression at $R_{13} = 0$ ; notes 5 and 6; $V_{i(rms)} = 30\text{ mV}$ ; $f = 19\text{ kHz}$ (sinewave); $V_{i(tr)M} = 60\text{ mV}$ ; $f_r = 400\text{ Hz}$	$\alpha_{int}$	20	30	—	dB
<b>Interference processing</b>					
Input signal at pin 1; output signal at pin 10					
Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1 measured with sinewave input signal $f = 120\text{ kHz}$ ; $-V_{10-9} > 1\text{ V}$ at $R_{13} = 0\ \Omega$	$V_{i(tr)rms}$	8	11	14	mV
at $R_{13} = 2,7\text{ k}\Omega$	$V_{i(tr)rms}$	18	28,5	40	mV
voltage difference for safe triggering/ non-triggering (r.m.s. value)	$\Delta V_{i(rms)}$	—	1	—	mV
measured with interference pulses $f = 400\text{ Hz}$ (see Fig. 3); peak value at $R_{13} = 0\ \Omega$	$V_{i(tr)M}$	—	19	—	mV
at $R_{13} = 2,7\text{ k}\Omega$	$V_{i(tr)M}$	—	45	—	mV
Suppression pulse duration (note 2)	$t_s$	24	27	30	$\mu s$



parameters	symbol	min.	typ.	max.	unit
<b>Noise threshold feedback control</b> (notes 1 and 3)					
Noise input voltage (r.m.s. value) f = 120 kHz sinewave					
for $V_{12.g} = 300$ mV at $R_{13} = 0 \Omega$	$V_{ni(rms)}$	2,3	3,3	4,3	mV
at $R_{13} = 2,7$ k $\Omega$	$V_{ni(rms)}$	—	8,2	—	mV
for $V_{12.g} = 425$ mV ( $V_{i(tr)O} + 3$ dB) at $R_{13} = 0 \Omega$	$V_{ni(rms)}$	—	7,3	—	mV
at $R_{13} = 2,7$ k $\Omega$	$V_{ni(rms)}$	—	16,5	—	mV
for $V_{12.g} = 560$ mV ( $V_{i(tr)O} + 20$ dB) at $R_{13} = 0 \Omega$	$V_{ni(rms)}$	33	45	57	mV
at $R_{13} = 2,7$ k $\Omega$	$V_{ni(rms)}$	—	107	—	mV
Amplification control voltage by interference intensity (note 4)					
$V_{i(rms)} = 50$ mV; f = 19 kHz;					
$V_{i(tr)M} = 300$ mV; r.m.s. value					
at repetition frequency $f_r = 1$ kHz	$V_{o6(rms)}$	49	—	56	mV
at repetition frequency $f_r = 16$ kHz	$V_{o6(rms)}$	45	—	65	mV



Notes to application information

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:  
 $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$  in which  $R_S = 2 \text{ k}\Omega$ ;  
 $V_{ni} = (1 + R13/R_S) \times V_{niO}$  in which  $R_S = 2 \text{ k}\Omega$ .
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 k $\Omega$ .
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with R7.16 (and R7.8). Adjustment is not required if components with small tolerances are used e.g.  $\Delta R < 1\%$  and  $\Delta C < 2\%$ .
6. Measuring conditions:  
 The peak output noise voltage ( $V_{no m}$ , CCITT filter) shall be measured at the output with a de-emphasizing time  $T = 50 \mu\text{s}$  ( $R = 5 \text{ k}\Omega$ ,  $C = 10 \text{ nF}$ ); the reference value of 0 dB is  $V_{o int}$  with the 19 kHz generator short-circuited (pin 7 grounded).

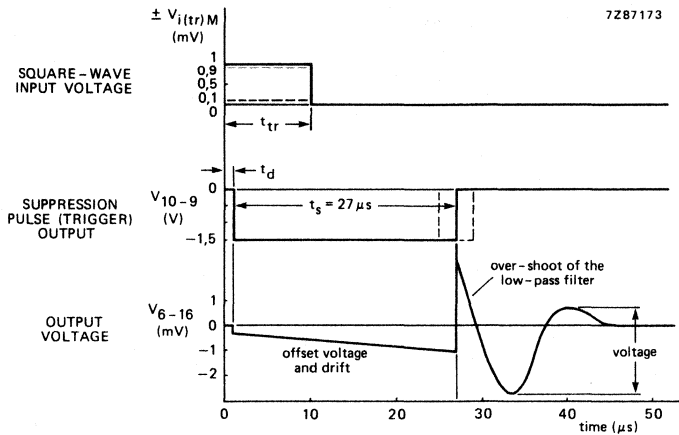


Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of  $t_{tr} = 10 \mu\text{s}$  and with rise and fall times  $t_r = t_f = 10 \text{ ns}$ .

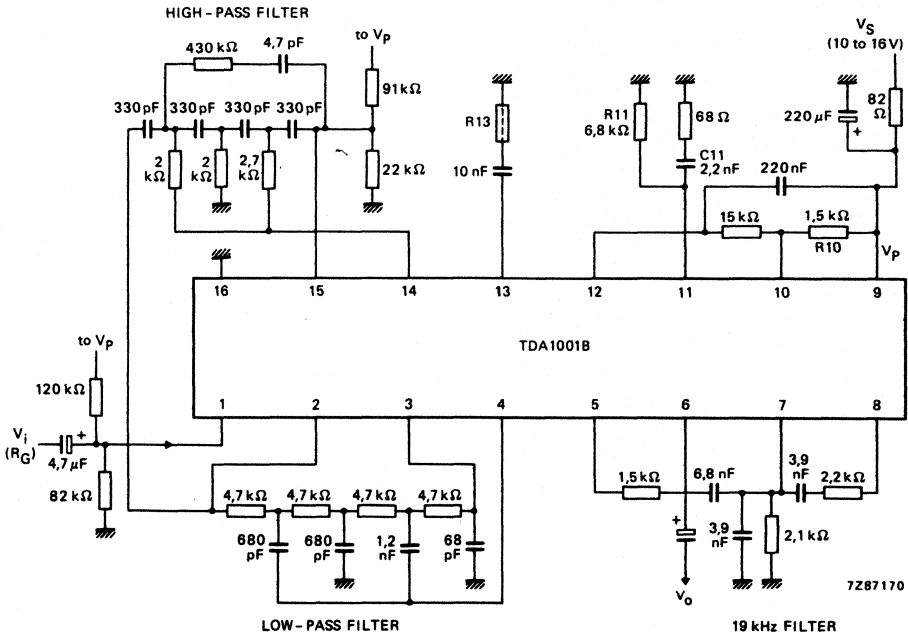


Fig. 4 Application circuit diagram.







## RECORDING AND PLAYBACK AMPLIFIER

This integrated circuit incorporates all amplifier circuits necessary for the record/playback functions, with the exception of the audio power output amplifier. It comprises:

- a preamplifier for microphone or playback,
- a recording amplifier with automatic level control,
- a dynamic limiter with a short limiting time.

Compared to its predecessor TDA1002, this type features an improved automatic level control circuit; the control range has been enlarged from 40 to 55 dB and the spread in control characteristic has been reduced to less than 2 dB.

### QUICK REFERENCE DATA

Supply voltage range	$V_p$		4 to 12 V
Operating ambient temperature	$T_{amb}$		–25 to + 125 °C
Total quiescent current ( $V_p = 9$ V)	$I_{tot}$	typ.	15 mA
<b>Preamplifier</b>			
Input impedance (pin 1)	$ Z_i $	typ.	16 k $\Omega$
Open loop gain	$G_o$	typ.	70 dB
Clipping level (pin 4); $V_p = 9$ V; r.m.s. value	$V_{4-5(rms)}$	typ.	2 V
Equivalent noise input voltage $R_S = 500 \Omega$ ; B = 300 Hz to 15 kHz	$V_{n(rms)}$	<	0,75 $\mu$ V
<b>Recording amplifier</b>			
Input impedance (pin 8)	$ Z_i $	typ.	40 k $\Omega$
Open loop gain	$G_o$	typ.	80 dB
Clipping level (pin 9); $V_p = 9$ V; r.m.s. value	$V_{9-10(rms)}$	typ.	2 V
<b>Automatic Level Control (A.L.C.)</b>			
Input impedance (pin 6)			
at low signal level at pin 8	$ Z_i $	typ.	250 k $\Omega$
at high signal level pin 8	$ Z_i $	typ.	25 $\Omega$
Control voltage			
$V_{4-5} = 10$ mV; f = 1 kHz; $V_p = 9$ V	$V_{9-10}$	typ.	250 mV
$V_{4-5} = 1000$ mV; f = 1 kHz; $V_p = 9$ V	$V_{9-10}$	typ.	750 mV
Limiting time (Fig. 12)	$t_l$	typ.	10 ms
Level setting time (Fig. 12)	$t_s$	typ.	4 s
Recovery time (Fig. 13)	$t_r$	typ.	35 s

### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

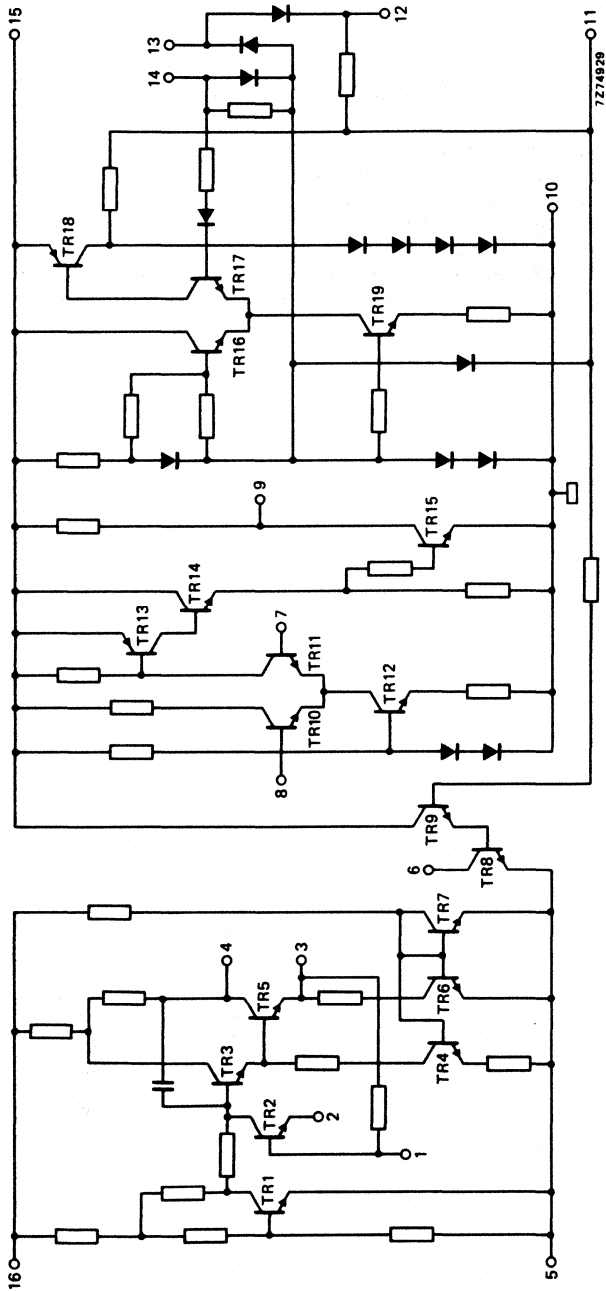


Fig. 1 Circuit diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage preamplifier	V <sub>16-5</sub>	max.	12 V
Supply voltage recording amplifier	V <sub>15-10</sub>	max.	12 V
Total power dissipation			see derating curve Fig. 2
Storage temperature	T <sub>stg</sub>		-65 to + 125 °C
Operating ambient temperature	T <sub>amb</sub>		-25 to + 125 °C

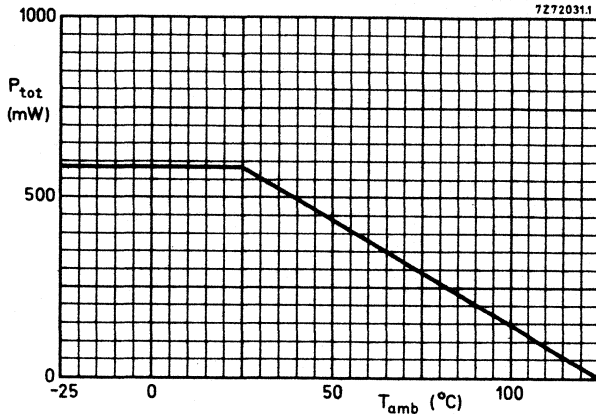


Fig. 2 Power dissipation derating curve.

**D.C. CHARACTERISTICS**T<sub>amb</sub> = 25 °C unless otherwise specified.

Supply voltage recording amplifier	V <sub>15-10</sub>		4 to 12 V
Supply voltage preamplifier	V <sub>16-5</sub>		4 to 12 V
Quiescent current rec. amplifier; V <sub>p</sub> = 9 V	I <sub>15</sub>	typ.	10 mA
Quiescent current preamplifier; V <sub>p</sub> = 9 V	I <sub>16</sub>	typ.	5 mA
Output voltage recording amplifier	V <sub>9-10</sub>	typ.	½ V <sub>p</sub> V
Output voltage preamplifier	V <sub>4-5</sub>	typ.	½ V <sub>p</sub> - 0,35 V

**A.C. CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_p = 9\text{ V}$  unless otherwise specified.

**Preamplifier (note 1)**

			recording	playback
Open loop voltage gain	$G_o$	typ.	70	70 dB
Closed loop voltage gain at $f = 1\text{ kHz}$	$G_c$	typ.	38	45 dB
Output voltage (clipping level); r.m.s. value	$V_{4-5(rms)}$	typ.	2	2 V
Equivalent noise input voltage; r.m.s. value (note 2)	$V_n$	<	0,75	0,75 $\mu\text{V}$
Input impedance (pin 1)	$ Z_i $	typ.	16	16 $\text{k}\Omega$
Total harmonic distortion				
$f = 1\text{ kHz}$ ; $V_{4-5} = 150\text{ mV}$	$d_t$	typ.	—	0,12 %
$f = 1\text{ kHz}$ ; $V_{4-5} = 500\text{ mV}$	$d_t$	<	0,2	—
Amplitude response			flat: 20 Hz to 20 kHz see Fig. 7	

**Recording amplifier (Fig. 9)**

with A.L.C.; unless otherwise specified.

Open loop gain	$G_o$	typ.	80 dB
Closed loop voltage gain at $f = 1\text{ kHz}$ (note 3)	$G_c$	typ.	49 dB
Output voltage (clipping level); r.m.s. value	$V_{9-10(rms)}$	typ.	2 V
Input impedance pin 8	$ Z_i $	typ.	40 $\text{k}\Omega$
Input impedance pin 6			
low signal levels	$ Z_i $	typ.	250 $\text{k}\Omega$
high signal levels	$ Z_i $	typ.	25 $\Omega$
Total harmonic distortion			see Fig. 11
Amplitude response (note 3)			see Fig. 10

**Automatic level control (see Fig. 8)**

$V_{4-5} = 10\text{ mV}$ ; $f = 1\text{ kHz}$	$V_{9-10}$	typ.	250 mV
$V_{4-5} = 100\text{ mV}$ ; $f = 1\text{ kHz}$	$V_{9-10}$	typ.	450 mV
$V_{4-5} = 1000\text{ mV}$ ; $f = 1\text{ kHz}$	$V_{9-10}$	typ.	750 mV
$V_{4-5} = 2000\text{ mV}$ ; $f = 1\text{ kHz}$	$V_{9-10}$	typ.	880 mV
Limiting time (see Fig. 12)	$t_l$	typ.	10 ms
Level setting time (see Fig. 12)	$t_s$	typ.	4 s
Recovery time (see Fig. 13)	$t_r$	typ.	35 s

**Notes**

1. For recording see Fig. 3; for playback see Fig. 5.
2.  $R_S = 500\text{ }\Omega$ ; bandwidth = 300 Hz to 15 kHz.
3. Pin 6 not connected to pin 8.

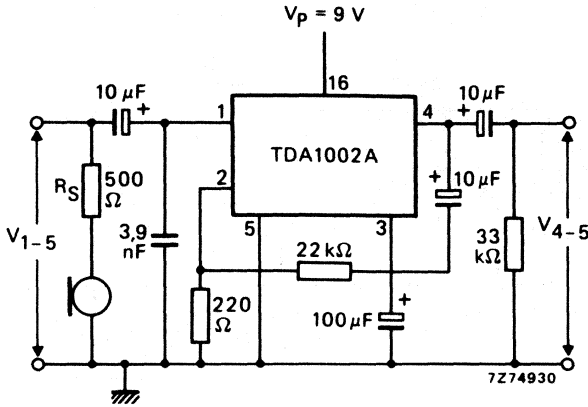


Fig. 3 Preamplifier used as microphone amplifier.

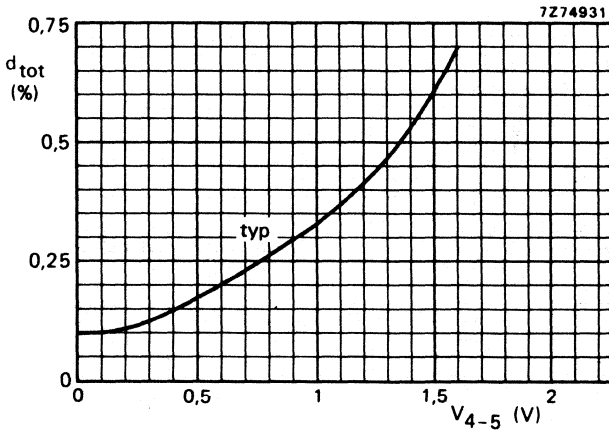


Fig. 4 Total harmonic distortion of preamplifier used for recording.

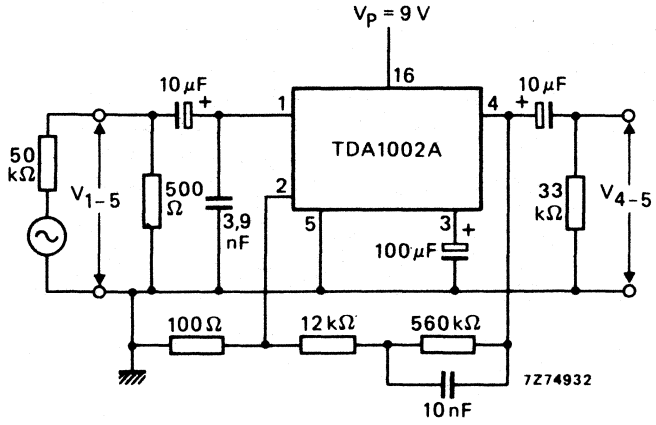


Fig. 5 Preamplifier used for playback.

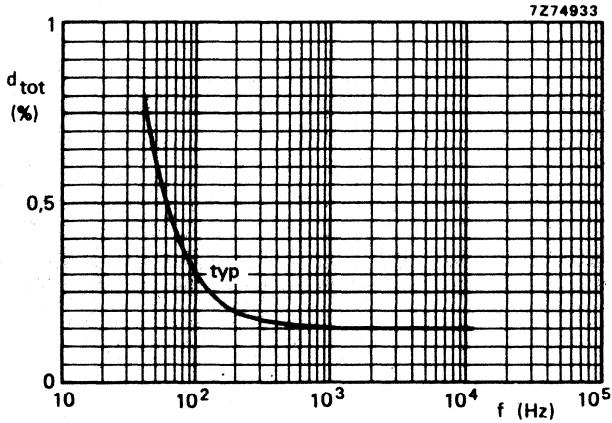


Fig. 6 Total harmonic distortion of preamplifier used for playback at  $V_{4.5} = 150\text{ mV}$ .

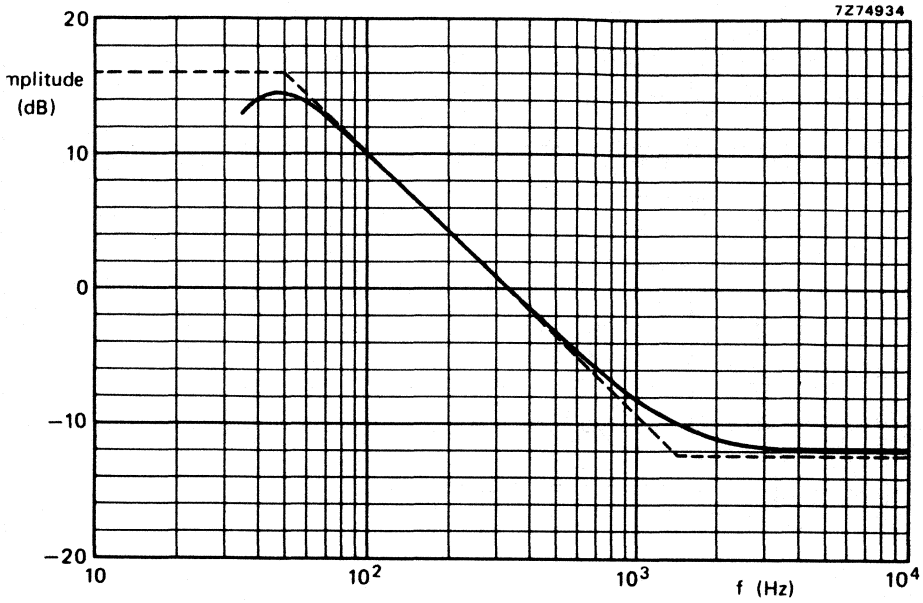


Fig. 7 Amplitude response of preamplifier used for playback; typical values. 0 dB = input voltage of 0,3 mV at f = 333 Hz. Dotted line according to DIN 45513.

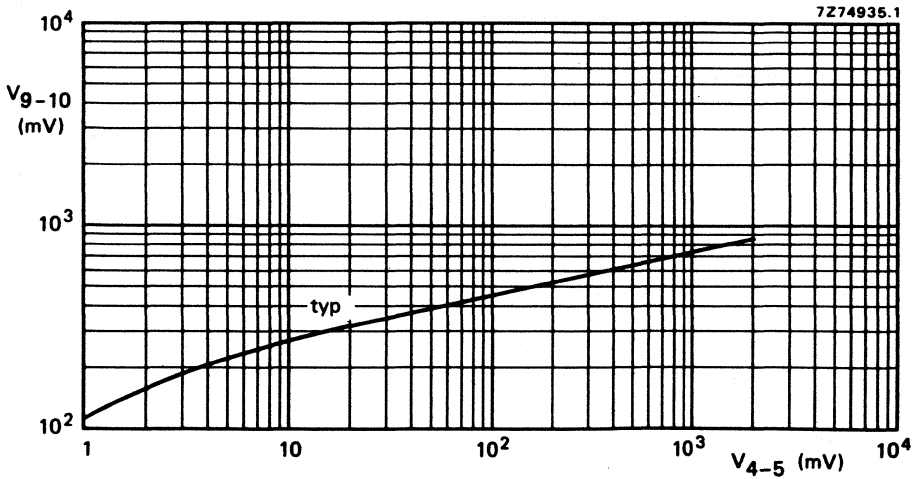


Fig. 8 Automatic level control; for circuitry see Fig. 9; f = 1 kHz.

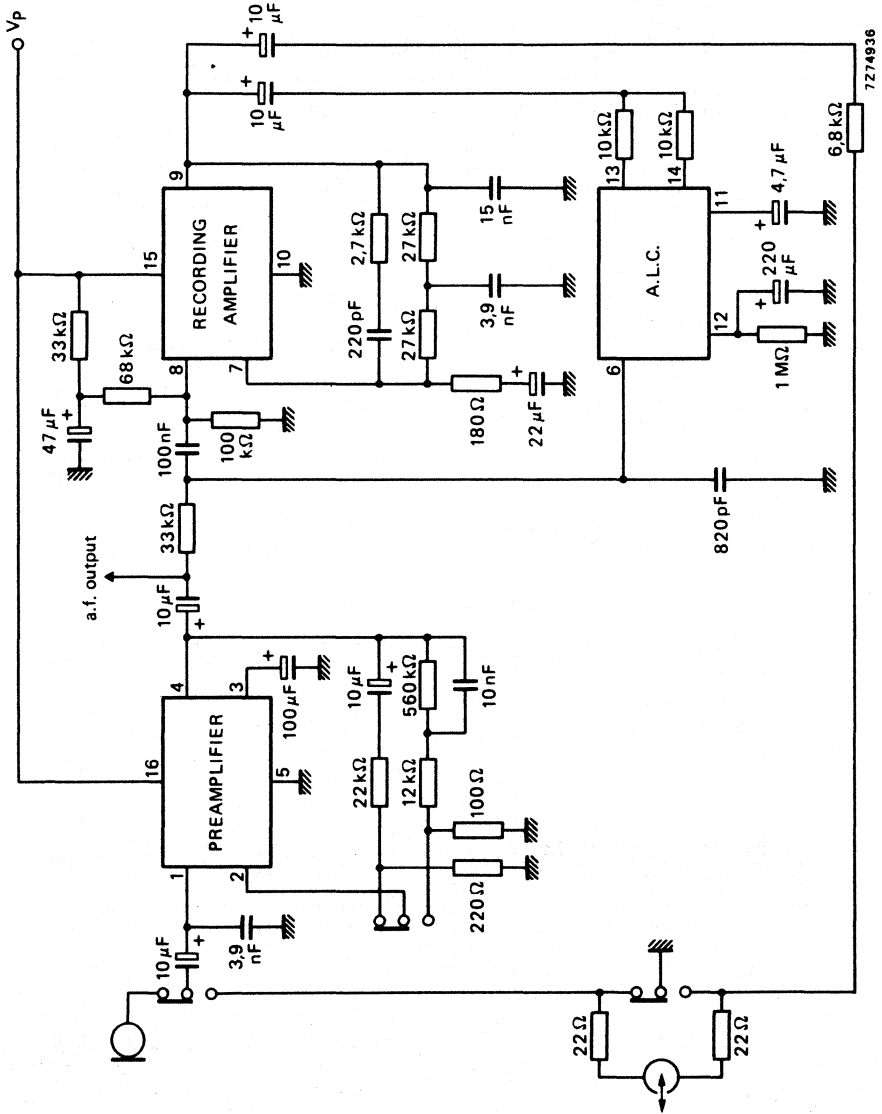


Fig. 9 Application of TDA1002A (recording position).



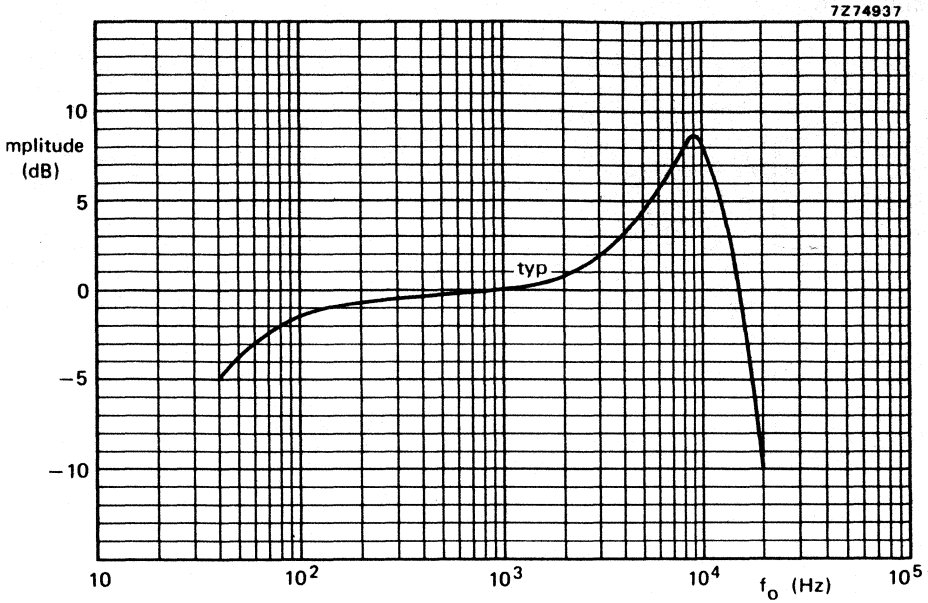


Fig. 10 Amplitude response of recording amplifier (A.L.C. not connected).

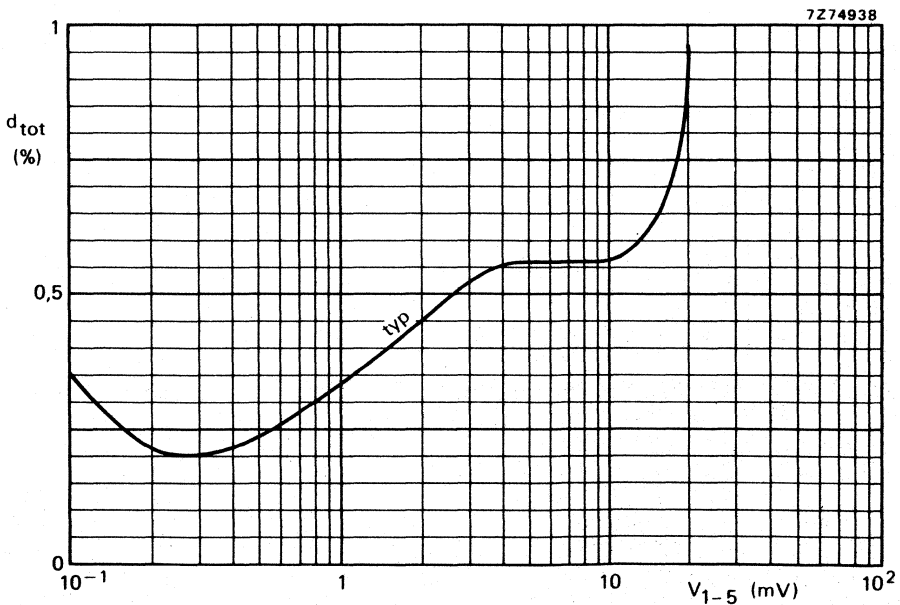


Fig. 11 Total harmonic distortion recording amplifier with A.L.C.; f = 1 kHz.

TIMING DIAGRAMS

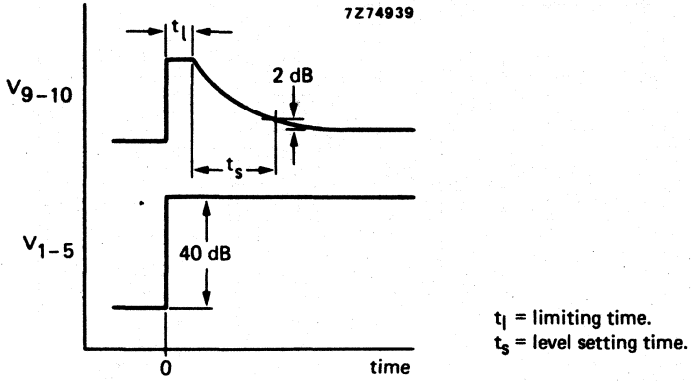


Fig. 12 Output response at input level jumps.

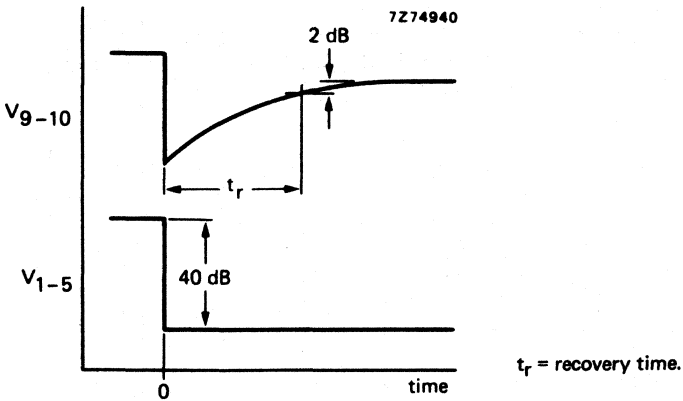


Fig. 13 Output response at input level jumps.

## FREQUENCY MULTIPLEX PLL STEREO DECODER

The TDA1005A is a high quality PLL stereo decoder based on the frequency-division multiplex (f.d.m.) principle, performing:

- excellent ACI (Adjacent Channel Interference) and SCA (Storecast) rejection
- very low BFC (Beat-Frequency Components) distortion in the higher frequency region

The circuit incorporates the following features:

- with simplified peripheral circuitry the circuit can perform as a time-division multiplex (t.d.m.) decoder, for use in economic medium and low-class apparatus
- for car radios: operation at a supply voltage of 8 V
- extra pin for smooth mono/stereo take-over without "clicks"
- automatic mono/stereo switching (minimum switching level is 16 mV), controlled by both pilot signal and field strength level
- low distortion in the loop resonance frequency region ( $\approx 300$  Hz; THD = 0,2% typ.)
- external adjustment for obtaining optimum channel separation in the complete receiver
- internal amplification: t.d.m., 7 dB; f.d.m., 10 dB
- driver for stereo indicator lamp
- externally switchable: VCO-off or mono condition
- guaranteed VCO capture range ( $> 3,5\%$  or 2,7 kHz)

### QUICK REFERENCE DATA

Supply voltage range	$V_{8-16}$		8 to 18	V
Supply voltage	$V_{8-16}$	typ.	15	V
Ambient temperature	$T_{amb}$	typ.	25	°C
-----				
Measured at $V_i(p-p) = 1$ V (MUX signal with 8% pilot)			t.d.m.	f.d.m.
Channel separation at $f = 1$ kHz	$\alpha$	typ.	50	55 dB
Carrier suppression				
at $f = 19$ kHz	$\alpha_{19}$	typ.	36	36 dB
at $f = 38$ kHz	$\alpha_{38}$	typ.	45	40 dB
at $f = 76$ kHz	$\alpha_{76}$	typ.	80	75 dB
ACI rejection at $f = 114$ kHz	$\alpha_{114}$	typ.	52	70 dB
SCA rejection at $f = 67$ kHz	$\alpha_{67}$	typ.	85	90 dB
VCO capture range		$>$	3,5	3,5 %
Total harmonic distortion				
$f_m = 1$ kHz	THD	typ.	0,2	0,1 %
$f_m = 300$ Hz to 10 kHz	THD	typ.	0,2	0,1 %
BFC suppression	$d_{BFC}$	$>$	40	60 dB

### PACKAGE OUTLINES

TDA1005A ; 16-lead DIL; plastic (SOT-38).

TDA1005AT; 16-lead flat pack; plastic (SO-16; SOT-109A).

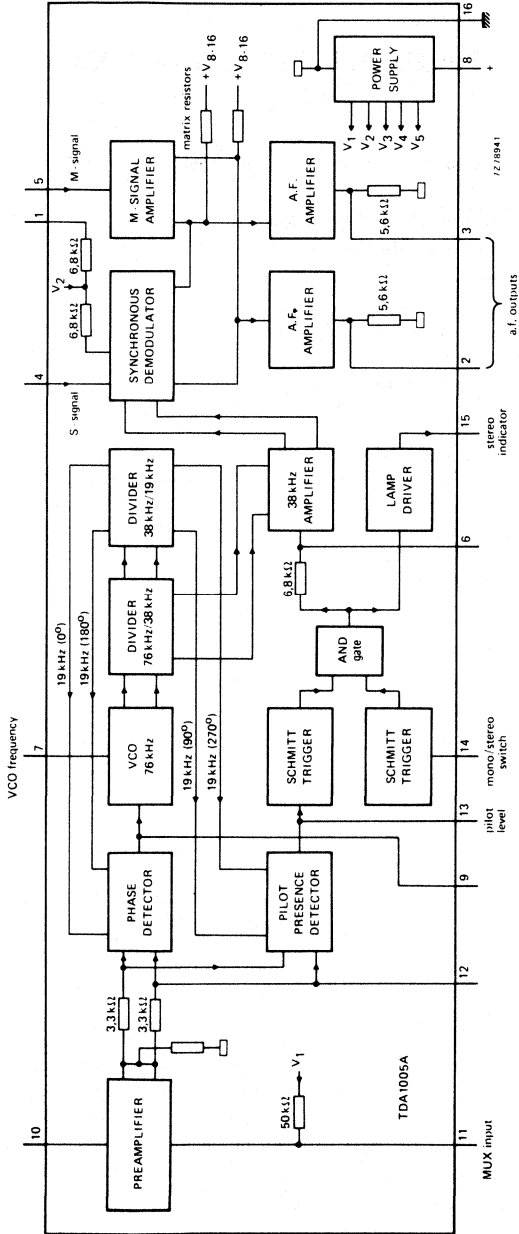


Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V <sub>8-16</sub>	max.	18 V
Indicator lamp voltage	V <sub>15-16</sub>	max.	22 V
Mono/stereo switching voltage	V <sub>14-16</sub>	max.	4 V
Indicator lamp current	I <sub>15</sub>	max.	100 mA
Indicator lamp turn-on current (peak value)	I <sub>15M</sub>	max.	200 mA
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T <sub>stg</sub>	-55 to + 150 °C	
Operating ambient temperature (see also Fig. 2)	T <sub>amb</sub>	-25 to + 150 °C	

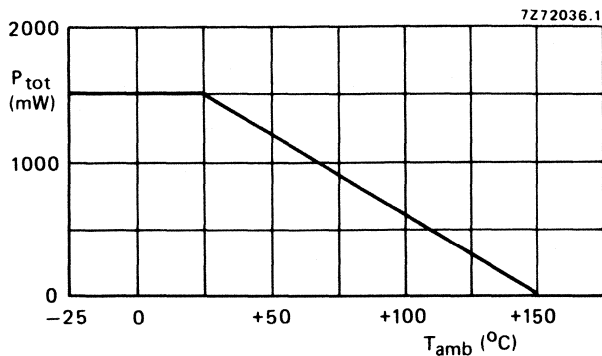


Fig. 2 Power derating curve.



A.C. CHARACTERISTICS and APPLICATION INFORMATION

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{8-16} = 15\text{ V}$  (unless otherwise specified); see also Fig. 7 and Fig. 10.

	note	pin	parameter	t.d.m.	f.d.m.	unit	
Channel separation see Figs 23 and 24	1, 2	2, 3	$\alpha$	>	40	45	dB
				typ.	50	55	dB
F.M.—I.F. roll-off correction range	1, 2			48 to 72	—	kHz	
Input MUX-voltage; L = 1; R = 1 for THD < 0,35%	1, 2	11	$V_{i(p-p)}$	typ.	1	1	V
Input impedance		11	$ Z_i $	>	35	35	k $\Omega$
				typ.	50	50	k $\Omega$
Voltage gain per channel	1, 2		$G_V$	typ.	7	10	dB
Channel balance	1, 2		$\pm \Delta G_V$	<	1	1	dB
Output voltage (r.m.s. value) L = 1; R = 1	1, 2	2	$V_{2-16(rms)}$	>	0,61	0,97	V
		3	$V_{3-16(rms)}$	>	0,61	0,97	V
Output impedance	3	2, 3	$ Z_o $	typ.	5,6	5,6	k $\Omega$
					4 to 7	4 to 7	k $\Omega$
Total harmonic distortion; see Figs 25 and 26 $f_m = 1\text{ kHz}$ (all conditions)	1	2, 3	THD	typ.	0,2	0,1	%
	1	2, 3	THD	<	0,35	0,35	%
		2, 3	THD	typ.	0,2	0,1	%
Carrier suppression		2, 3					
f = 19 kHz; without notch filter	1		$\alpha_{19}$	typ.	36	36	dB
f = 19 kHz; with notch filter	1, 9		$\alpha_{19}$	typ.	60	60	dB
f = 38 kHz; without notch filter	1		$\alpha_{38}$	>	40	38	dB
f = 38 kHz; with notch filter	1, 9		$\alpha_{38}$	>	72	72	dB
f = 57 kHz; without notch filter	1		$\alpha_{57}$	typ.	46	56	dB
f = 57 kHz; with notch filter	1, 9		$\alpha_{57}$	typ.	59	61	dB
f = 76 kHz; without notch filter	1		$\alpha_{76}$	typ.	80	75	dB
ACI rejection		2, 3					
at f = 114 kHz	4		$\alpha_{114}$	typ.	52	70	dB
at f = 190 kHz	4		$\alpha_{190}$	typ.	55	74	dB
SCA rejection at f = 67 kHz	5	2, 3	$\alpha_{67}$	typ.	85	90	dB
Ripple rejection; f = 100 Hz; $V_{8-16(rms)} = 200\text{ mV}$			RR	>	40	40	dB
				typ.	50	50	dB



	note	pin	parameter	t.d.m.	f.d.m.	unit
VCO; adjustable with R7-16						
nominal frequency	6		$f_{VCO}$ typ.	76	76	kHz
capture range (deviation from 76 kHz centre frequency)	6		>	3,5	3,5	%
19 kHz pilot signal of 32 mV	6					
temperature coefficient uncompensated	6		-TC typ.	$450 \cdot 10^{-6}$	$450 \cdot 10^{-6}$	K <sup>-1</sup>
compensated	6		± TC typ.	$200 \cdot 10^{-6}$	$200 \cdot 10^{-6}$	K <sup>-1</sup>
Stereo/mono switch						
when equal to 19 kHz pilot-tone threshold voltage; adjustable with R13-8	7	11	$V_i$	10 to 100	10 to 100	mV
when equal to threshold voltage at R13-8 = 620 kΩ		11	$V_i$	7 to 16	7 to 16	mV
for switching to stereo		11	$V_i$ <	5	5	mV
for switching to mono						
hysteresis	8	11	$\Delta V_i$ typ.	2,5	2,5	dB
Smooth take-over circuit						
full mono	8	6	$V_{6-16}$ <	0,65	0,65	V
full stereo	8	6	$V_{6-16}$ >	1,3	1,3	V

Notes

- $V_{i(p-p)} = 1$  V (MUX signal with 8% pilot level).
  - $f_m = 1$  kHz.
  - At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.
  - Measured with a composite input signal: L = R;  $f_m = 1$  kHz; 90% M-signal; 9% pilot signal; 1% spurious signal of 110 kHz (for  $\alpha_{114}$ ) or 186 kHz (for  $\alpha_{190}$ ).  
ACI suppression is defined as:  $20 \log \frac{V_o \text{ (at 4 kHz)}}{V_o \text{ (at 1 kHz)}}$ .
  - Measured with a composite input signal: L = R;  $f_m = 1$  kHz; 80% S-signal; 9% pilot signal; 10% SCA carrier (67 kHz);  $d_{13} = 20 \log \frac{V_o \text{ (at 9 kHz)}}{V_o \text{ (at 1 kHz)}}$ .
  - See also Figs 7 and 10; compensated with RC network on pin 7.
  - Adjustable with R13-8; see also Fig. 28; for field strength dependent input (pin 14) see next page.
  - $\Delta V_i = 20 \log \frac{V_{11-16} \text{ (mono/stereo)}}{V_{11-16} \text{ (stereo/mono)}}$ .
- For additional circuitry on pin 6 see Figs 7 and 10; for graph see Fig. 29.
- For example of notch filter see Fig. 6.



### D.C. CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{8-16} = 15\text{ V}$  (unless otherwise specified)

Supply voltage range	$V_{8-16}$		8 to 18 V *
Total current (except indicator lamp)	$I_g$	typ.	21 mA
Power dissipation (operating) at lamp current $I_{15} = 100\text{ mA}$ ; $V_{8-16} = 18\text{ V}$	$P_{tot}$	<	570 mW
Saturation voltage of lamp driver at $I_{15} = 100\text{ mA}$	$V_{15-16}$	typ.	0,9 V
Maximum lamp driver voltage	$V_{15-16}$	<	22 V
Switching voltage to mono	$V_{14-16}$	>	1,2 V **
to stereo	$V_{14-16}$	<	0,65 V
hysteresis	$V_{14-16}$	typ.	0,2 V

### APPLICATION NOTES

#### 1. Switching-off the VCO

If the internal gain is used with A.M. reception, the VCO can be switched off by connecting pin 9 via a 100 k $\Omega$  resistor to ground (no h.f. signal on the leads), or connecting pin 7 to ground.

#### 2. Mono button

The decoder can be switched to the mono position by connecting pin 12 to ground. The VCO then remains operational so this possibility cannot be used with A.M. reception.

#### 3. Economic periphery

- a. For a fixed stereo switching level of  $\leq 16\text{ mV}$  a resistor of 620 k $\Omega$  can be connected between pin 13 and positive supply (+) instead of a potentiometer in series with a resistor.
- b. The 10 k $\Omega$  resistor connected in parallel with the stereo indicator lamp can be omitted, however, some TDA1005A circuits will switch to mono during lamp failure.
- c. The 10  $\mu\text{F}$  capacitor in series with a 1 k $\Omega$  resistor at pin 9 can be decreased to a 1  $\mu\text{F}$  capacitor, bearing in mind that the distortion will increase, especially around loop resonance.
- d. A MUX-input filter is not needed, if i.f. roll-off starts at a frequency of 62 kHz.

#### 4. Printed-circuit boards

For both the f.d.m. and t.d.m. stereo decoder circuits a printed-circuit board layout is given as an example (Figs 8 and 11). Also for an active filter, which is mainly used with a t.d.m. decoder, a printed-circuit board layout is given in Fig. 4.

#### 5. Notch filter

If attention has to be paid for suppression of the 57 kHz signal (T.W.S. = Traffic Warning System) and the 19 kHz signal, an input filter can be used as given in Fig. 6.

\* At supply voltages of 8 to 11 V, resistors of 5,6 k $\Omega$  have to be connected from ground to pins 2 and 3.

\*\* Maximum voltage for safe operation:  $V_{14-16} < 4\text{ V}$ .



APPLICATION INFORMATION

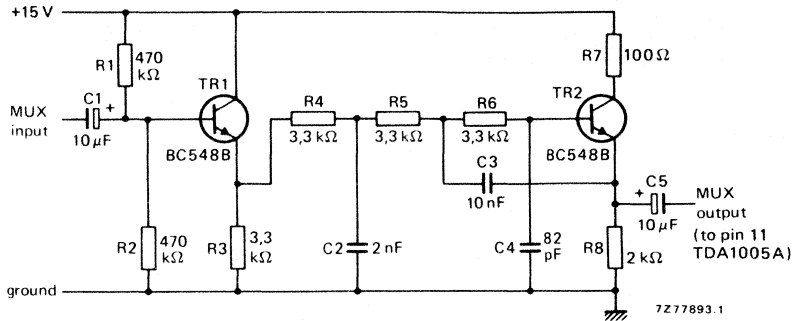


Fig. 3 Active filter circuit diagram.

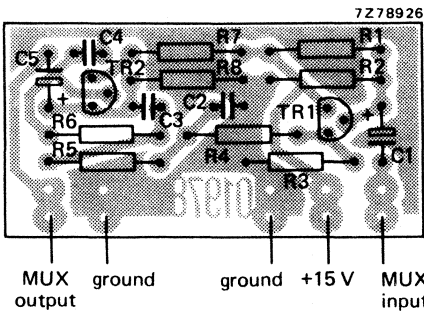


Fig. 4 Printed-circuit board component side, showing component layout.

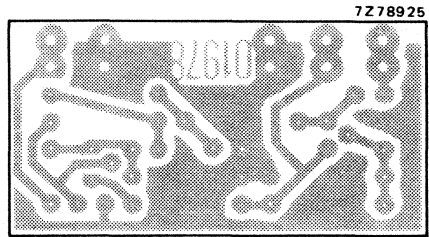
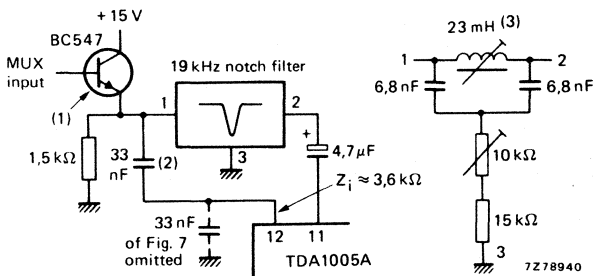
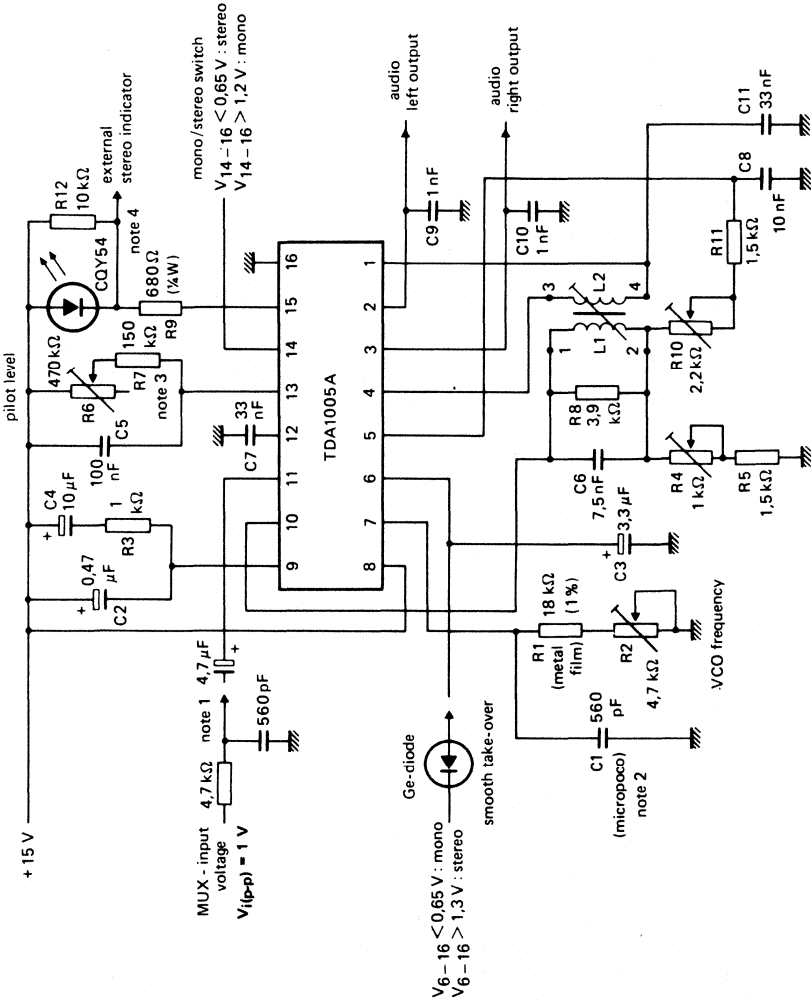


Fig. 5 Printed-circuit board showing track side.



- (1) Transistor to achieve low impedance driving of notch filter.
- (2) 33 nF will give common mode suppression of 19 kHz.
- (3) Coil: TOKO 10 PA, 700 turns,  $\phi$ 0,07 mm Cu; case type: P06-0114; drumcore: AN01-0021; base 5 pins type: 07-0084-02; core type CAN02-0029.

Fig. 6 Example of using a 19 kHz tuned notch filter; for other input structures see Figs 13 to 21.



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**Notes**

1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micro-poco capacitor has a temperature coefficient of  $125 \cdot 10^{-6} \pm 60 \cdot 10^{-6} \text{ K}^{-1}$ .
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of  $\leq 16 \text{ mV}$ .
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 7 Basic application circuit of a frequency-division multiplex (f.d.m.) stereo decoder.

**Coil data:**  
 $L_1 L_2 = 2,6 \text{ mH}$   
 $Q_{1-2} = 35; Q_{\text{min}} \approx 30$   
 $N_{1-2} = 357\frac{1}{2} \text{ turns;}$   
 $N_{3-4} = 297\frac{1}{2} \text{ turns;}$   
 scrambled wound with  
 wire diameter 0,09 mm,  
 $\frac{E_{3-4}}{E_{1-2}} \times 100\% = 82\%$

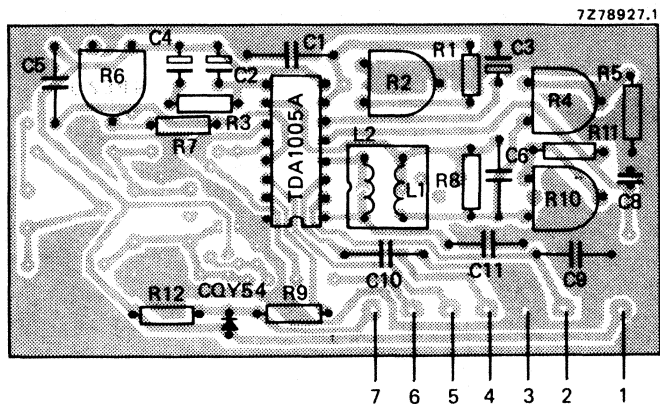


Fig. 8 Printed-circuit board component side of an f.d.m. decoder, showing component layout. For circuit diagram see Fig. 7.

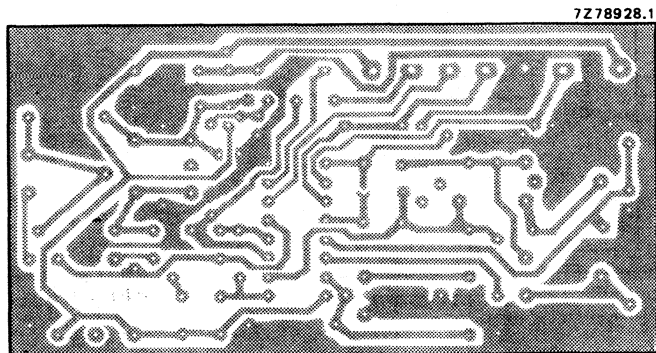
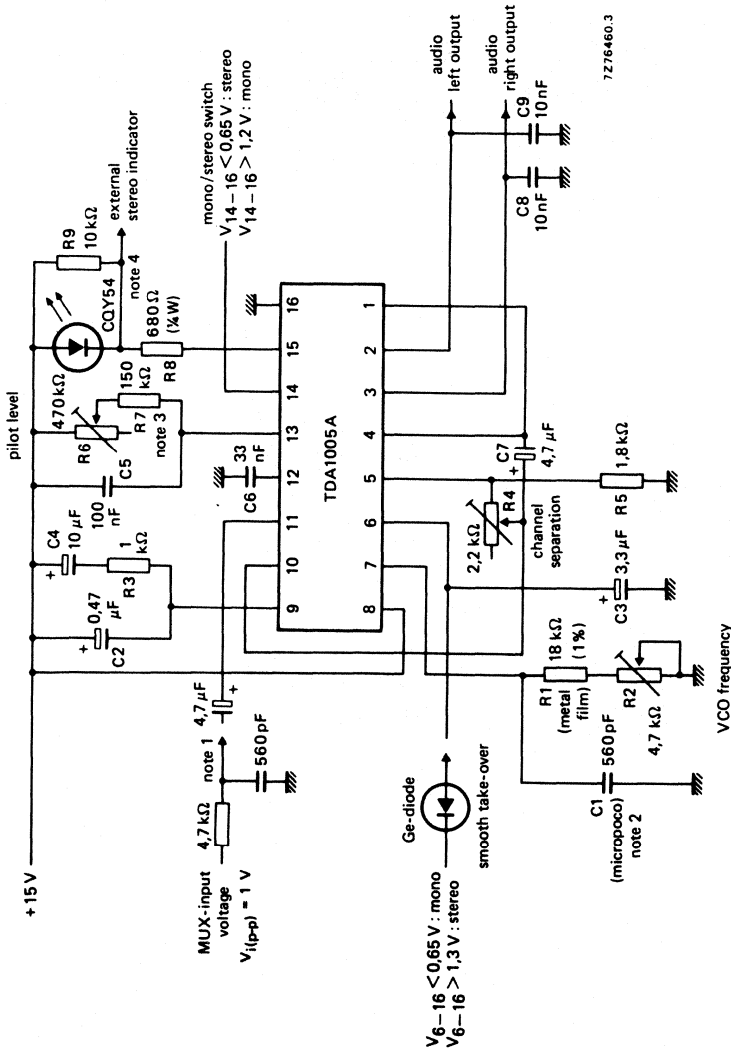


Fig. 9 Printed-circuit board showing track side.





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**Notes**

1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micro-poco capacitor has a temperature coefficient of  $125 \cdot 10^{-6} \pm 60 \cdot 10^{-6} \text{ } ^\circ\text{C}^{-1}$ .
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of  $\leq 16 \text{ mV}$ .
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 10 Basic application circuit of a time-division multiplex (t.d.m.) stereo decoder.

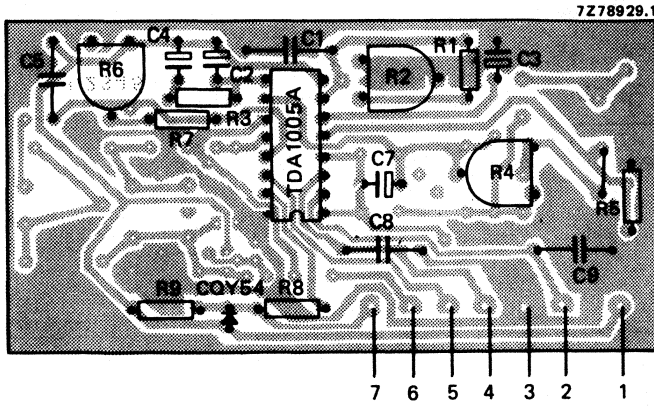


Fig. 11 Printed-circuit board component side of a t.d.m. decoder, showing component layout. For circuit diagram see Fig. 10.

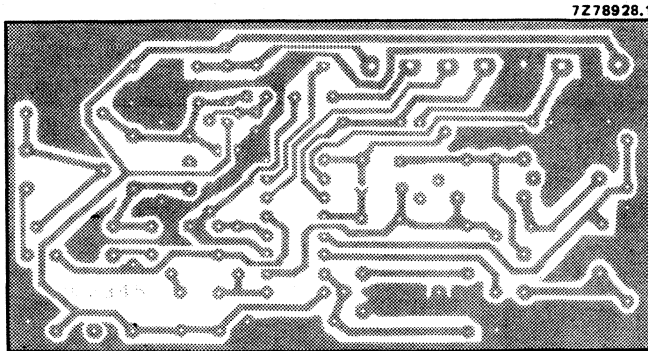


Fig. 12 Printed-circuit board showing track side.

INPUT STRUCTURES (see also Figs 7 and 10)

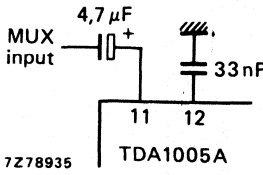


Fig. 13 Without filtering.

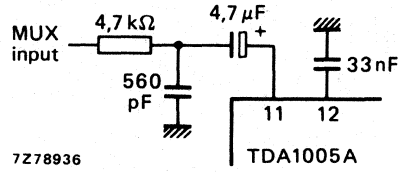


Fig. 15 With RC-filter for achieving i.f. roll-off (typ. 62 kHz).

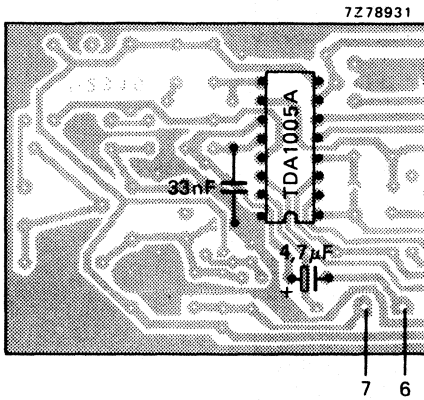


Fig. 14 Printed-circuit board component side, showing component layout of Fig. 13.

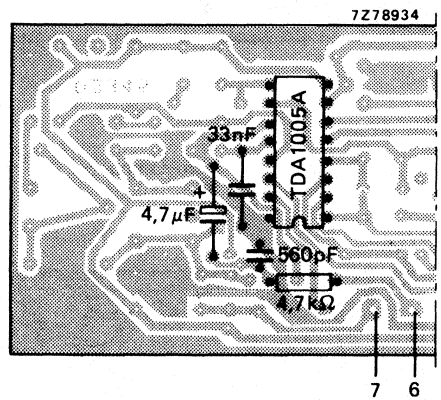


Fig. 16 Printed-circuit board component side, showing component layout of Fig. 15.

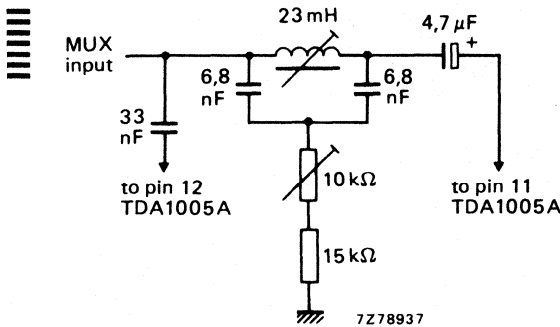


Fig. 17 With 19 kHz notch filter.

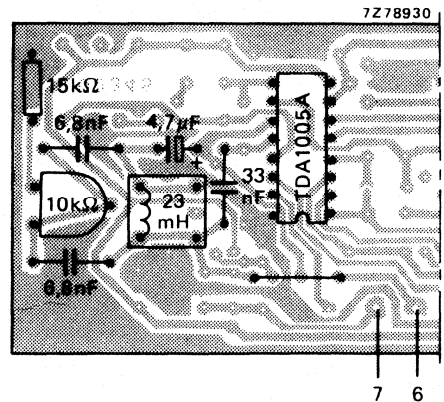


Fig. 18 Printed-circuit board component side, showing component layout of Fig. 17.

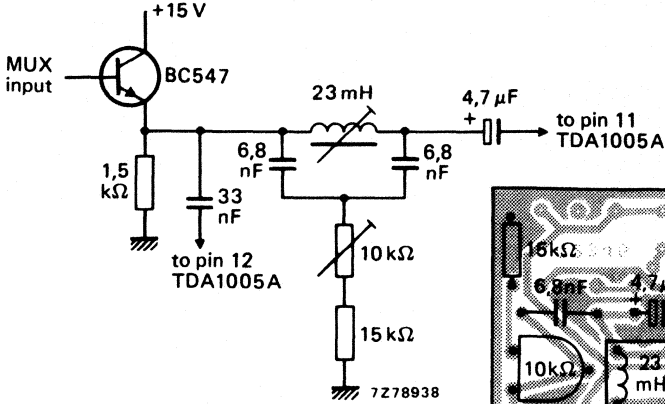


Fig. 19 With buffer stage (to achieve low impedance driving of notch filter; see Fig. 6) and 19 kHz notch filter.

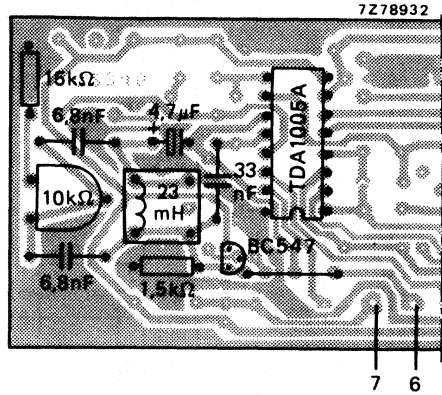


Fig. 20 Printed-circuit board component side, showing component layout of Fig. 19.

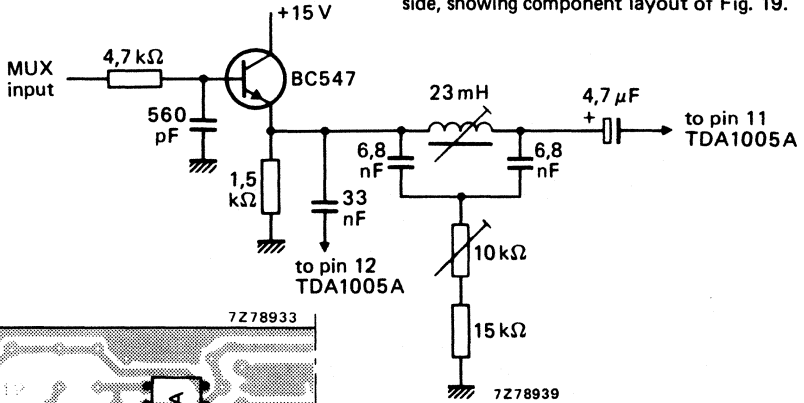


Fig. 21 With RC-filter, buffer stage and 19 kHz notch filter.

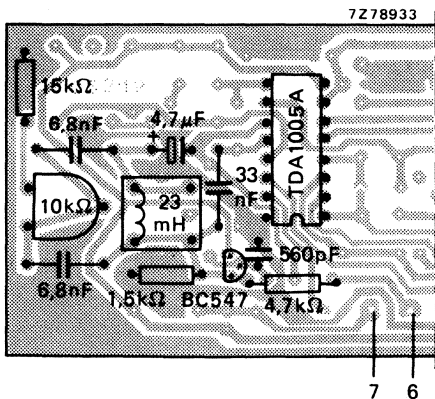
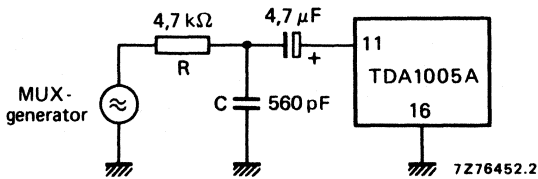
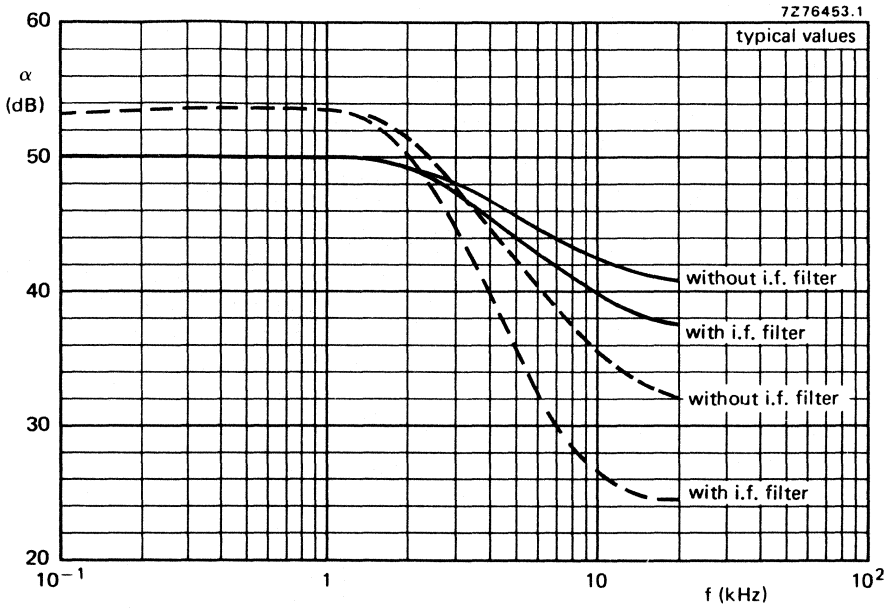


Fig. 22 Printed-circuit board component side, showing component layout of Fig. 21.



- time-division multiplex system; adjusted at 1 kHz (R4 in Fig. 10)
- - - frequency-division multiplex system; adjusted at 1 and 5 kHz (R4 and R10 in Fig. 7)

Conditions:  $V_{8,16} = 15$  V;  $V_{i(p-p)} = 1$  V.

Note: RC-filter for simulating the i.f. roll-off (typ. 62 kHz).

Fig. 23 Channel separation as a function of frequency.



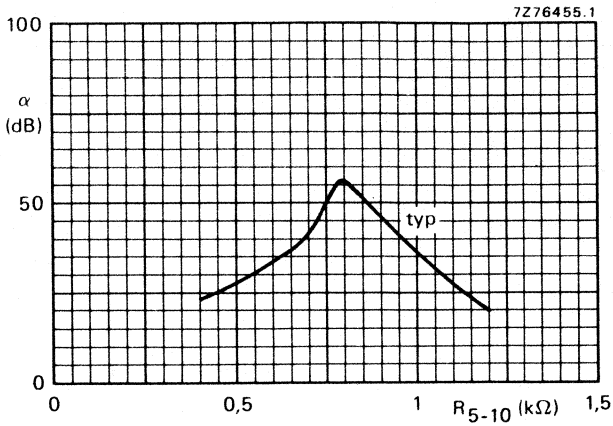


Fig. 24 Channel separation at  $f = 1$  kHz as a function of resistance between pins 5 and 10 for a t.d.m. system. For test circuit see Fig. 23.

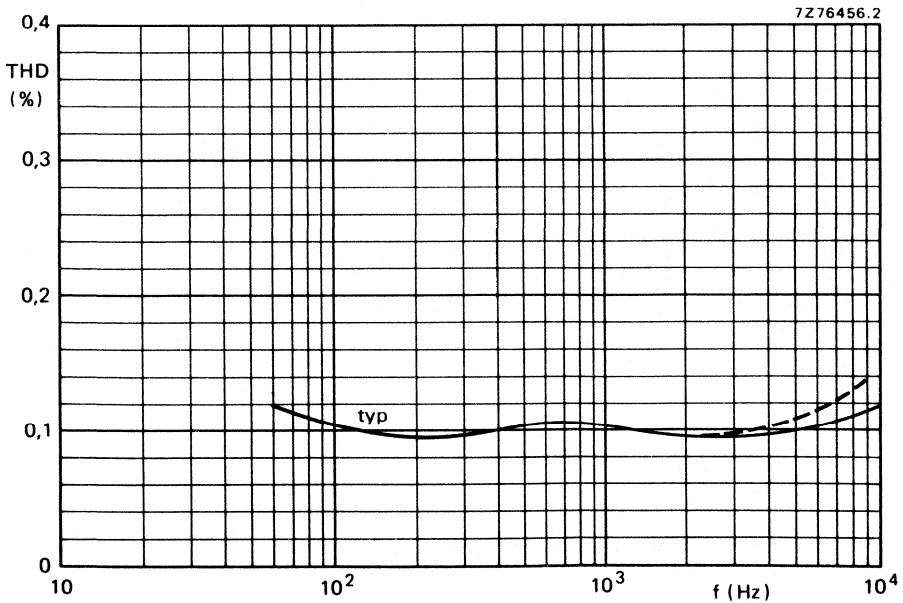
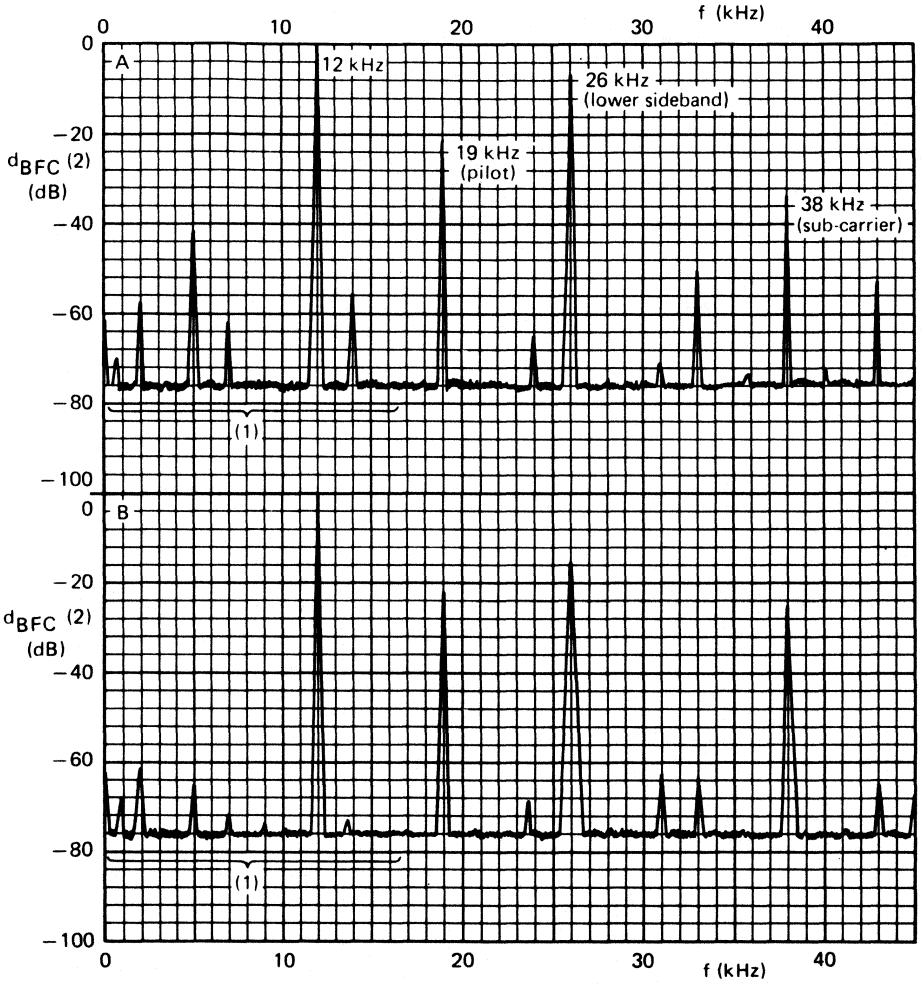


Fig. 25 Distortion as a function of audio frequency;  $R = 1$ ;  $L = 0$ ;  $V_{8-16} = 15$  V;  $V_{2-16} = V_{3-16} = 1$  V (r.m.s.). --- t.d.m. system; — f.d.m. system.



(1) Audible interferences (BFC-distortion) and desired 12 kHz signal.

$$(2) d_{BFC} = 20 \log \frac{V_{BFC}}{V \text{ (at 12 kHz)}}$$

Fig. 26 Spectrum at the decoder outputs; A for t.d.m.; B for f.d.m.  $V_{i(p-p)} = 1 \text{ V}$ ;  $R = 1$ ;  $L = 0$ ;  $m = 90\%$  for  $f = 12 \text{ kHz}$ ;  $m = 10\%$  for  $f = 19 \text{ kHz}$ .

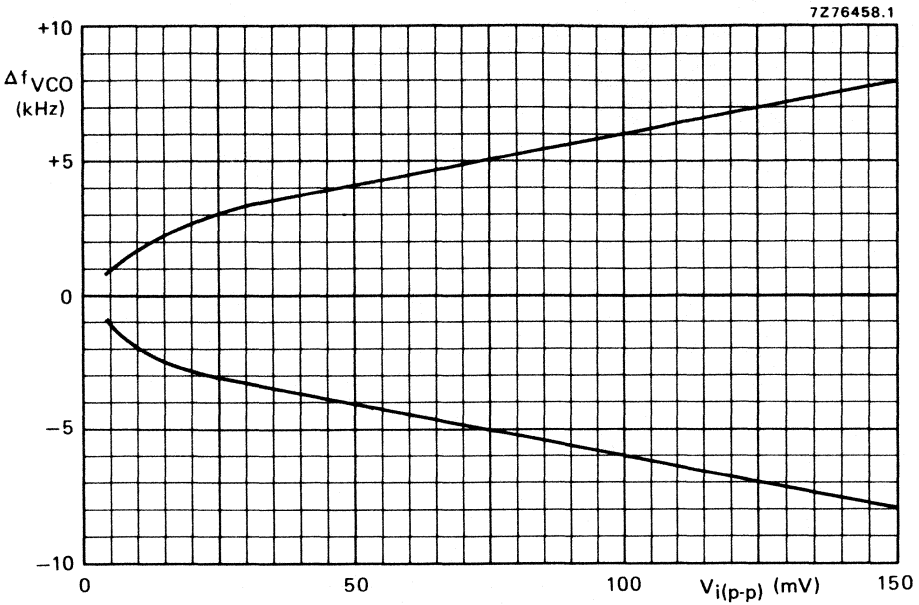


Fig. 27 Typical values of the capture range of the oscillator as a function of the pilot threshold voltage at MUX-input.

$V_{8-16} = 15 \text{ V}$ ;  $\Delta f_{VCO} = f_{VCO} - 76 \text{ kHz}$  where:  $f_{VCO}$  = modulated, free-running oscillator frequency;  
 $\Delta f_{VCO}$  = maximum  $f_{VCO}$  deviation which will be captured if pilot signal (pin 11) is switched-on.



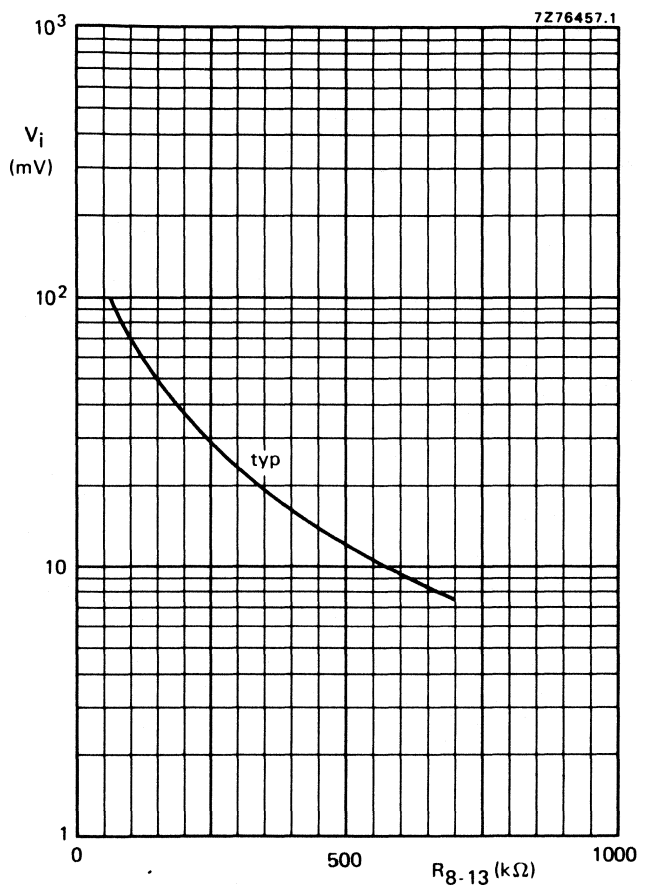


Fig. 28 Pilot input voltage switching level (stereo 'on') as a function of resistance between pins 8 and 13.

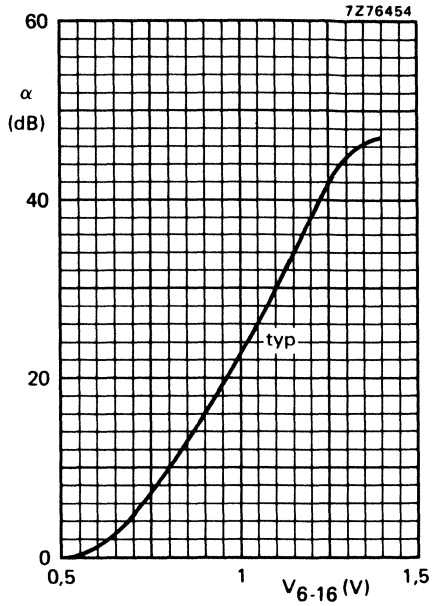


Fig. 29 Channel separation as a function of  $V_{6-16}$  at 1 kHz (smooth take-over).





## MOTOR REGULATOR WITH AUTOMATIC TAPE-END INDICATOR

### The TDA1006A is for use in car radio tape-decks

The circuit incorporates the following functions:

- capstan motor speed control;
- an electronic motor stop in conjunction with hysteresis slip-coupling or commutator pulses;
- an automatic switch from playback to radio at tape-end;
- playback indication with lamp;
- tape-end indication with intermittent light.

### QUICK REFERENCE DATA

Supply voltage range	$V_p$	6 to 22 V
Ambient temperature	$T_{amb}$	typ. 25 °C
Supply voltage	$V_p$	typ. 14 V

#### Motor regulator

Current consumption ( $R_{3-4} = 7,5 \text{ k}\Omega$ )

radio	$I_4$	typ. 9 mA
playback ( $I_1 = 0$ )	$I_4$	typ. 12 mA
playback	$I_4$	typ. 52 mA
tape-end	$I_4$	typ. 32 mA
Operating motor current	$I_3$	typ. 200 mA
Supply voltage rejection	$\Delta V_{3-2}/\Delta V_{4-2}$	typ. 1 mV/V

#### Automatic stop circuit

Input current	$I_{14}$	> 25 $\mu\text{A}$
Input voltage at commutator	$V_{11-2}$	-6 to +6 V

### PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-38BE-2).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage

pin 4	$V_{4-2}$	max.	24 V
pin 9	$V_{9-2}$	max.	24 V
	$V_{4-2}$	$\geq$	$V_{9-2}$

Output current

pin 1 (d.c. value)	$-I_1$	max.	40 mA
(peak value)	$-I_{1M}$	max.	100 mA
pin 3 (d.c. value)	$I_3$	max.	250 mA
(non-repetitive peak value)	$I_{3SM}$	max.	600 mA
pin 8 (d.c. value)	$-I_8$	max.	45 mA
(peak value)	$-I_{8M}$	max.	80 mA
pin 10 (d.c. value)	$-I_{10}$	max.	20 mA
(peak value)	$-I_{10M}$	max.	20 mA

Storage temperature

$T_{stg}$  -65 to +150 °C

Operating ambient temperature

see power derating curve Fig. 2

$T_{amb}$  -25 to +150 °C

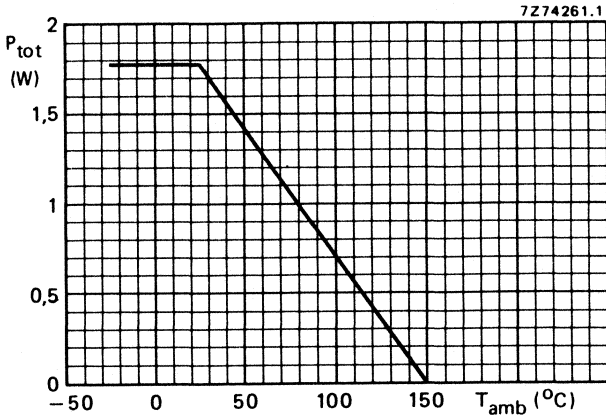


Fig. 2 Power derating curve; derating factor: 14,3 mW/°C.



## GATING/FREQUENCY DIVIDER FOR ELECTRONIC MUSICAL INSTRUMENTS

The TDA1008 is a monolithic bipolar integrated circuit based on  $I^2L$  (integrated injection logic), with frequency dividers directly coupled to the gating system.

The outputs of the dividers, together with the input signal, are applied internally to nine gate inputs. By activating a key input, five successive signals out of the nine are selected and transferred to the outputs. Five key inputs are available, each selecting a different combination; e.g.  $16^1$ ,  $8^1$ ,  $4^1$ ,  $2^1$  and  $1^1$ . The output signal level is proportional to the voltage applied to the key inputs. By connecting RC combinations to the key inputs, sustain of the output signal is easily obtained. The duration of the sustained signal can be adjusted by connecting a variable voltage to the appropriate terminal (pin 7).

In electronic organs using a top octave synthesizer directly coupled to twelve TDA1008 circuits, only one busbar per manual is needed to obtain five octave-related tones per key.

The tone output signals are symmetrical around a fixed d.c. voltage, thereby avoiding key clicks.

### QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_{P1-16}$	typ.	12 V
Supply voltage divider (pin 13)	$V_{P13-16}$	typ.	6 V
Supply voltage tone outputs (pins 2, 3, 4, 5, 6)	$V_{P_{tone}}$	typ.	9 V
Input voltage; HIGH	$V_{IH}$	>	1,5 V
Input voltage; LOW	$V_{IL}$	<	0,4 V
Required key voltage (pins 8, 9, 10, 11, 12)	$V_{K1}$ to $V_{K5}$	typ.	$V_{P13-16}$
Key input impedance (see note)	$Z_{K1}$ to $Z_{K5}$	>	8 M $\Omega$
Supply current (pin 1)			
all keys activated	$I_1$	typ.	13 mA
no activated keys	$I_1$	typ.	0 mA
Supply current (pin 13)	$I_{13}$	typ.	11 mA
Sustaining voltage range (pin 7)	$V_{7sust}$		0 to 2 V
Input frequency	$f_i$	<	100 kHz
Tone output signal voltage with one key activated	$V_{Q(p-p)}$	typ.	600 mV
Operating ambient temperature range	$T_{amb}$		0 to +70 °C

#### Note

Key input impedance is determined by the voltage applied to pin 7. This impedance is stated at zero volt on pin 7.

### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

**Supply voltages**

pin 1	$V_{P1-16}$	max.	13 V
pin 13	$V_{P13-16}$	max.	6,5 V
pin 14	$V_{P14-16}$	max.	6,5 V

**Input voltages**

K inputs (pins 8, 9, 10, 11, 12)	$V_{K1}$ to $V_{K5}$	max.	$V_{P13-16}$
$f_i$ input (pin 15)	$V_{fi}$	max.	15 V
S input (pin 7)	$V_S$	max.	2,5 V

**Output voltages**

$Q_1$ to $Q_5$ (pins 2, 3, 4, 5, 6)	$V_{Q1}$ to $V_{Q5}$	max.	12 V
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Operating ambient temperature

see derating curve Fig. 4

Storage temperature

$T_{stg}$  -25 to + 125 °C

Total power dissipation

see derating curve Fig. 4

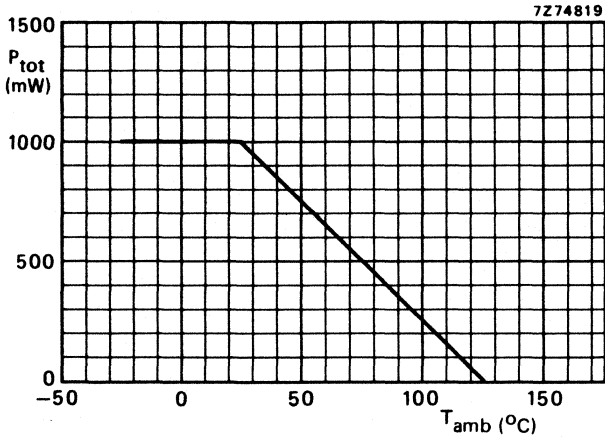


Fig. 4 Power derating curve.

## 6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS

### 10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4  $\Omega$  and 2  $\Omega$  load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

#### QUICK REFERENCE DATA

Supply voltage range	$V_P$	6 to 24 V
Repetitive peak output current	$I_{ORM}$	max. 3 A
Output power at pin 2; $d_{tot} = 10\%$		
$V_P = 14,4$ V; $R_L = 2 \Omega$	$P_O$	typ. 6,4 W
$V_P = 14,4$ V; $R_L = 4 \Omega$	$P_O$	typ. 6,2 W
$V_P = 14,4$ V; $R_L = 8 \Omega$	$P_O$	typ. 3,4 W
$V_P = 14,4$ V; $R_L = 2 \Omega$ ; with additional bootstrap resistor of 220 $\Omega$ between pins 3 and 4	$P_O$	typ. 9 W
Total harmonic distortion at $P_O = 1$ W; $R_L = 4 \Omega$	$d_{tot}$	typ. 0,2 %
Input impedance		
preamplifier (pin 8)	$ Z_i $	typ. 30 k $\Omega$
power amplifier (pin 6)	$ Z_i $	typ. 20 k $\Omega$
Total quiescent current at $V_P = 14,4$ V	$I_{tot}$	typ. 31 mA
Sensitivity for $P_O = 5,8$ W; $R_L = 4 \Omega$	$V_i$	typ. 10 mV
Operating ambient temperature	$T_{amb}$	-25 to + 150 $^{\circ}$ C
Storage temperature	$T_{stg}$	-55 to + 150 $^{\circ}$ C

#### PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

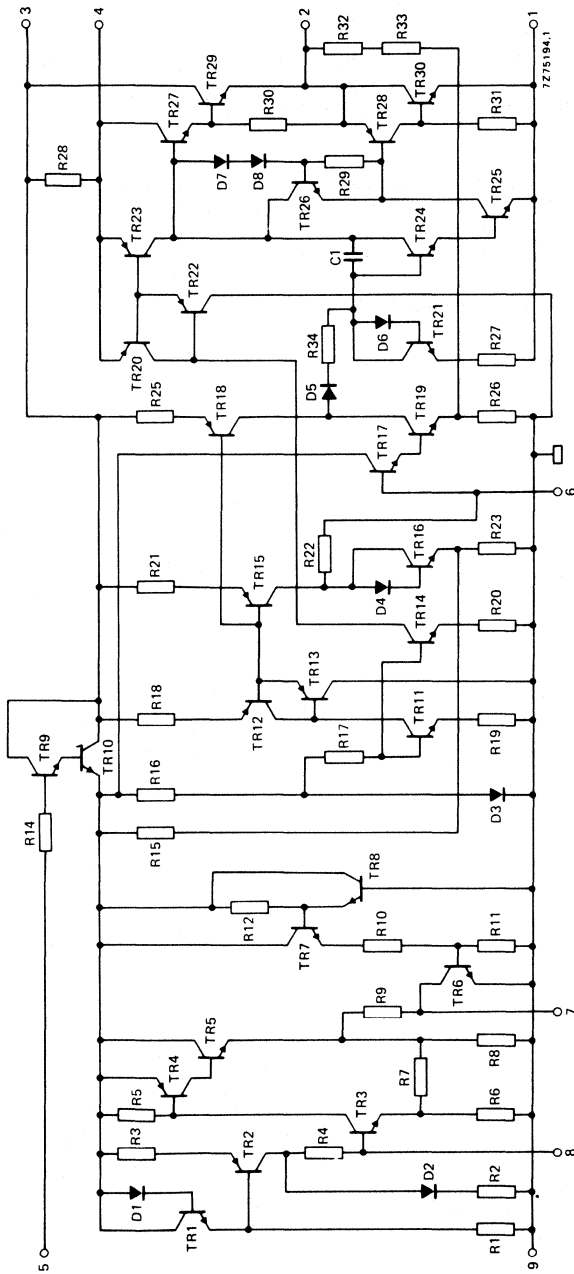


Fig. 1 Circuit diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p$	max.	24 V
Peak output current	$I_{OM}$	max.	5 A
Repetitive peak output current	$I_{ORM}$	max.	3 A
Total power dissipation			see derating curve Fig. 2
Storage temperature	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature	$T_{amb}$		-25 to + 150 °C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at $V_p = 14,4$ V	$t_{sc}$	max.	100 hours

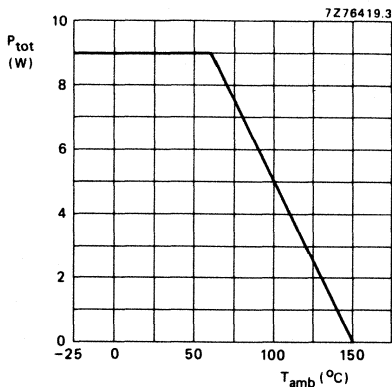


Fig. 2 Power derating curve.

**HEATSINK DESIGN**

Assume  $V_p = 14,4$  V;  $R_L = 2 \Omega$ ;  $T_{amb} = 60$  °C maximum; thermal shut-down starts at  $T_j = 150$  °C. The maximum sine-wave dissipation in a  $2 \Omega$  load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th j-a} = R_{th j-tab} + R_{th tab-h} + R_{th h-a} = \frac{150 - 60}{3,9} = 23 \text{ K/W.}$$

Since  $R_{th j-tab} = 10$  K/W and  $R_{th tab-h} = 1$  K/W,

$$R_{th h-a} = 23 - (10 + 1) = 12 \text{ K/W.}$$



**D.C. CHARACTERISTICS**

Supply voltage range	$V_P$	6 to 24 V
Repetitive peak output current	$I_{ORM}$	< 3 A
Total quiescent current at $V_P = 14,4$ V	$I_{tot}$	typ. 31 mA

**A.C. CHARACTERISTICS**

$T_{amb} = 25$  °C;  $V_P = 14,4$  V;  $R_L = 4$   $\Omega$ ;  $f = 1$  kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at  $d_{tot} = 10\%$ ;  
measured at pin 2; with bootstrap

$V_P = 14,4$ V; $R_L = 2$ $\Omega$ (note 1)	$P_O$	typ. 6,4 W
$V_P = 14,4$ V; $R_L = 4$ $\Omega$ (note 1 and 2)	$P_O$	{ > 5,9 W typ. 6,2 W
$V_P = 14,4$ V; $R_L = 8$ $\Omega$ (note 1)	$P_O$	typ. 3,4 W
$V_P = 14,4$ V; $R_L = 4$ $\Omega$ ; without bootstrap	$P_O$	typ. 5,7 W
$V_P = 14,4$ V; $R_L = 2$ $\Omega$ ; with additional bootstrap resistor of 220 $\Omega$ between pins 3 and 4	$P_O$	typ. 9 W
Voltage gain preamplifier (note 3)	$G_{V1}$	typ. 24 dB 21 to 27 dB
power amplifier	$G_{V2}$	typ. 30 dB 27 to 33 dB
total amplifier	$G_{Vtot}$	typ. 54 dB 51 to 57 dB
Total harmonic distortion at $P_O = 1$ W	$d_{tot}$	typ. 0,2 %
Efficiency at $P_O = 6$ W	$\eta$	typ. 75 %
Frequency response (-3 dB)	B	80 Hz to 15 kHz
Input impedance preamplifier (note 4)	$ Z_i $	typ. 30 k $\Omega$ 20 to 40 k $\Omega$
power amplifier (note 5)	$ Z_i $	typ. 20 k $\Omega$ 14 to 26 k $\Omega$
Output impedance of preamplifier; pin 7 (note 5)	$ Z_o $	typ. 20 k $\Omega$ 14 to 26 k $\Omega$
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (pin 7) (note 3)	$V_{O(rms)}$	> 0,7 V
Noise output voltage (r.m.s. value; note 6) $R_S = 0$ $\Omega$	$V_{n(rms)}$	typ. 0,3 mV
$R_S = 8,2$ k $\Omega$	$V_{n(rms)}$	typ. 0,7 mV < 1,4 mV
Ripple rejection at $f = 1$ kHz to 10 kHz (note 7) at $f = 100$ Hz; $C_2 = 1$ $\mu$ F	RR	> 42 dB > 37 dB
Sensitivity for $P_O = 5,8$ W	$V_i$	typ. 10 mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_4(rms)$	typ. 30 mA



Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to  $P_O \leq 3 \text{ W}$  :  $d_{\text{tot}} \leq 1\%$ .
3. Measured with a load impedance of  $20 \text{ k}\Omega$ .
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ( $|Z_O|$ ) is correlated (within 10%) with the input impedance ( $|Z_i|$ ) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and  $2 \text{ k}\Omega$  (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

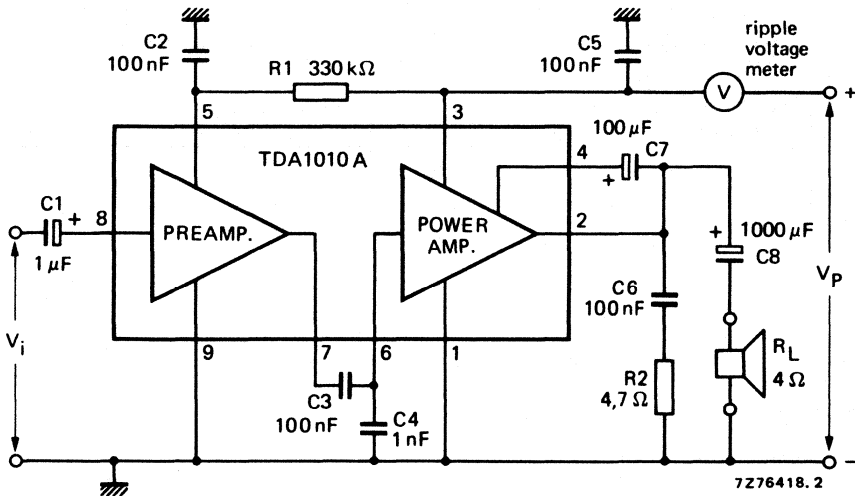


Fig. 3 Test circuit.



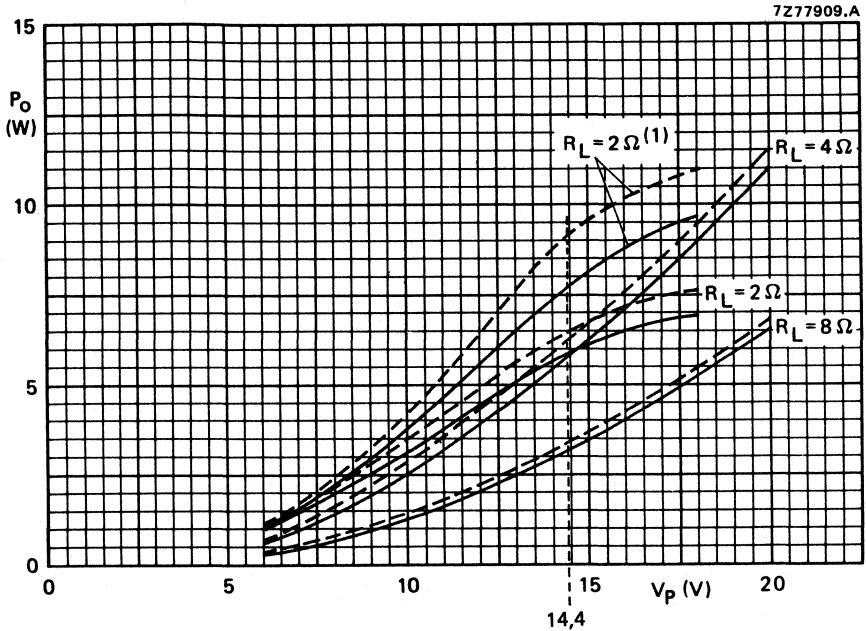


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010.  $R_L = 2\Omega^{(1)}$  has been measured with an additional  $220\Omega$  bootstrap resistor between pins 3 and 4. Measurements were made at  $f = 1\text{ kHz}$ ,  $d_{tot} = 10\%$ ,  $T_{amb} = 25^\circ\text{C}$ .

Fig. 5 See next page.

Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010.  $R_L = 2\Omega^{(1)}$  has been measured with an additional  $220\Omega$  bootstrap resistor between pins 3 and 4. Measurements were made at  $f = 1\text{ kHz}$ ,  $V_p = 14,4\text{ V}$ .





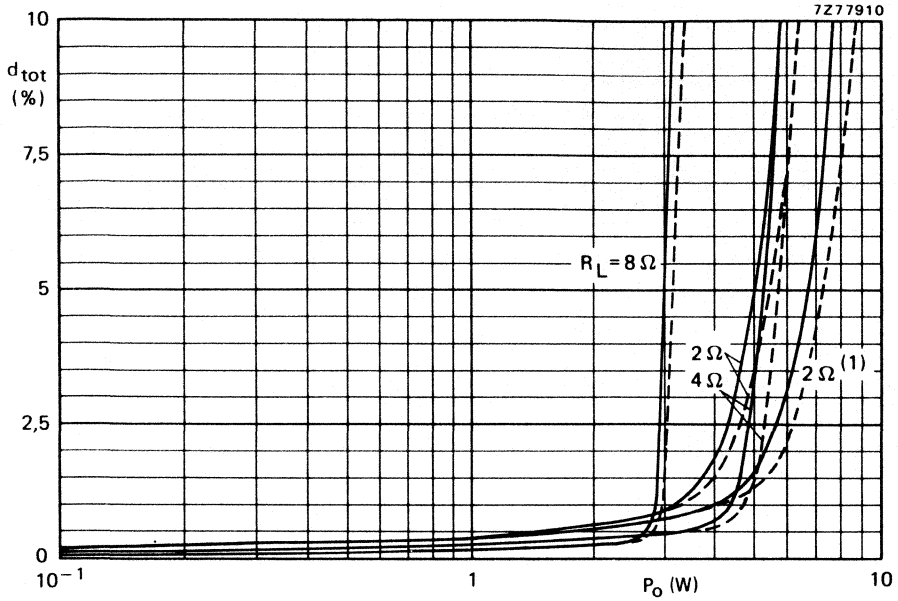


Fig. 5 For caption see preceding page.

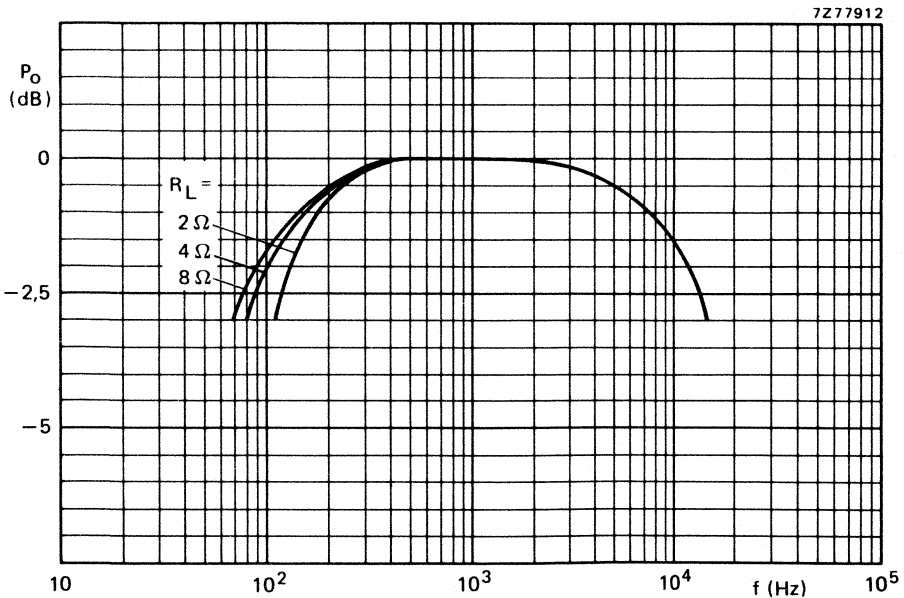


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values.  $P_o$  relative to 0 dB = 1 W;  $V_p = 14,4$  V.



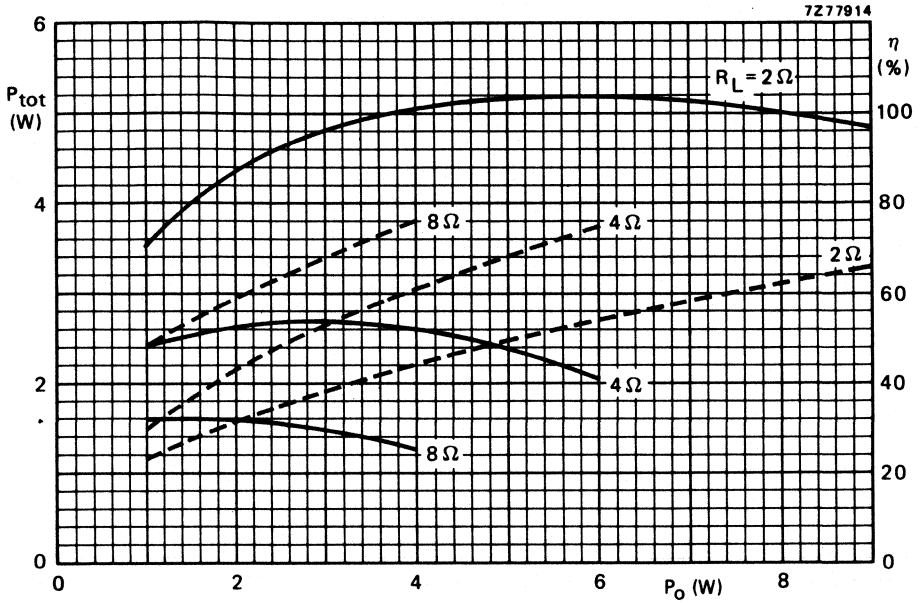


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for  $R_L = 2\ \Omega$  an external bootstrap resistor of  $220\ \Omega$  has been used); typical values.  $V_p = 14,4\ \text{V}$ ;  $f = 1\ \text{kHz}$ .



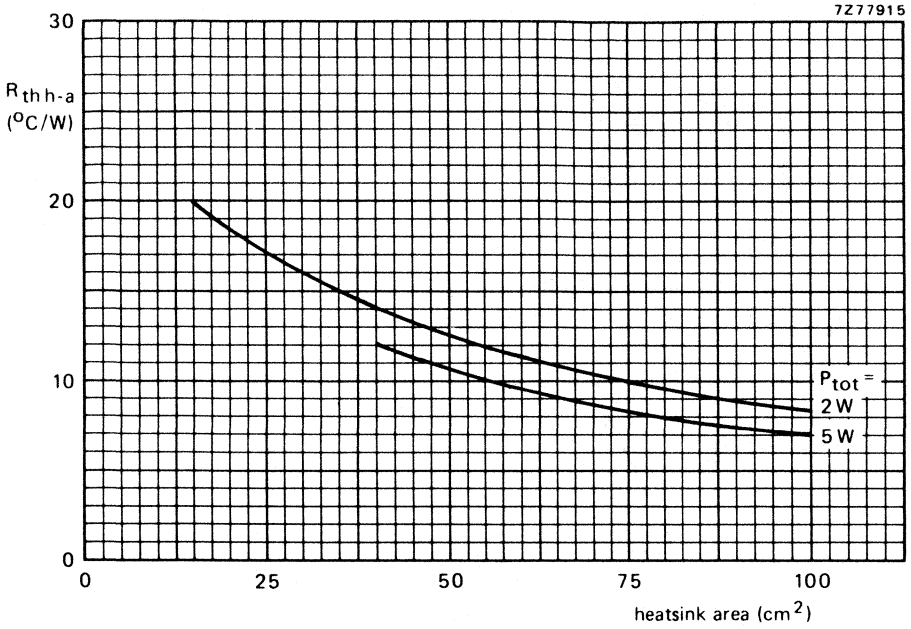


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.



APPLICATION INFORMATION

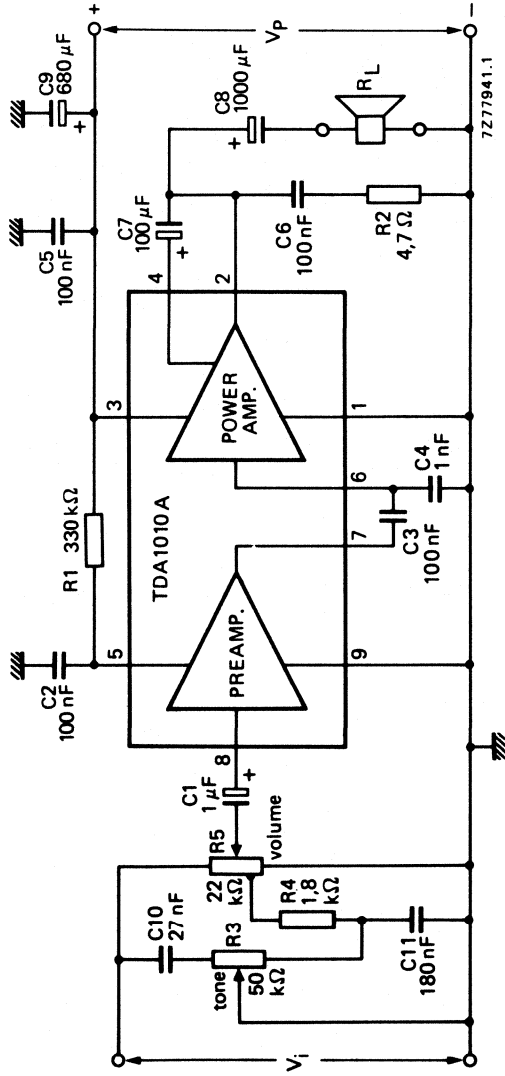
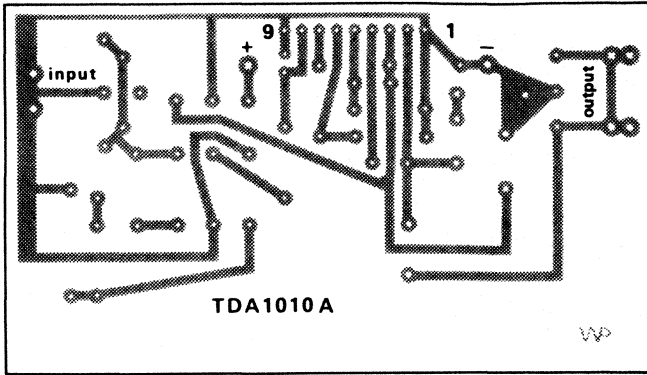


Fig. 9 Complete mono audio amplifier of a car radio.



7Z77931

Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

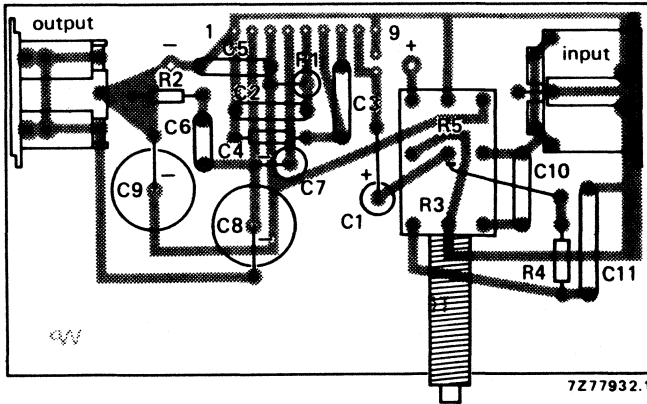


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

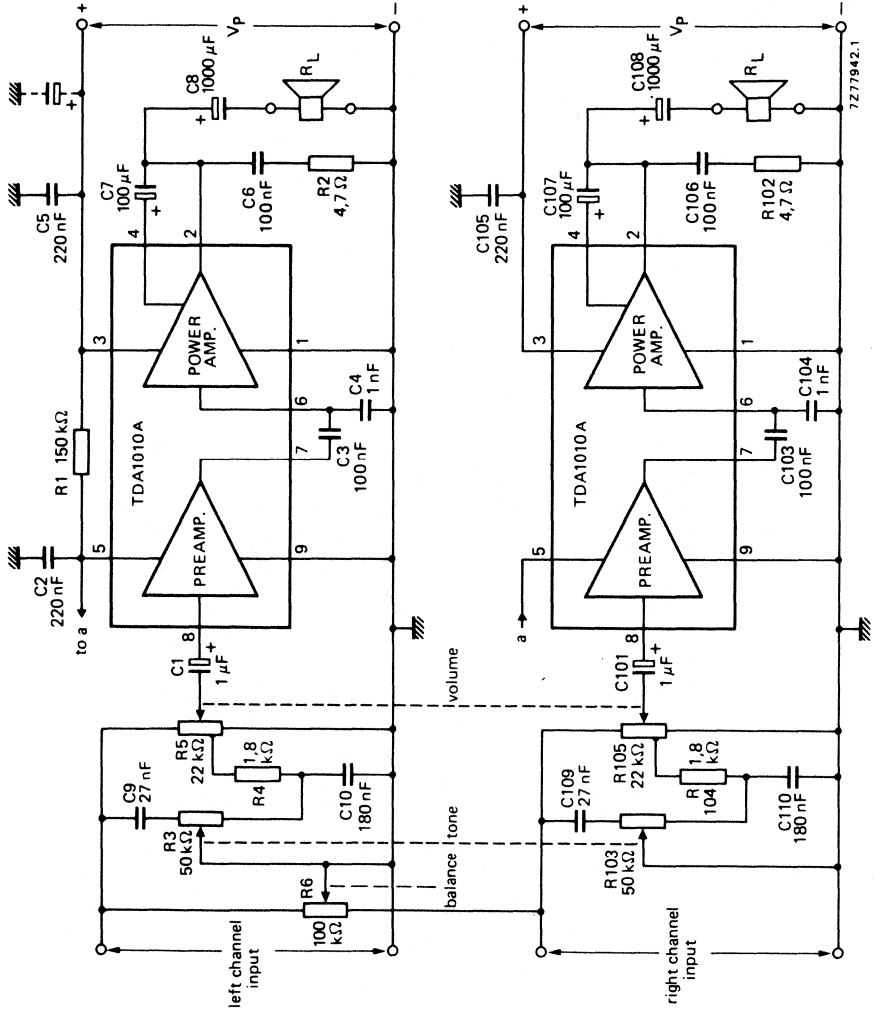


Fig. 12 Complete stereo car radio amplifier.

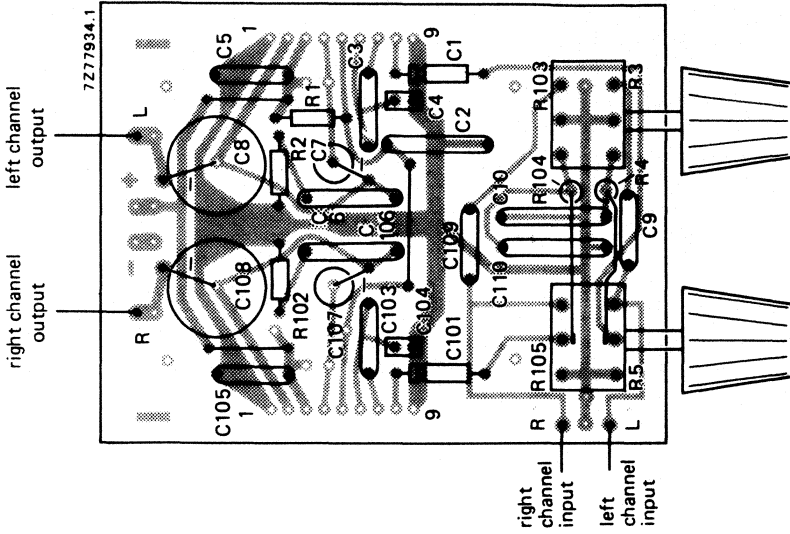


Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

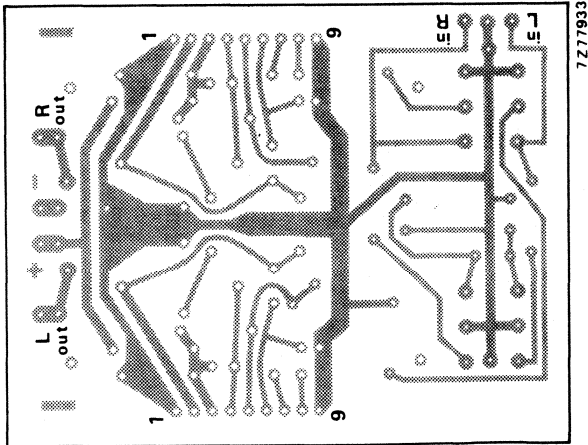


Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.



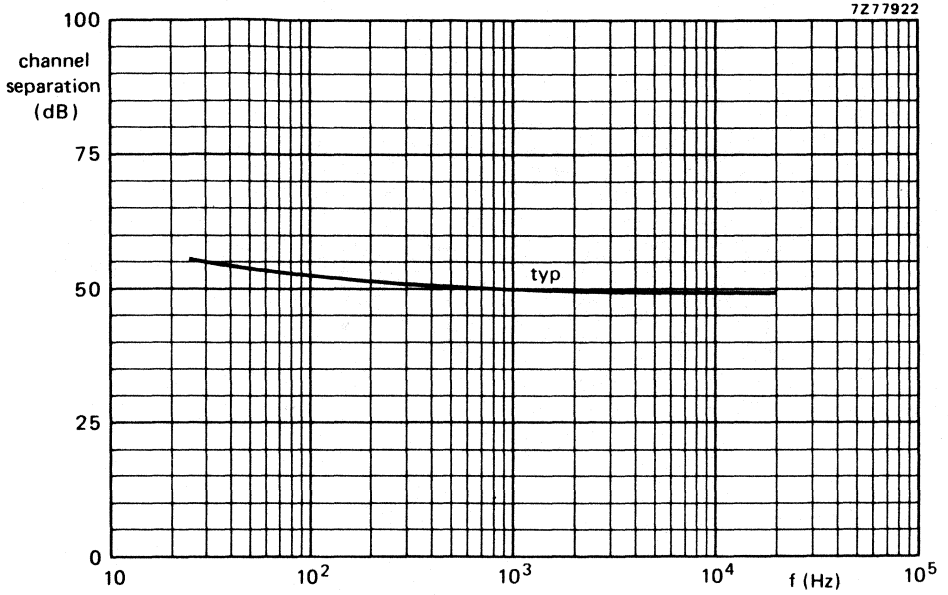


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

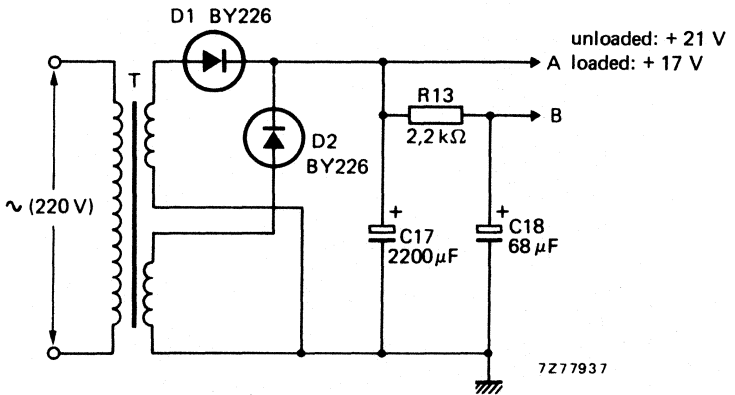


Fig. 16 Power supply of circuit of Fig. 17.



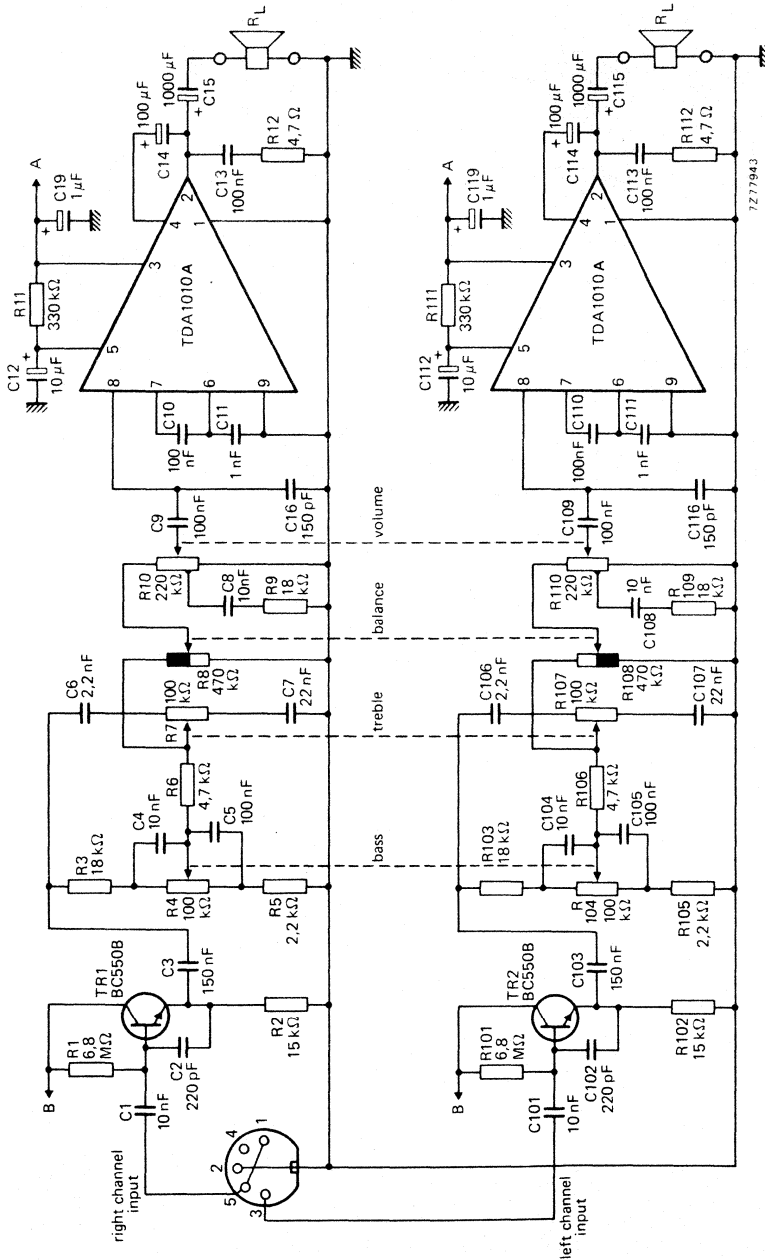


Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.



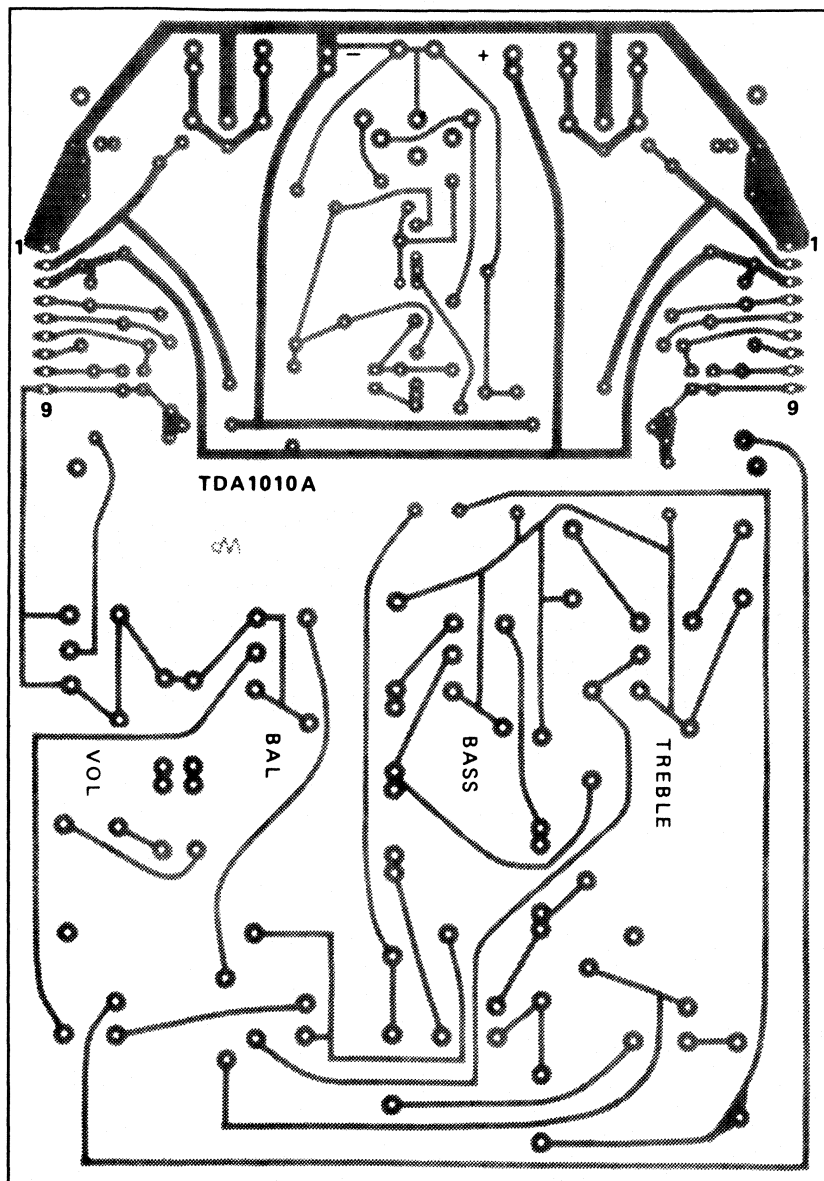


Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

7277935

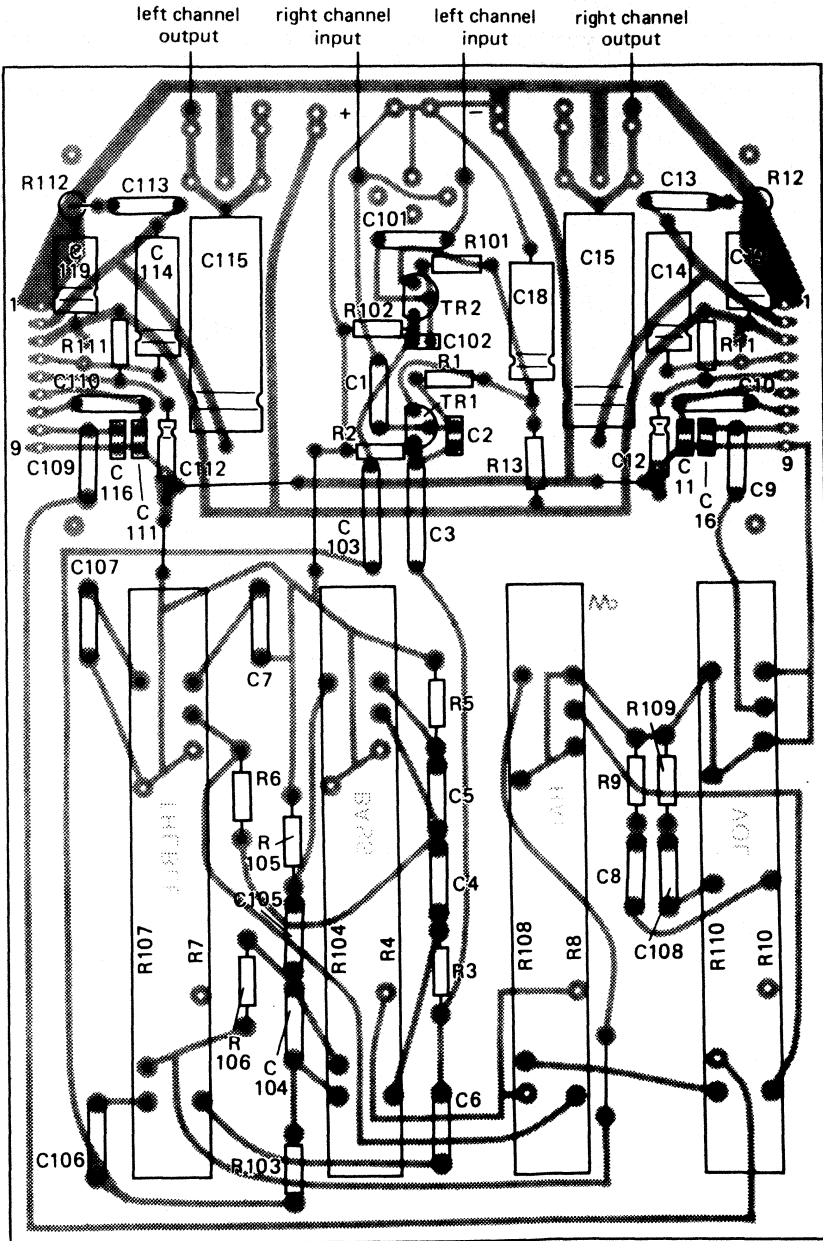


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

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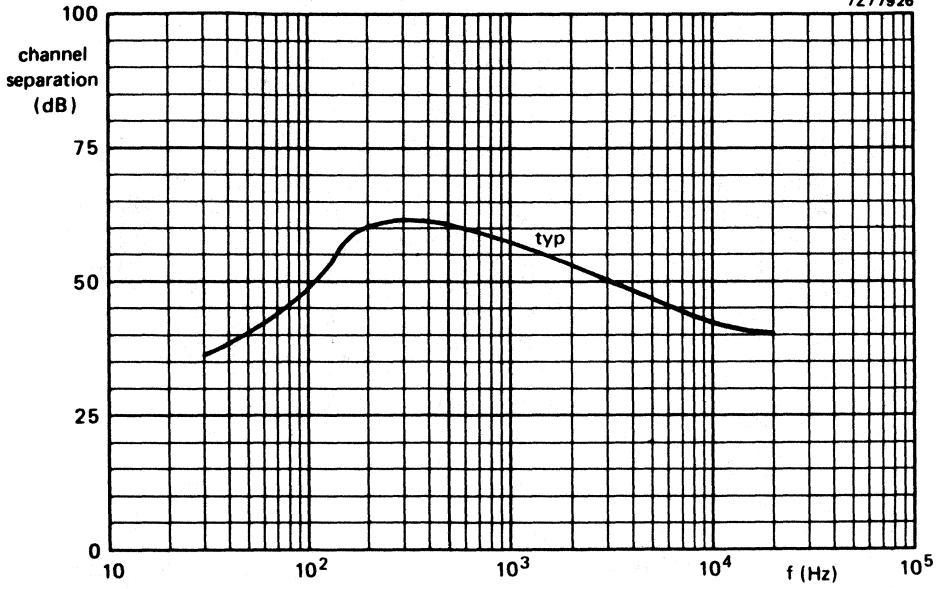


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.



## 2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a  $4 \Omega$  load impedance. The device can deliver up to 6 W into  $4 \Omega$  at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

### QUICK REFERENCE DATA

Supply voltage range	$V_p$	3,6 to 20 V
Peak output current	$I_{OM}$	max. 3 A
Output power at $d_{tot} = 10\%$		
$V_p = 16 \text{ V}; R_L = 4 \Omega$	$P_o$	typ. 6,5 W
$V_p = 12 \text{ V}; R_L = 4 \Omega$	$P_o$	typ. 4,2 W
$V_p = 9 \text{ V}; R_L = 4 \Omega$	$P_o$	typ. 2,3 W
$V_p = 6 \text{ V}; R_L = 4 \Omega$	$P_o$	typ. 1,0 W
Total harmonic distortion at $P_o = 1 \text{ W}; R_L = 4 \Omega$	$d_{tot}$	typ. 0,2 %
Input impedance		
preamplifier (pin 8)	$ Z_i $	> 100 k $\Omega$
power amplifier (pin 6)	$ Z_i $	typ. 20 k $\Omega$
Total quiescent current	$I_{tot}$	typ. 14 mA
Operating ambient temperature	$T_{amb}$	-25 to + 150 °C
Storage temperature	$T_{stg}$	-55 to + 150 °C

### PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

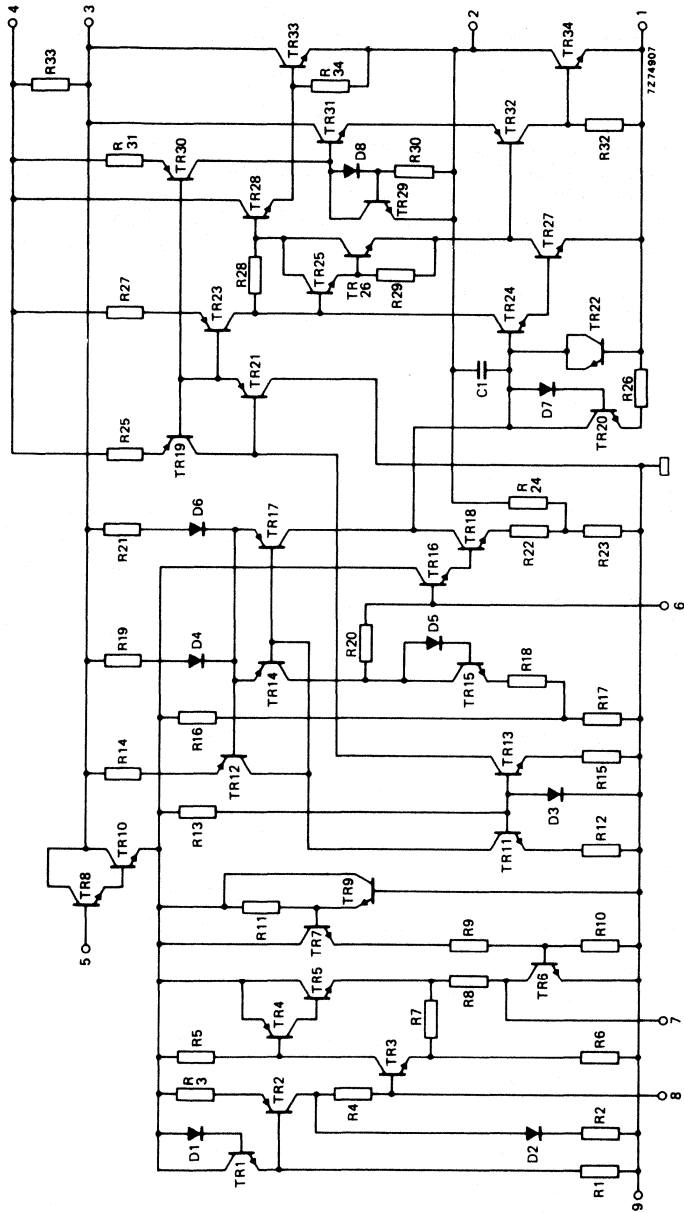


Fig. 1 Circuit diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P$	max.	24 V
Peak output current	$I_{OM}$	max.	3 A
Total power dissipation			see derating curve Fig. 2
Storage temperature	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature	$T_{amb}$		-25 to + 150 °C
A.C. short-circuit duration of load during sine-wave drive; $V_P = 12 V$	$t_{sc}$	max.	100 hours

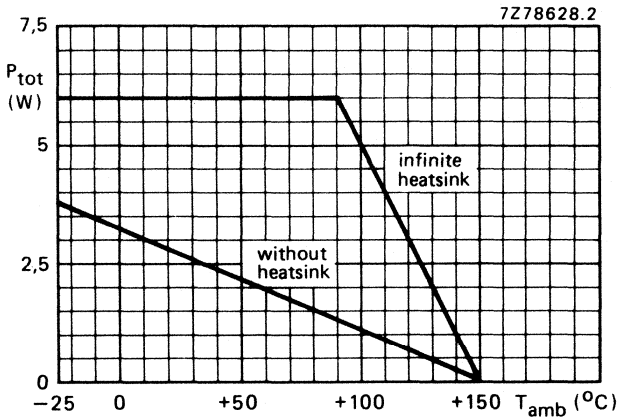


Fig. 2 Power derating curve.

**HEATSINK DESIGN**

Assume  $V_P = 12 V$ ;  $R_L = 4 \Omega$ ;  $T_{amb} = 60 \text{ }^\circ\text{C}$  maximum;  $P_O = 3,8 W$ .

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th j-a} = R_{th j-tab} + R_{th tab-h} + R_{th h-a} = \frac{150 - 60}{1,8} = 50 \text{ K/W.}$$

Since  $R_{th j-tab} = 10 \text{ K/W}$  and  $R_{th tab-h} = 1 \text{ K/W}$ ,  $R_{th h-a} = 50 - (10 + 1) = 39 \text{ K/W}$ .



**D.C. CHARACTERISTICS**

Supply voltage range	$V_p$	3,6 to 20 V
Repetitive peak output current	$I_{ORM}$	< 2 A
Total quiescent current at $V_p = 12$ V	$I_{tot}$	typ. 14 mA < 22 mA

**A.C. CHARACTERISTICS**

$T_{amb} = 25$  °C;  $V_p = 12$  V;  $R_L = 4$   $\Omega$ ;  $f = 1$  kHz unless otherwise specified; see also Fig. 3.

A.F. output power at  $d_{tot} = 10\%$  (note 1)

with bootstrap:

$V_p = 16$  V;  $R_L = 4$   $\Omega$

$P_o$  typ. 6,5 W

$V_p = 12$  V;  $R_L = 4$   $\Omega$

$P_o$  > 3,6 W  
typ. 4,2 W

$V_p = 9$  V;  $R_L = 4$   $\Omega$

$P_o$  typ. 2,3 W

$V_p = 6$  V;  $R_L = 4$   $\Omega$

$P_o$  typ. 1,0 W

without bootstrap:

$V_p = 12$  V;  $R_L = 4$   $\Omega$

$P_o$  typ. 3,0 W

Voltage gain:

preamplifier (note 2)

$G_{v1}$  typ. 23 dB  
21 to 25 dB

power amplifier

$G_{v2}$  typ. 29 dB  
27 to 31 dB

total amplifier

$G_{v\ tot}$  typ. 52 dB  
50 to 54 dB

Total harmonic distortion at  $P_o = 1,5$  W

$d_{tot}$  typ. 0,3 %  
< 1 %

Frequency response; -3 dB (note 3)

B 60 Hz to 15 kHz

Input impedance:

preamplifier (note 4)

$|Z_{i1}|$  > 100 k $\Omega$   
typ. 200 k $\Omega$

power amplifier

$|Z_{i2}|$  typ. 20 k $\Omega$

Output impedance preamplifier

$|Z_{o1}|$  typ. 1 k $\Omega$

Output voltage preamplifier (r.m.s. value)

$d_{tot} < 1\%$  (note 2)

$V_o(rms)$  > 0,7 V

Noise output voltage (r.m.s. value; note 5)

$R_S = 0$   $\Omega$

$V_n(rms)$  typ. 0,2 mV

$R_S = 10$  k $\Omega$

$V_n(rms)$  typ. 0,6 mV  
< 1,4 mV

Noise output voltage at  $f = 500$  kHz (r.m.s. value)

B = 5 kHz;  $R_S = 0$   $\Omega$

$V_n(rms)$  typ. 8  $\mu$ V

Ripple rejection (note 6)

$f = 1$  to 10 kHz

RR typ. 42 dB

$f = 100$  Hz;  $C_2 = 1$   $\mu$ F

RR > 35 dB

Bootstrap current at onset of clipping; pin 4 (r.m.s. value)

$I_4(rms)$  typ. 35 mA



Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at  $P_O = 1\text{ W}$ ; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

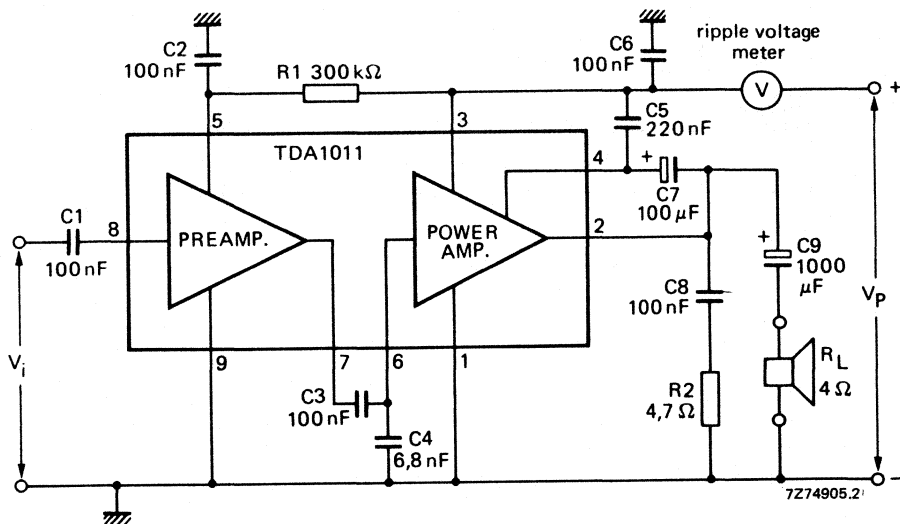


Fig. 3 Test circuit.



APPLICATION INFORMATION

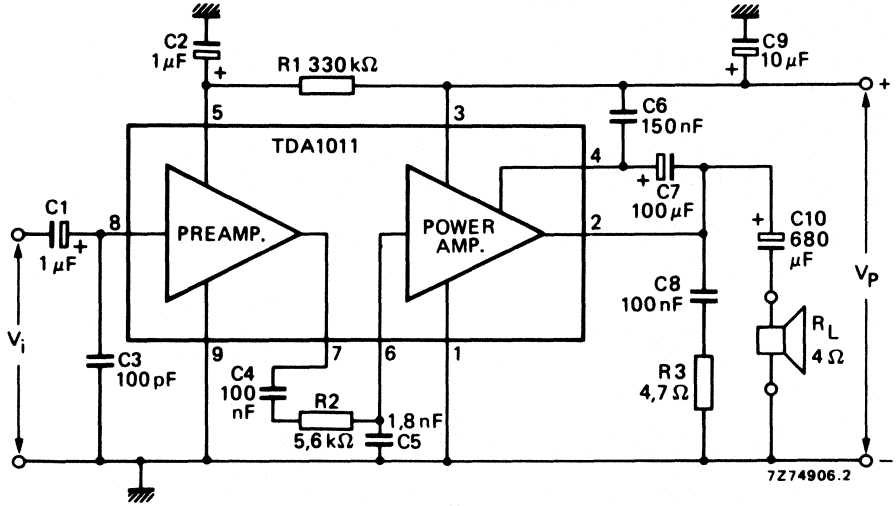


Fig. 4 Circuit diagram of a 4 W amplifier.

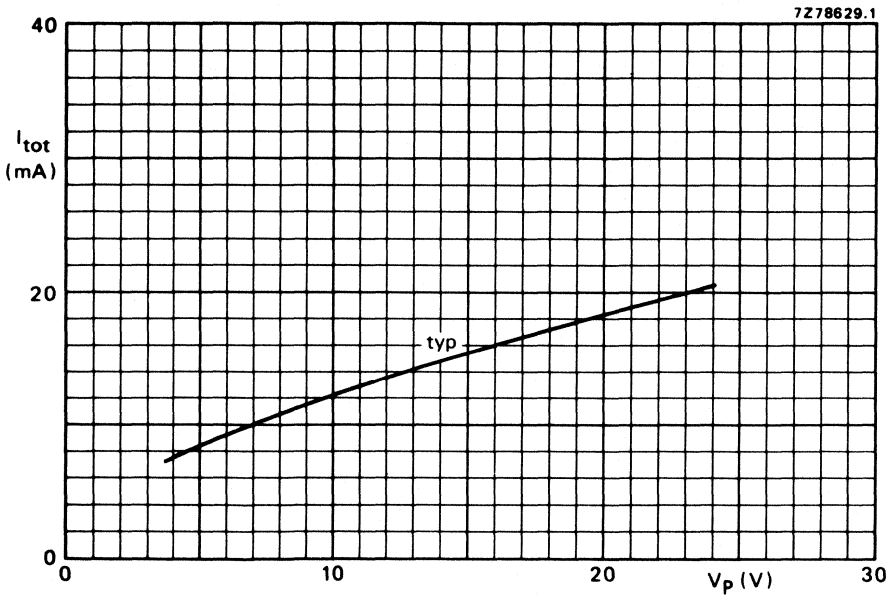


Fig. 5 Total quiescent current as a function of supply voltage.

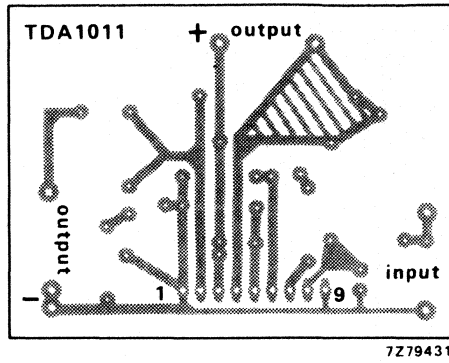


Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4; p.c. board dimensions 62 mm x 48 mm.

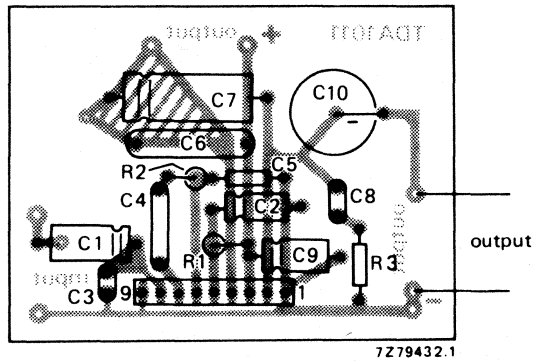


Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

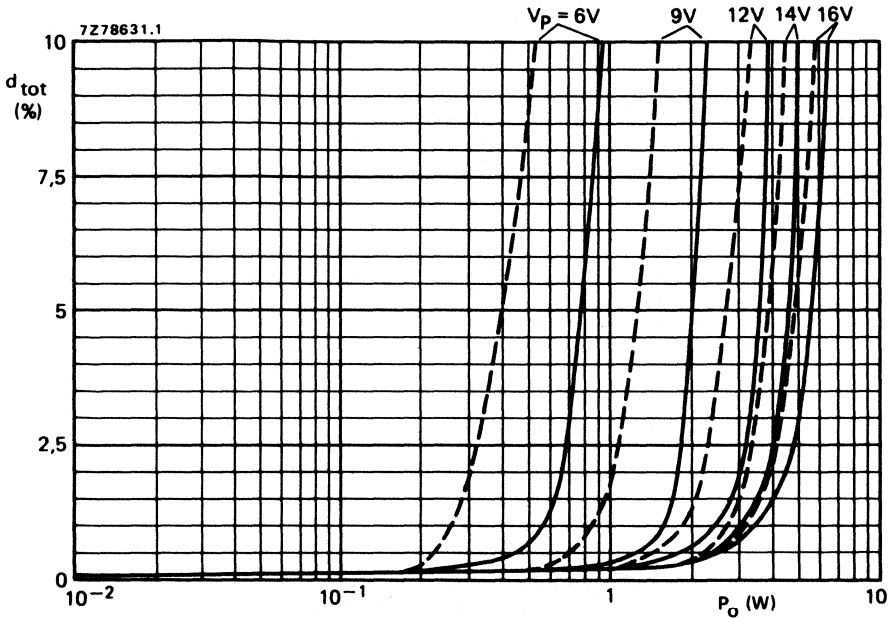


Fig. 8 Total harmonic distortion as a function of output power across  $R_L$ ; — with bootstrap; - - - without bootstrap;  $f = 1$  kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

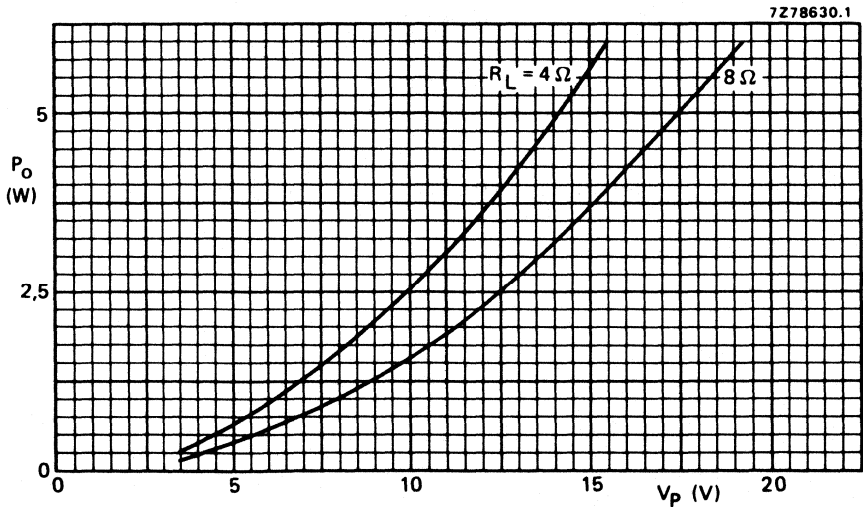


Fig. 9 Output power across  $R_L$  as a function of supply voltage with bootstrap;  $d_{tot} = 10\%$ ; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

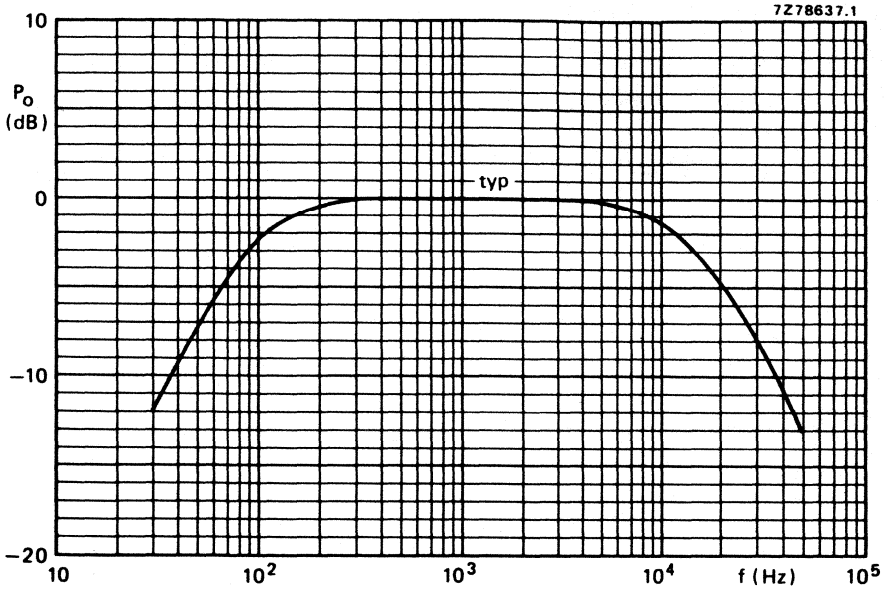


Fig. 10 Voltage gain as a function of frequency;  $P_o$  relative to 0 dB = 1 W;  $V_p = 12$  V;  $R_L = 4 \Omega$ .

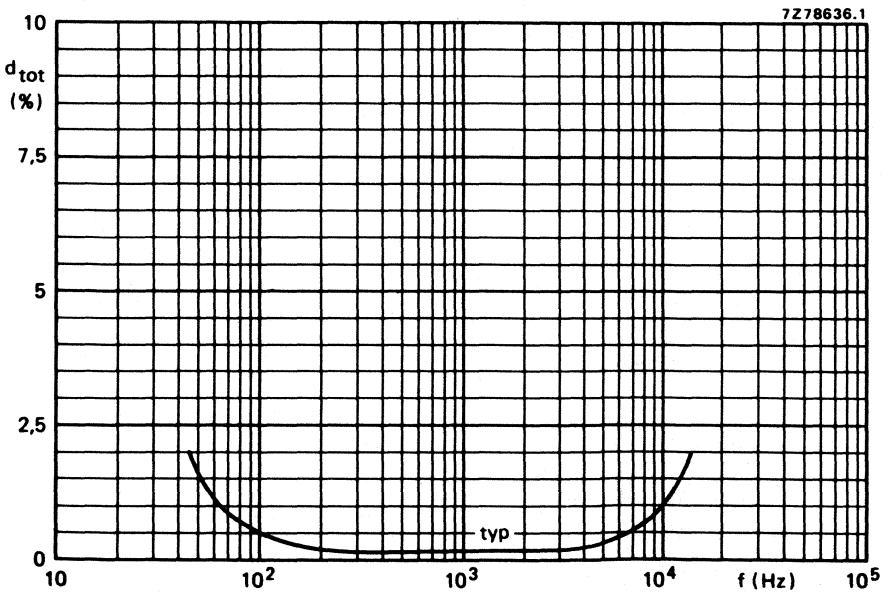


Fig. 11 Total harmonic distortion as a function of frequency;  $P_o = 1$  W;  $V_p = 12$  V;  $R_L = 4 \Omega$ .

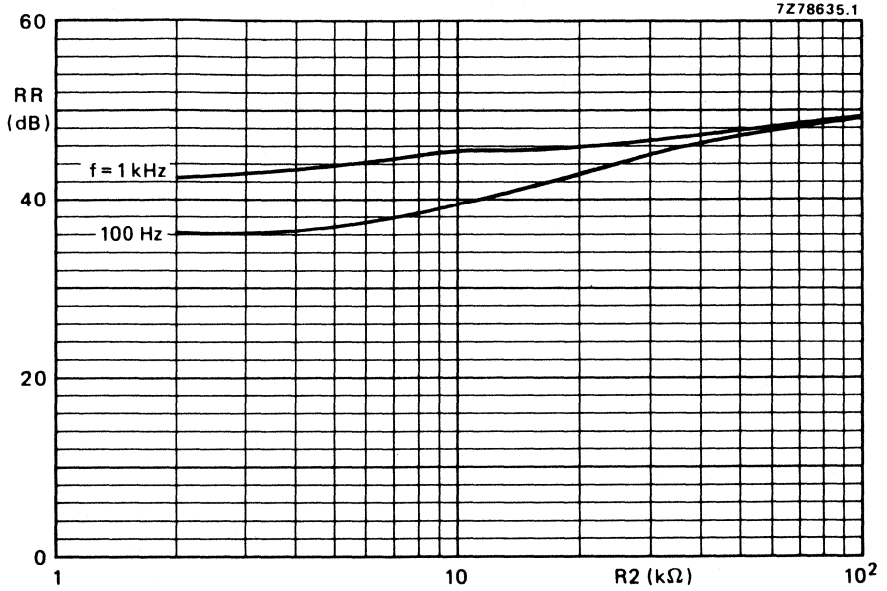


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4);  $R_S = 0$ ; typical values.

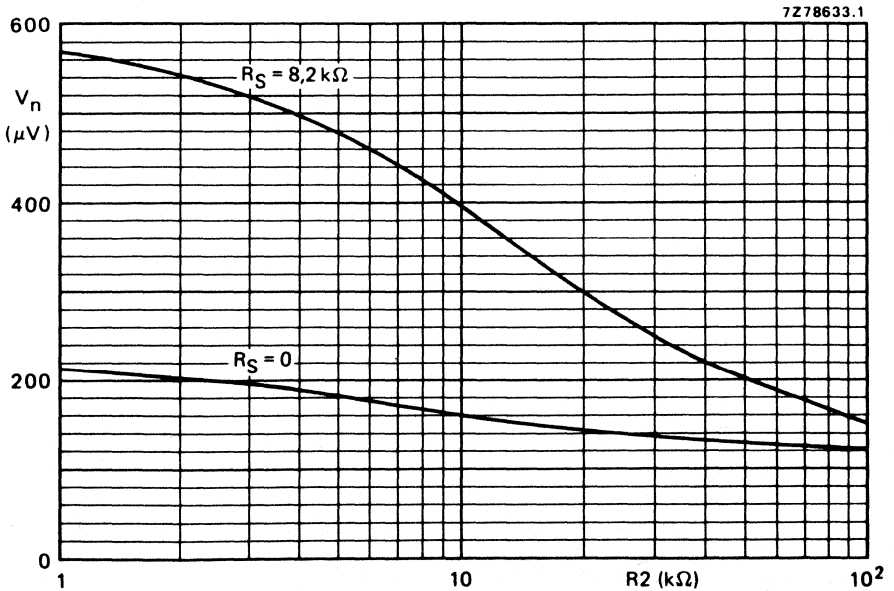


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

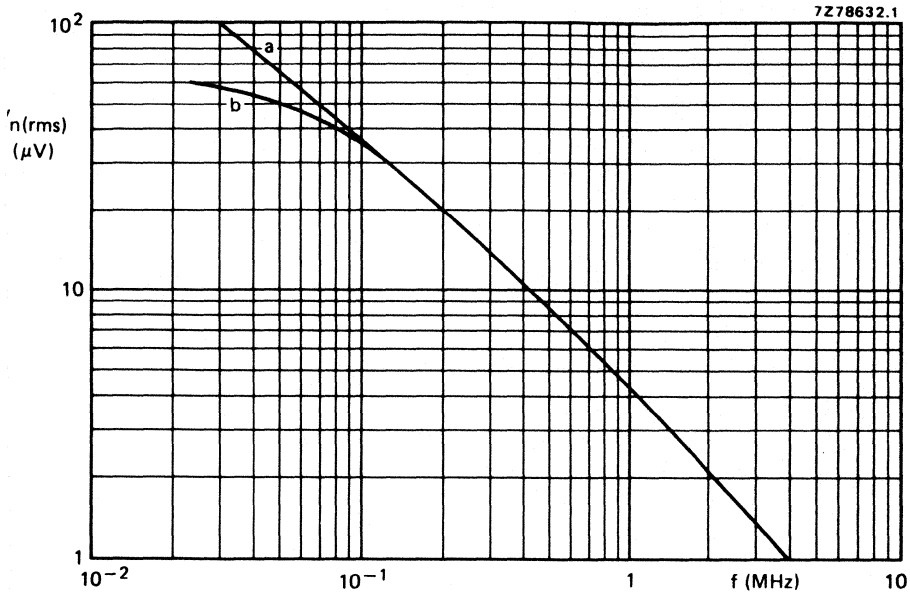


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier;  $B = 5$  kHz;  $R_S = 0$ ; typical values.

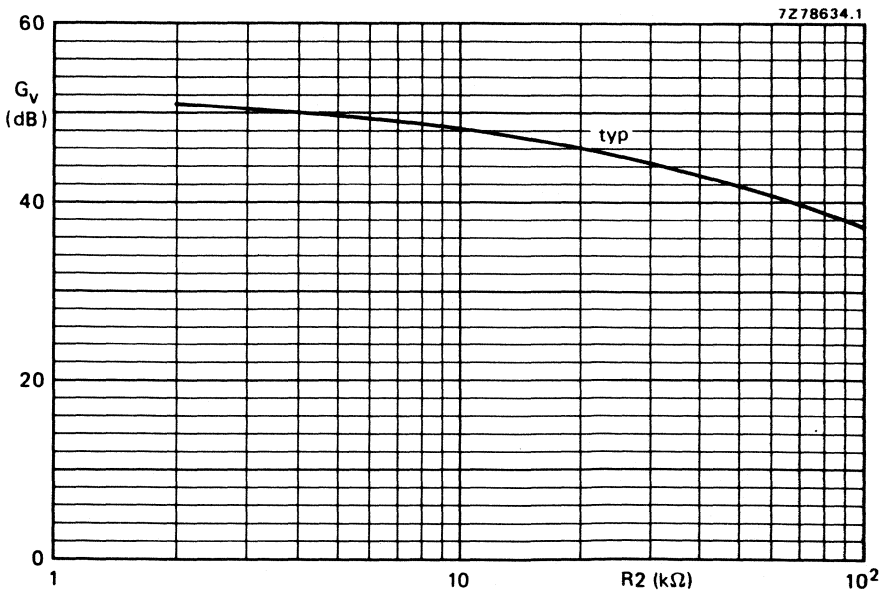


Fig. 15 Voltage gain as a function of  $R_2$  (see Fig. 4).







## 2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011A is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4  $\Omega$  load impedance. The device can deliver up to 6 W into 4  $\Omega$  at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the low applicable supply voltage of 5,4 V permits 9 V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

### QUICK REFERENCE DATA

Supply voltage range	$V_P$	5,4 to 20 V
Peak output current	$I_{OM}$	max. 3 A
Output power at $d_{tot} = 10\%$		
$V_P = 16$ V; $R_L = 4$ $\Omega$	$P_O$	typ. 6,5 W
$V_P = 12$ V; $R_L = 4$ $\Omega$	$P_O$	typ. 4,2 W
$V_P = 9$ V; $R_L = 4$ $\Omega$	$P_O$	typ. 2,3 W
$V_P = 6$ V; $R_L = 4$ $\Omega$	$P_O$	typ. 1,0 W
Total harmonic distortion at $P_O = 1$ W; $R_L = 4$ $\Omega$	$d_{tot}$	typ. 0,2 %
Input impedance preamplifier (pin 8)	$ Z_i $	> 100 k $\Omega$
Total quiescent current	$I_{tot}$	typ. 14 mA
Operating ambient temperature	$T_{amb}$	-25 to + 150 $^{\circ}$ C
Storage temperature	$T_{stg}$	-55 to + 150 $^{\circ}$ C



### PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

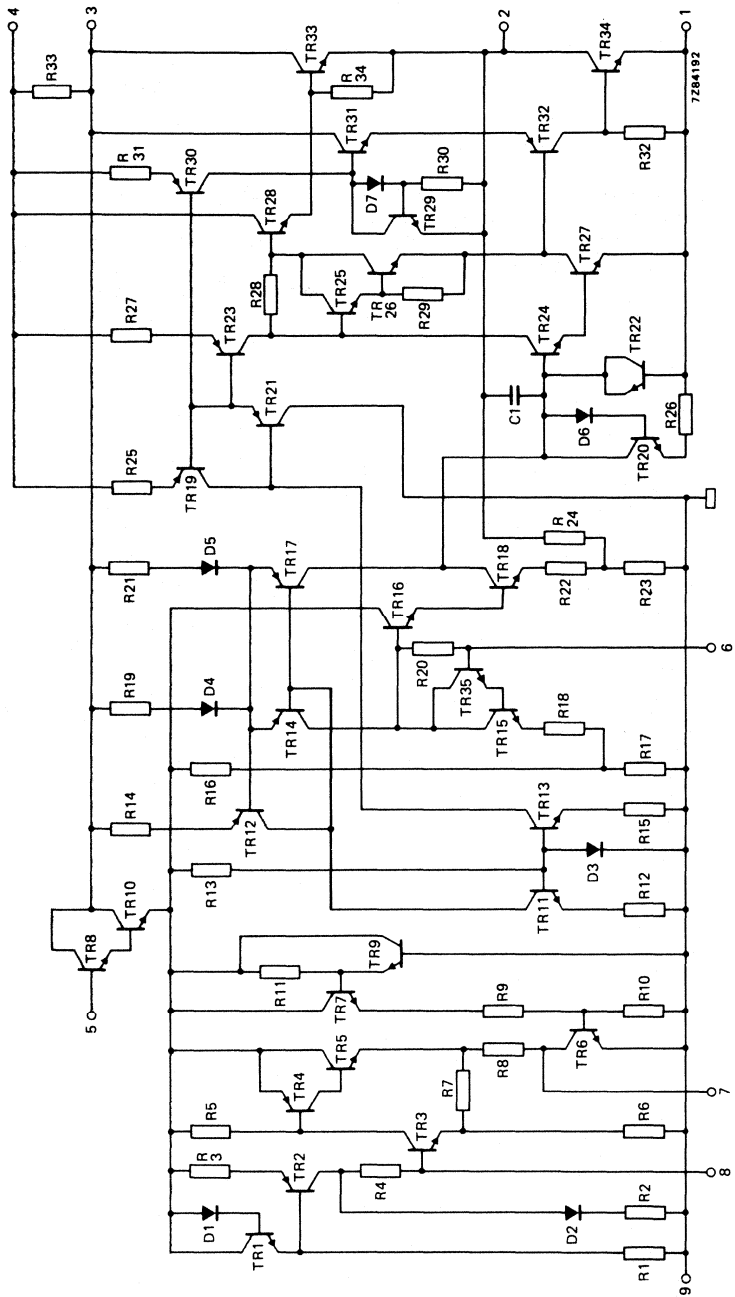


Fig. 1 Circuit diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P$	max.	24 V
Peak output current	$I_{OM}$	max.	3 A
Total power dissipation			see derating curve Fig. 2
Storage temperature	$T_{stg}$		-55 to +150 °C
Operating ambient temperature	$T_{amb}$		-25 to +150 °C
A.C. short-circuit duration of load during sine-wave drive; $V_P = 12$ V	$t_{sc}$	max.	100 hours

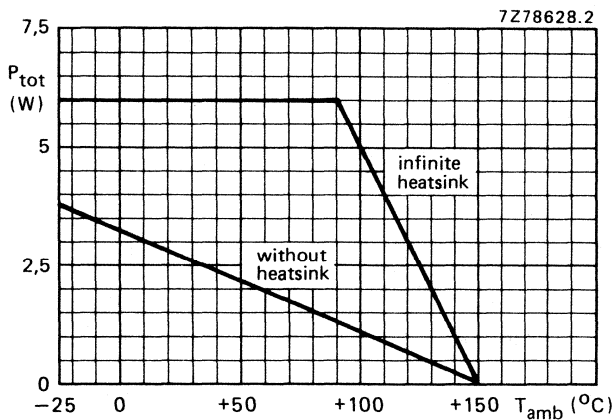


Fig. 2 Power derating curve.

**HEATSINK DESIGN**Assume  $V_P = 12$  V;  $R_L = 4 \Omega$ ;  $T_{amb} = 60$  °C maximum;  $P_O = 3,8$  W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th j-a} = R_{th j-tab} + R_{th tab-h} + R_{th h-a} = \frac{150 - 60}{1,8} = 50 \text{ K/W.}$$

Since  $R_{th j-tab} = 10$  K/W and  $R_{th tab-h} = 1$  K/W,  $R_{th h-a} = 50 - (10 + 1) = 39$  K/W.

**D.C. CHARACTERISTICS**

Supply voltage range	$V_P$	5,4 to 20 V
Repetitive peak output current	$I_{ORM}$	< 2 A
Total quiescent current at $V_P = 12$ V	$I_{tot}$	typ. 14 mA < 22 mA

**A.C. CHARACTERISTICS**

$T_{amb} = 25$  °C;  $V_P = 12$  V;  $R_L = 4$   $\Omega$ ;  $f = 1$  kHz unless otherwise specified; see also Fig. 3.

**A.F. output power at  $d_{tot} = 10\%$  (note 1)**

with bootstrap:

$V_P = 16$  V;  $R_L = 4$   $\Omega$   $P_O$  typ. 6,5 W

$V_P = 12$  V;  $R_L = 4$   $\Omega$   $P_O$  > 3,6 W

$V_P = 9$  V;  $R_L = 4$   $\Omega$   $P_O$  typ. 4,2 W

$V_P = 6$  V;  $R_L = 4$   $\Omega$   $P_O$  typ. 2,3 W

$V_P = 6$  V;  $R_L = 4$   $\Omega$   $P_O$  typ. 1,0 W

without bootstrap:

$V_P = 12$  V;  $R_L = 4$   $\Omega$   $P_O$  typ. 3,5 W

**Voltage gain:**

preamplifier (note 2)  $G_{v1}$  typ. 23 dB

power amplifier (note 3) 21 to 25 dB

total amplifier (note 3)  $G_{v2}$  typ. 29 dB

total amplifier (note 3)  $G_{v\ tot}$  typ. 52 dB

**Total harmonic distortion at  $P_O = 1,5$  W**

$d_{tot}$  typ. 0,3 %

$d_{tot}$  < 1 %

**Frequency response; -3 dB (note 4)**

B 60 Hz to 15 kHz

**Input impedance:**

preamplifier (note 5)  $|Z_{i1}|$  > 100 k $\Omega$

preamplifier (note 5) typ. 200 k $\Omega$

**Output impedance preamplifier**

$|Z_{o1}|$  typ. 1 k $\Omega$

**Output voltage preamplifier (r.m.s. value)**

$d_{tot} < 1\%$  (note 2)  $V_{O(rms)}$  > 1,2 V

**Noise output voltage (r.m.s. value; note 6)**

$R_S = 0$   $\Omega$   $V_{n(rms)}$  typ. 0,5 mV

$R_S = 10$  k $\Omega$   $V_{n(rms)}$  typ. 0,8 mV

**Noise output voltage at  $f = 500$  kHz (r.m.s. value)**

B = 5 kHz;  $R_S = 0$   $\Omega$   $V_{n(rms)}$  typ. 8  $\mu$ V

**Ripple rejection (note 6)**

$f = 1$  to 10 kHz RR typ. 42 dB

$f = 100$  Hz;  $C_2 = 1$   $\mu$ F RR > 35 dB

**Bootstrap current at onset of clipping; pin 4 (r.m.s. value)**

$I_{4(rms)}$  typ. 35 mA

**Stand-by current at maximum  $V_P$  (note 8)**

$I_{sb}$  < 100  $\mu$ A



Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured with R2 = 20 kΩ.
4. Measured at  $P_O = 1 W$ ; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The total current when disconnecting pin 5 or short-circuited to ground (pin 9).
9. The tab must be electrically floating or connected to the substrate (pin 9).

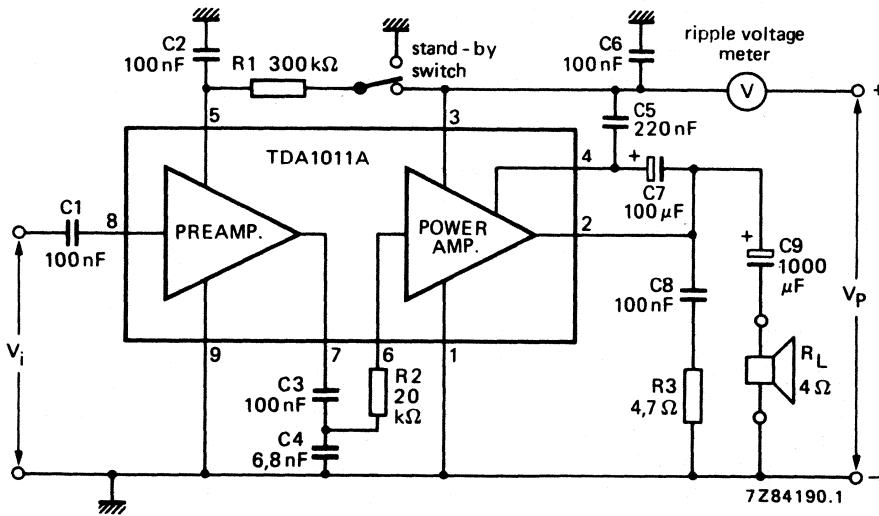


Fig. 3 Test circuit.

APPLICATION INFORMATION

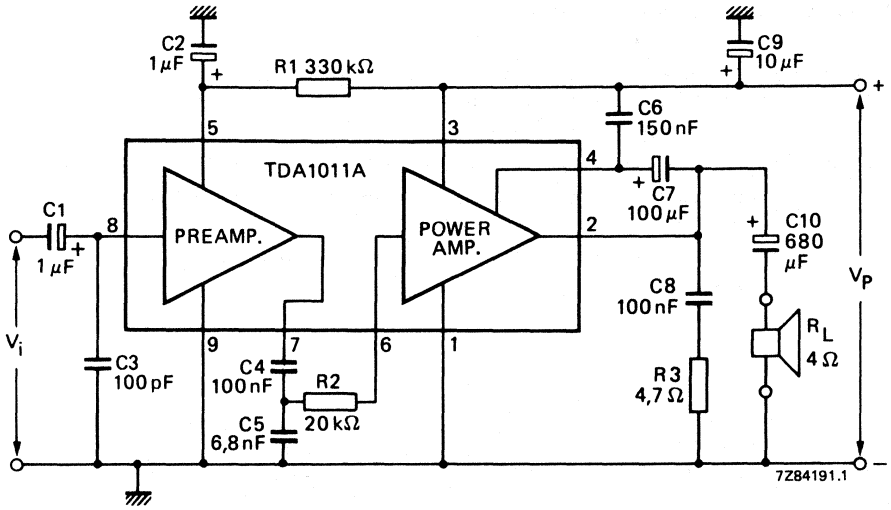


Fig. 4 Circuit diagram of a 4 W amplifier.

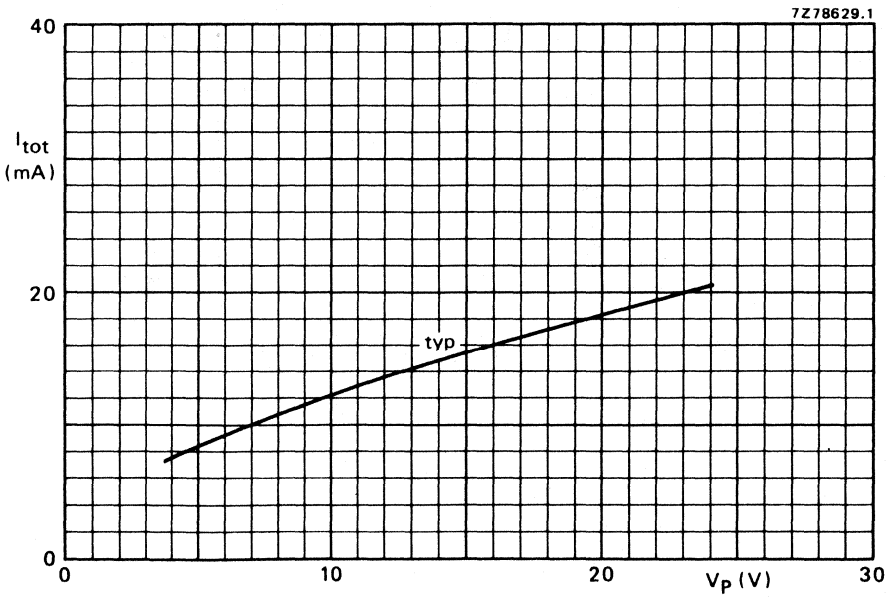


Fig. 5 Total quiescent current as a function of supply voltage.

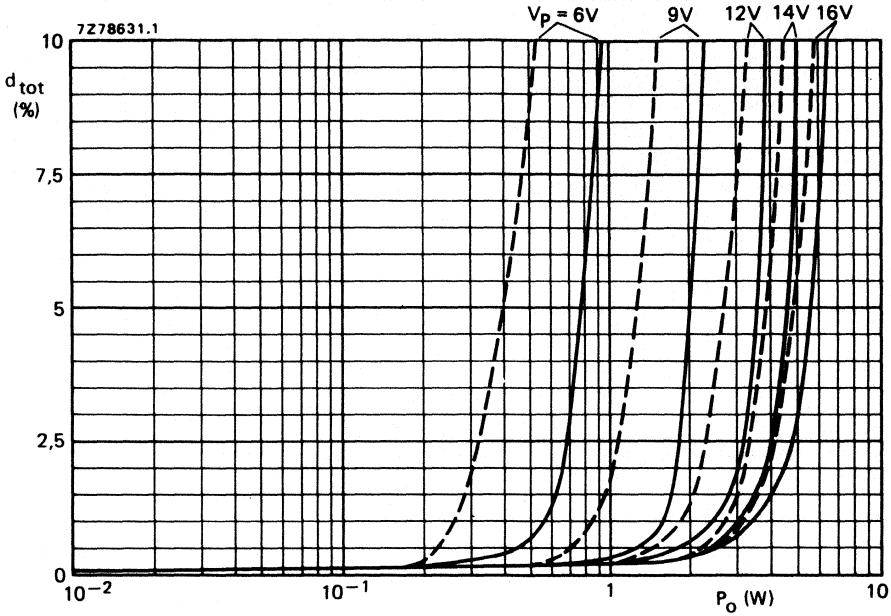


Fig. 6 Total harmonic distortion as a function of output power across  $R_L$ ; — with bootstrap; - - - without bootstrap;  $f = 1$  kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

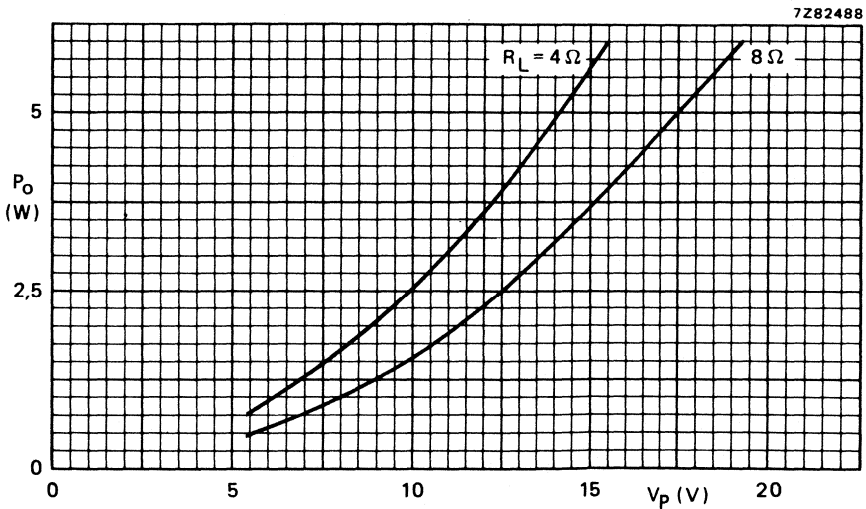


Fig. 7 Output power across  $R_L$  as a function of supply voltage with bootstrap;  $d_{tot} = 10\%$ ; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

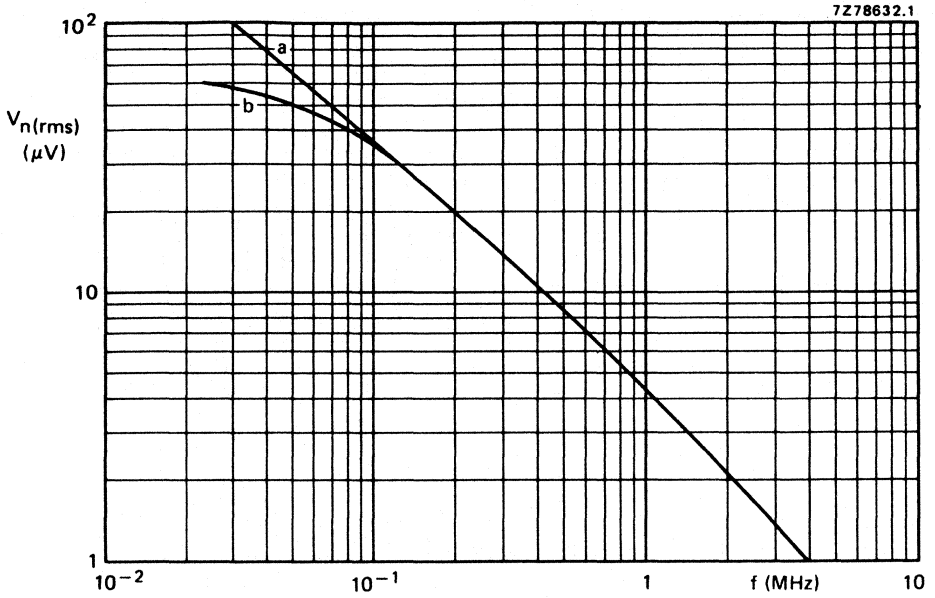


Fig. 8 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier;  $B = 5 \text{ kHz}$ ;  $R_S = 0$ ; typical values.





## RECORDING / PLAY-BACK AND 2 W AUDIO POWER AMPLIFIER

The TDA1012 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit is thermal protected and contains the following functions:

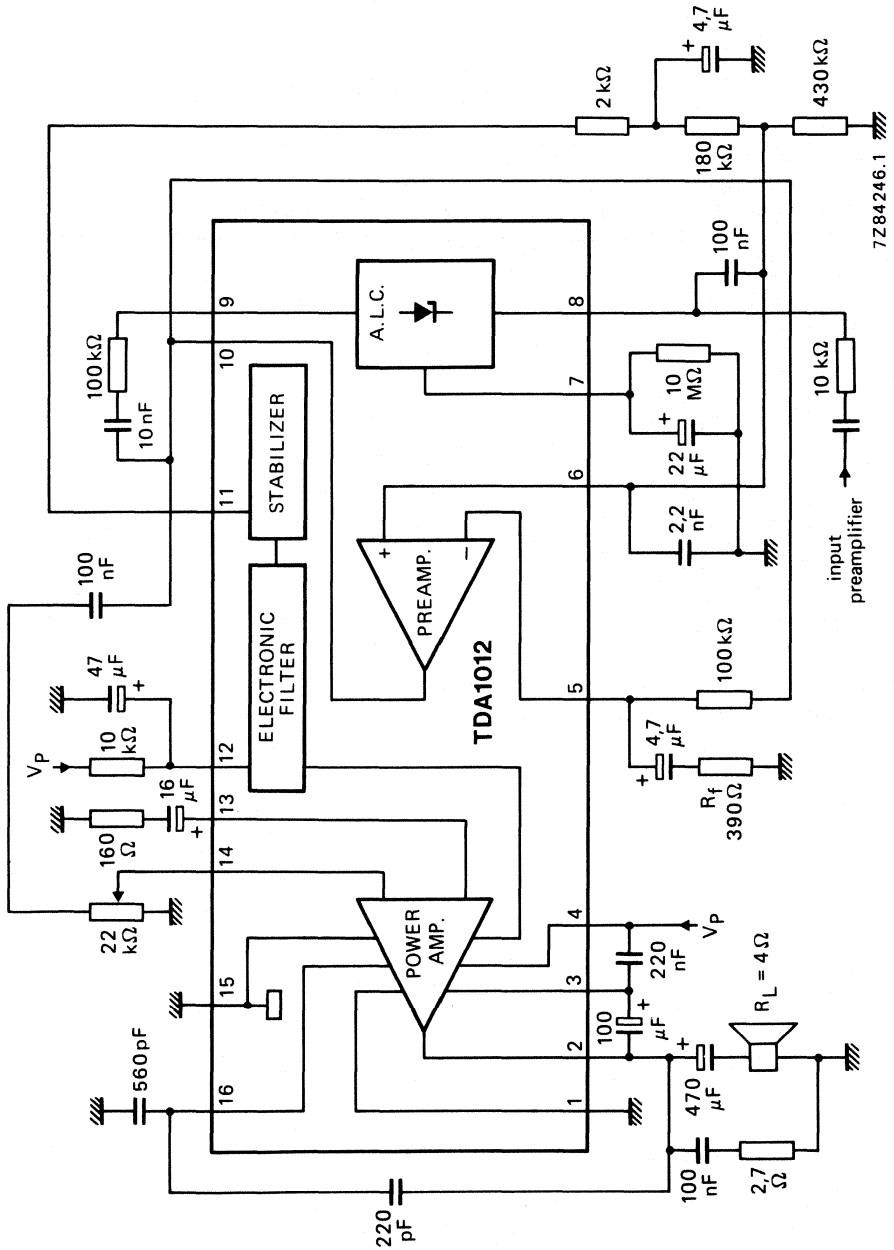
- Power amplifier
- Preamplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer

## QUICK REFERENCE DATA

Supply voltage range	$V_P$		3,6 to 18 V
Total quiescent current at $V_P = 9\text{ V}$	$I_{tot}$	typ.	14 mA
<b>Power amplifier</b>			
Output power at $d_{tot} = 10\%$ $V_P = 9\text{ V}; R_L = 4\ \Omega$	$P_o$	typ.	2 W
Closed loop voltage gain	$G_c$	typ.	36 dB
<b>Preamplifier</b>			
Open loop voltage gain	$G_o$	>	66 dB
Minimum closed loop voltage gain	$G_{c\ min}$		31 dB
Output voltage at $d_{tot} = 1\%$	$V_o$	>	2 V
<b>Automatic Level Control (A.L.C.)</b>			
Gain variation for $\Delta V_i = 40\text{ dB}$	$\Delta G_v$	typ.	2 dB
<b>Stabilized supply voltage</b>			
Output voltage	$V_{11-15}$	typ.	4,2 V

## PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT-38WE-2).



7Z84246.1

Fig. 1 Block diagram/test circuit.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	$V_P = V_{4-1}$	max.	18 V
Non-repetitive peak output current (pin 2)	$I_{OSM}$	max.	2 A
Storage temperature	$T_{stg}$		-55 to +150 °C
Crystal temperature	$T_C$	max.	150 °C
Total power dissipation	see derating curve Fig. 2		
A.C. short-circuit duration of load during sine-wave drive; $V_P = 12$ V	$t_{sc}$	max.	100 hours

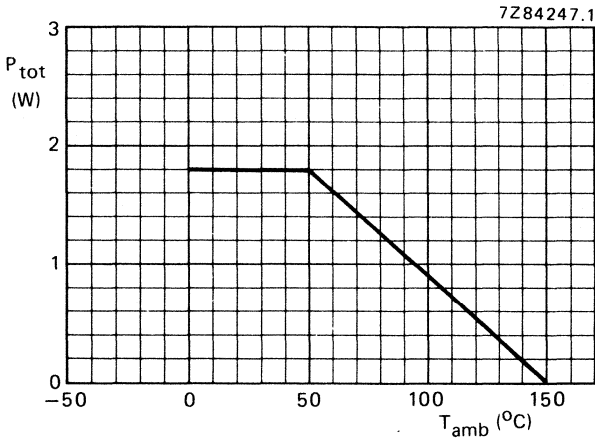


Fig. 2 Power derating curve.

**THERMAL RESISTANCE**

From junction to ambient

$$R_{thj-a} = 55 \text{ K/W}$$



**CHARACTERISTICS**

$V_P = 9\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f = 1\text{ kHz}$ ;  $T_{\text{amb}} = 25\ \text{°C}$ ; measured in test circuit of Fig. 1; unless otherwise specified.

**Power amplifier**

Output power at $d_{\text{tot}} = 10\ \%$	$P_O$	typ.	2 W
Closed loop voltage gain	$G_C$	typ.	36 dB
Total harmonic distortion at $P_O = 1\text{ W}$	$d_{\text{tot}}$	<	1 %
Input impedance	$ Z_i $	>	1 M $\Omega$
Ripple rejection at $f = 100\text{ Hz}$	RR	>	40 dB
Noise output voltage (r.m.s. value) $R_S = 0\ \Omega$ ; $B = 60\text{ Hz to }15\text{ kHz}$	$V_{N(\text{rms})}$	typ.	150 $\mu\text{V}$

**Preamplifier**

Open loop voltage gain	$G_O$	>	66 dB
Closed loop voltage gain	$G_C$	typ.	48 dB
Minimum closed loop voltage gain (when changing $R_f$ )	$G_C\ \text{min}$		31 dB
Output voltage at $d_{\text{tot}} = 1\ \%$	$V_O$	>	2 V
Output voltage with A.L.C. $V_i = 4,8\text{ mV}$	$V_O$	typ.	1,1 V
Total harmonic distortion with A.L.C. $V_i = 4,8\text{ mV}$ $V_i = 480\text{ mV}$	$d_{\text{tot}}$ $d_{\text{tot}}$	< <	1 % 3 %

**Signal-to-noise ratio**

related to $V_i = 1,2\text{ mV}$ ; $R_S = 0\ \Omega$ ; $B = 60\text{ Hz to }15\text{ kHz}$	S/N	typ.	60 dB
Input impedance	$ Z_i $	>	100 k $\Omega$
Ripple rejection at $f = 100\text{ Hz}$	RR	>	52 dB
Output impedance	$ Z_o $	<	50 $\Omega$

**Automatic Level Control (A.L.C.)**

Gain variation for $\Delta V_i = 40\text{ dB}$	$\Delta G_V$	typ.	2 dB
Limiting time at $\Delta V_i = 40\text{ dB}$	$t_l$	<	50 ms
Level setting time at $\Delta V_i = 40\text{ dB}$	$t_s$	<	50 ms
Recovery time at $\Delta V_i = 40\text{ dB}$	$t_r$	typ.	100 s

**Voltage stabilizer**

Output voltage	$V_{11-15}$	typ.	4,2 V
Load current	$I_{11}$	<	1 mA
Ripple rejection at $f = 100\text{ Hz}$	RR	>	40 dB



## 4 W AUDIO POWER AMPLIFIER WITH D.C. VOLUME CONTROL

The TDA1013A is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as television receivers and record players.

The d.c. volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 3,5 and 8 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.

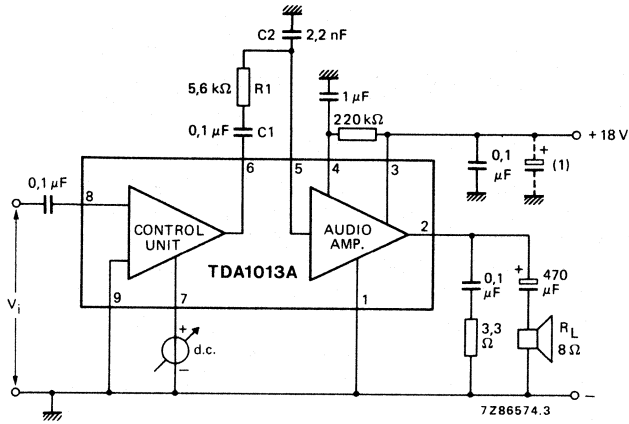
The SIL package (SOT-110B) offers a simple and low-cost heatsink connection.

### QUICK REFERENCE DATA

Supply voltage range	$V_p$		15 to 35 V
Repetitive peak output current	$I_{ORM}$	max.	1,5 A
Total sensitivity (d.c. control at max. gain) for $P_O = 2,5$ W	$V_i$	typ.	55 mV
<b>Audio amplifier</b>			
Output power at $d_{tot} = 10\%$ $V_p = 18$ V; $R_L = 8 \Omega$	$P_O$	typ.	4,5 W
Total harmonic distortion at $P_O = 2,5$ W; $R_L = 8 \Omega$	$d_{tot}$	typ.	0,5 %
Sensitivity for $P_O = 2,5$ W	$V_i$	typ.	125 mV
<b>D.C. volume control unit</b>			
Gain control range	$\phi$	>	80 dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	$V_i$	>	1,2 V
Sensitivity for $V_O = 125$ mV at max. voltage gain	$V_i$	typ.	55 mV
Input impedance (pin 8)	$ Z_i $	typ.	250 k $\Omega$

### PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).



(1) Belongs to power supply.

Fig. 1 Basic application diagram also used as test circuit with  $R1 = 5,1 \text{ k}\Omega$  and  $C1 = 22 \text{ nF}$ .

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p$	max.	35 V
Non-repetitive peak output current	$I_{OSM}$	max.	3 A
Repetitive peak output current	$I_{ORM}$	max.	1,5 A
Storage temperature	$T_{stg}$		-55 to + 150 °C
Crystal temperature	$T_j$		-25 to + 150 °C
Total power dissipation			see derating curve Fig. 2

**HEATSINK DESIGN**

Assume  $V_p = 18 \text{ V}$ ;  $R_L = 8 \Omega$ ;  $T_{amb} = 60 \text{ }^\circ\text{C}$  (max.);  $T_j = 150 \text{ }^\circ\text{C}$  (max.); for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,5 W.

The thermal resistance from junction to ambient can be expressed as:

$$R_{th \text{ j-a}} = R_{th \text{ j-tab}} + R_{th \text{ tab-h}} + R_{th \text{ h-a}} = \frac{T_j \text{ max} - T_{amb \text{ max}}}{P_{\text{max}}} = \frac{150 - 60}{2,5} = 36 \text{ K/W.}$$

Since  $R_{th \text{ j-tab}} = 9 \text{ K/W}$  and  $R_{th \text{ tab-h}} = 1 \text{ K/W}$ ,  $R_{th \text{ h-a}} = 36 - (9 + 1) = 26 \text{ K/W}$ .

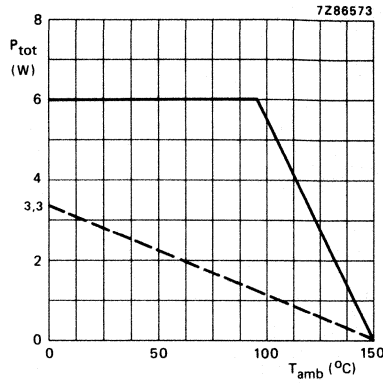


Fig. 2 Power derating curve.  
 ——— infinite heatsink;  
 - - - without heatsink.

**CHARACTERISTICS**

V<sub>p</sub> = 18 V; R<sub>L</sub> = 8 Ω; f = 1 kHz; T<sub>amb</sub> = 25 °C; unless otherwise specified

Supply voltage	V <sub>p</sub>	typ. 18 V 15 to 35 V
Total quiescent current	I <sub>tot</sub>	typ. 35 mA
Noise output voltage (see also note)	V <sub>n</sub>	< 1,4 mV
Total sensitivity (d.c. control at maximum gain) for P <sub>O</sub> = 2,5 W	V <sub>i</sub>	38 to 69 mV typ. 55 mV
Frequency response (-3 dB)	f	35 Hz to 20 kHz

**Audio amplifier**

Repetitive peak output current	I <sub>ORM</sub>	< 1,5 A
Output power at d <sub>tot</sub> = 10%	P <sub>O</sub>	> 4 W typ. 4,5 W
Total harmonic distortion at P <sub>O</sub> = 2,5 W	d <sub>tot</sub>	typ. 0,5 % < 1 %
Voltage gain	G <sub>v</sub>	typ. 30 dB
Sensitivity for P <sub>O</sub> = 2,5 W	V <sub>i</sub>	typ. 125 mV
Input impedance (pin 5)	Z <sub>i</sub>	> 100 kΩ typ. 250 kΩ

**Note**

Measured in a bandwidth according to IEC 179-curve 'A'; R<sub>S</sub> = 5 kΩ and d.c. control at minimum gain.

**CHARACTERISTICS (continued)**

**D.C. volume control unit**

Gain control range (see also Fig. 3)

Signal handling at  $d_{tot} < 1\%$   
(d.c. control at 0 dB)

Sensitivity for  $V_O = 125$  mV at max. voltage gain

Input impedance (pin 8)

Output impedance (pin 6)

$\phi > 80$  dB

$V_i > 1,2$  V

$V_i$  typ. 55 mV

$|Z_i| > 100$  k $\Omega$   
typ. 250 k $\Omega$

$|Z_o|$  100 to 400  $\Omega$   
typ. 200  $\Omega$

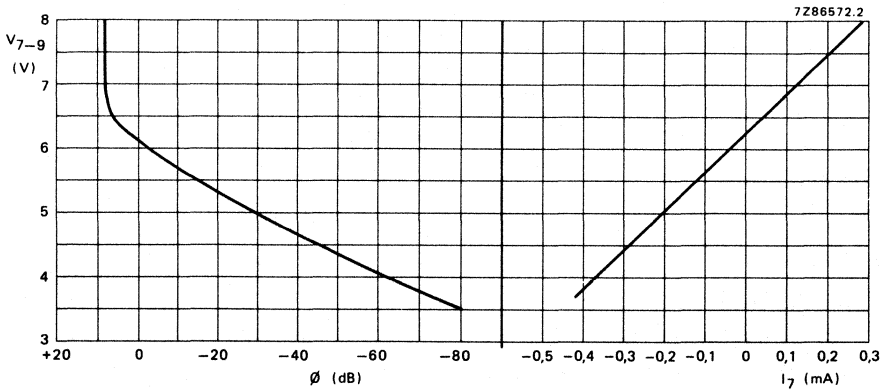


Fig. 3 Typical values gain control;  $V_i$  at pin 7.



## 1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a  $4 \Omega$  load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

## QUICK REFERENCE DATA

Supply voltage range	$V_P$	3,6 to 18 V
Peak output current	$I_{OM}$	max. 2,5 A
Output power at $d_{tot} = 10\%$		
$V_P = 12 \text{ V}; R_L = 4 \Omega$	$P_O$	typ. 4,2 W
$V_P = 9 \text{ V}; R_L = 4 \Omega$	$P_O$	typ. 2,3 W
$V_P = 6 \text{ V}; R_L = 4 \Omega$	$P_O$	typ. 1,0 W
Total harmonic distortion at $P_O = 1 \text{ W}; R_L = 4 \Omega$	$d_{tot}$	typ. 0,3 %
Input impedance		
preamplifier (pin 8)	$ Z_i $	> 100 k $\Omega$
power amplifier (pin 6)	$ Z_i $	typ. 20 k $\Omega$
Total quiescent current	$I_{tot}$	typ. 14 mA
Operating ambient temperature	$T_{amb}$	-25 to + 150 °C
Storage temperature	$T_{stg}$	-55 to + 150 °C

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

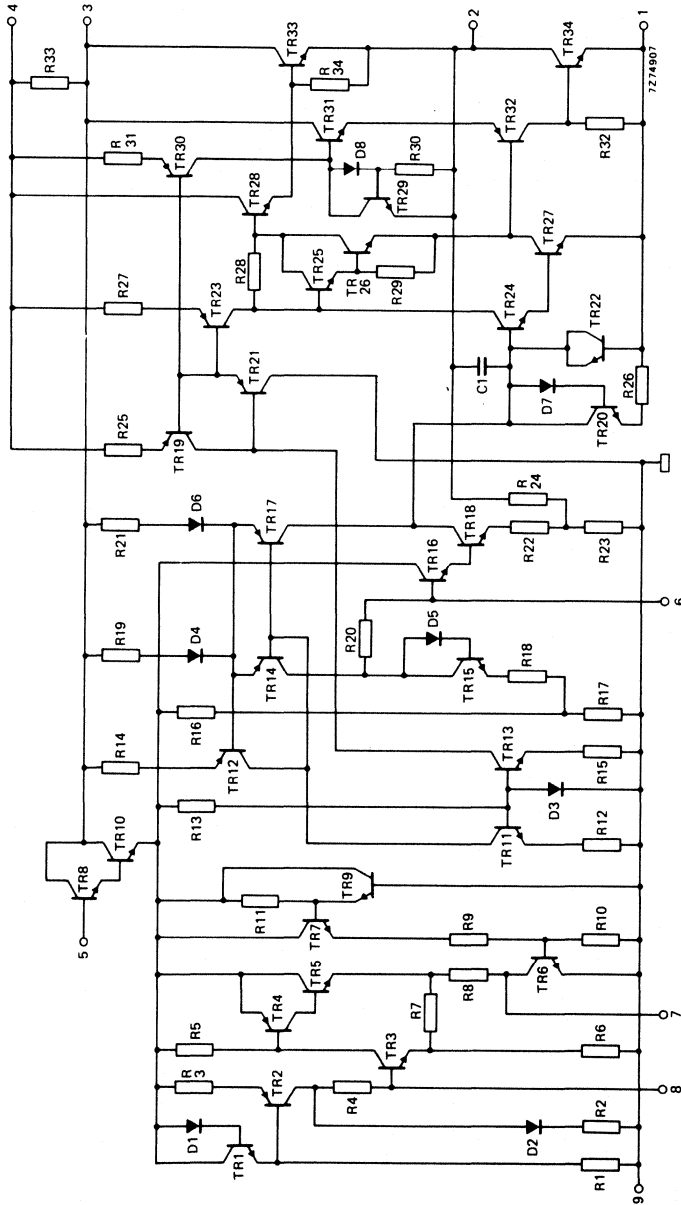


Fig. 1 Circuit diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p$	max.	18 V
Peak output current	$I_{OM}$	max.	2,5 A
Total power dissipation			see derating curve Fig. 2
Storage temperature	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature	$T_{amb}$		-25 to + 150 °C
A.C. short-circuit duration of load during sine-wave drive; $V_p = 12$ V	$t_{sc}$	max.	100 hours

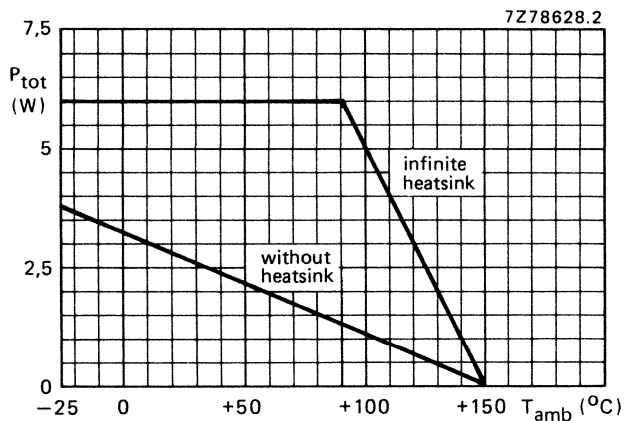


Fig. 2 Power derating curve.

**HEATSINK DESIGN**Assume  $V_p = 12$  V;  $R_L = 4 \Omega$ ;  $T_{amb} = 45$  °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th j-a} = R_{th j-tab} + R_{th tab-h} + R_{th h-a} = \frac{150 - 45}{1,8} = 58 \text{ K/W.}$$

Where  $R_{th j-a}$  of the package is 45 K/W, so no external heatsink is required.

**D.C. CHARACTERISTICS**

Supply voltage range	$V_P$	3,6 to 18 V
Repetitive peak output current	$I_{ORM}$	< 2 A
Total quiescent current at $V_P = 12$ V	$I_{tot}$	typ. 14 mA < 25 mA

**A.C. CHARACTERISTICS**

$T_{amb} = 25$  °C;  $V_P = 12$  V;  $R_L = 4$   $\Omega$ ;  $f = 1$  kHz unless otherwise specified; see also Fig. 3.

A.F. output power at  $d_{tot} = 10\%$  (note 1)

with bootstrap:

$V_P = 12$  V;  $R_L = 4$   $\Omega$

$P_O$  typ. 4,2 W

$V_P = 9$  V;  $R_L = 4$   $\Omega$

$P_O$  typ. 2,3 W

$V_P = 6$  V;  $R_L = 4$   $\Omega$

$P_O$  typ. 1,0 W

without bootstrap:

$V_P = 12$  V;  $R_L = 4$   $\Omega$

$P_O$  typ. 3,0 W

Voltage gain:

preamplifier (note 2)

$G_{V1}$  typ. 23 dB

power amplifier

$G_{V2}$  typ. 29 dB

total amplifier

$G_{Vtot}$  typ. 52 dB  
49 to 55 dB

Total harmonic distortion at  $P_O = 1,5$  W

$d_{tot}$  typ. 0,3 %  
< 1,0 %

Frequency response; -3 dB (note 3)

B 60 Hz to 15 kHz

Input impedance:

preamplifier (note 4)

$|Z_{i1}|$  > 100 k $\Omega$   
typ. 200 k $\Omega$

power amplifier

$|Z_{i2}|$  typ. 20 k $\Omega$

Output impedance preamplifier

$|Z_{o1}|$  typ. 1 k $\Omega$

Output voltage preamplifier (r.m.s. value)

$d_{tot} < 1\%$  (note 2)

$V_{O(rms)}$  typ. 0,8 V

Noise output voltage (r.m.s. value; note 5)

$R_S = 0$   $\Omega$

$V_{n(rms)}$  typ. 0,2 mV

$R_S = 10$  k $\Omega$

$V_{n(rms)}$  typ. 0,5 mV

Noise output voltage at  $f = 500$  kHz (r.m.s. value)

B = 5 kHz;  $R_S = 0$   $\Omega$

$V_{n(rms)}$  typ. 8  $\mu$ V

Ripple rejection (note 6)

$f = 100$  Hz

RR typ. 38 dB

## Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 k $\Omega$ .
3. Measured at  $P_O = 1$  W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 k $\Omega$  (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

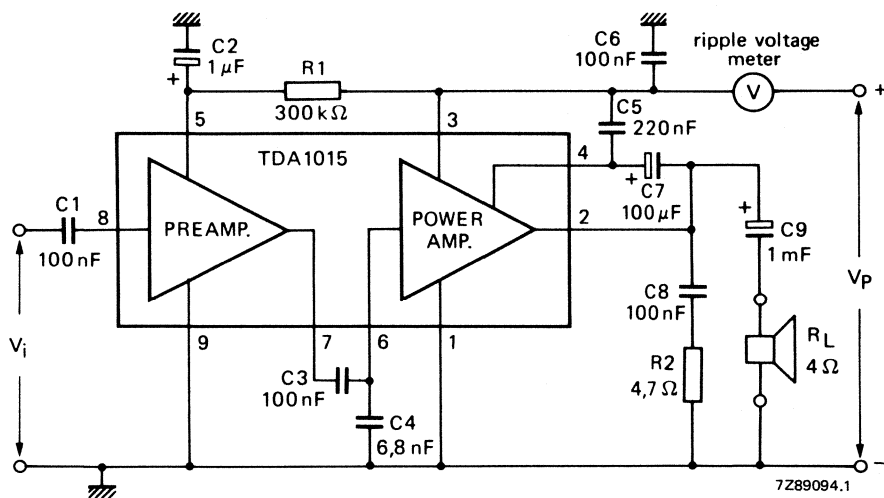


Fig. 3 Test circuit.

APPLICATION INFORMATION

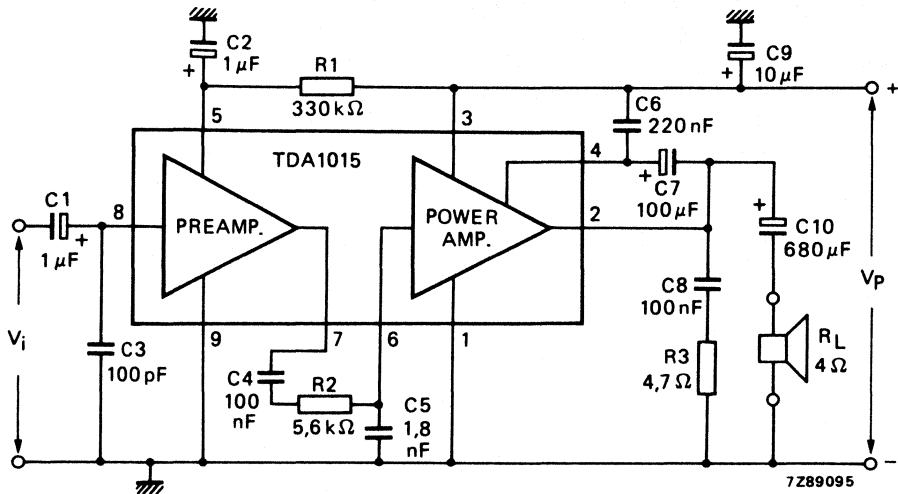


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

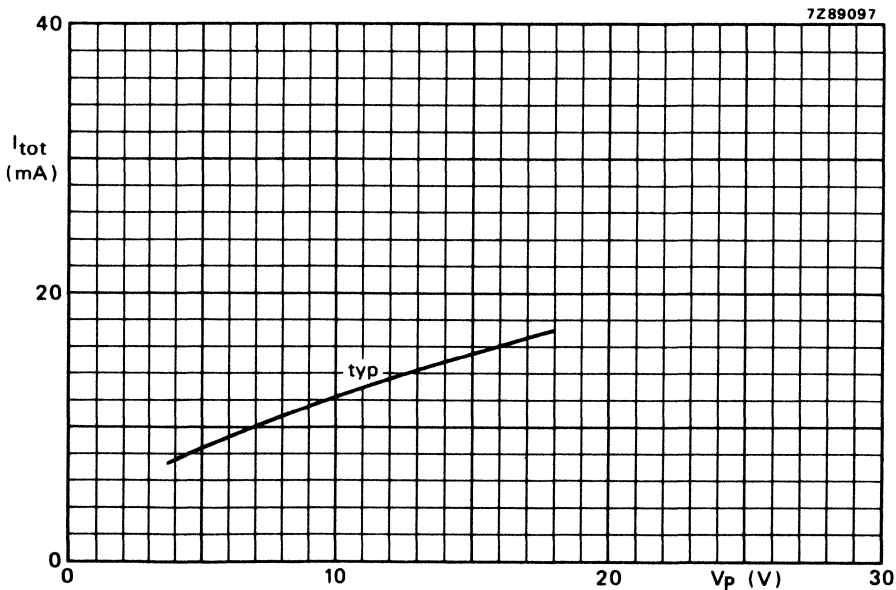


Fig. 5 Total quiescent current as a function of supply voltage.

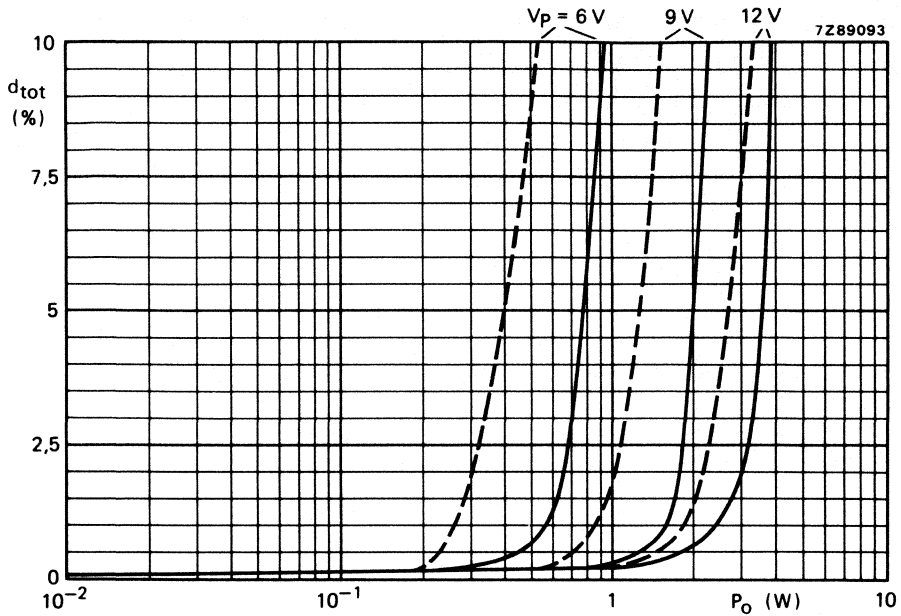


Fig. 6 Total harmonic distortion as a function of output power across  $R_L$ ; — with bootstrap; - - - without bootstrap;  $f = 1$  kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

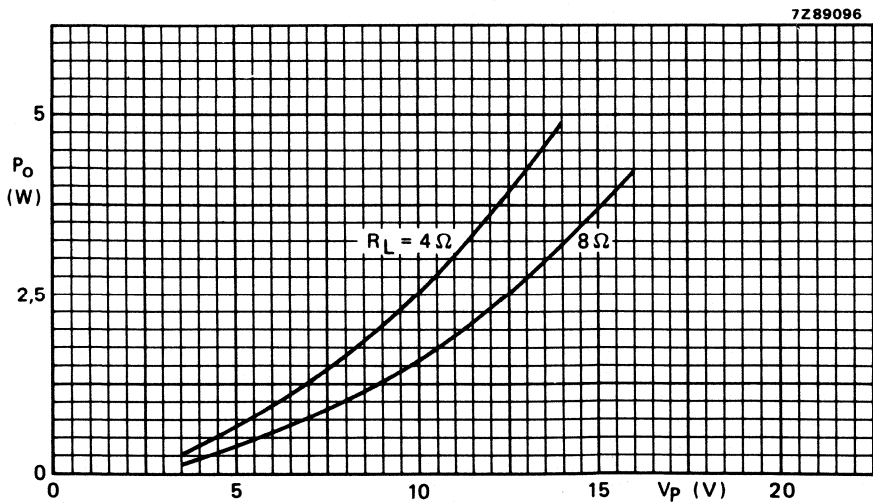


Fig. 7 Output power across  $R_L$  as a function of supply voltage with bootstrap;  $d_{tot} = 10\%$ ; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

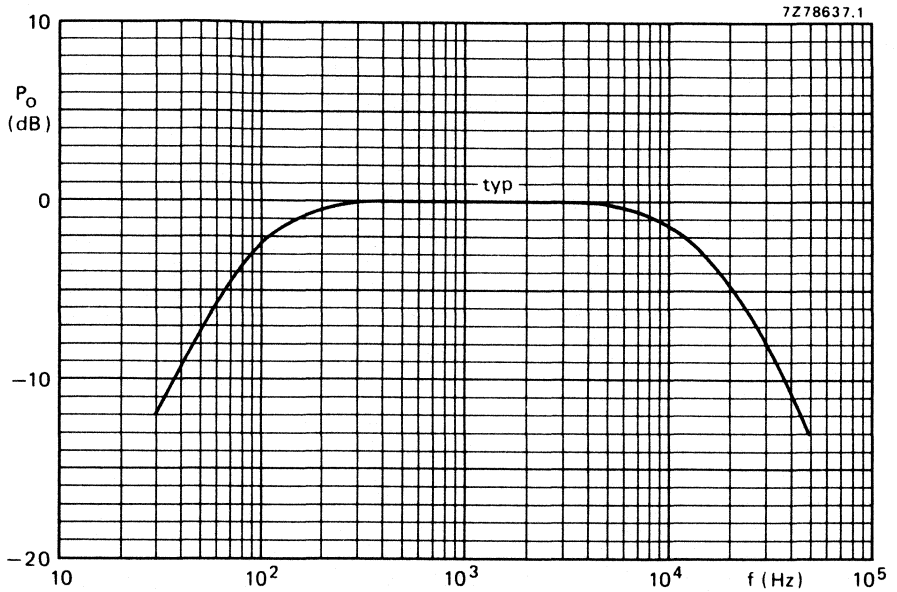


Fig. 8 Voltage gain as a function of frequency;  $P_o$  relative to 0 dB = 1 W;  $V_p = 12$  V;  $R_L = 4 \Omega$ .

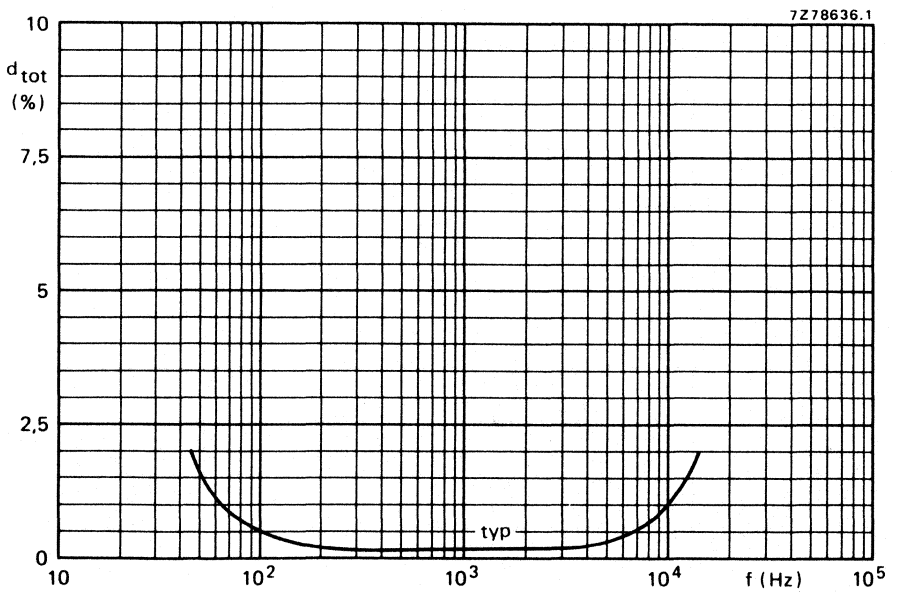


Fig. 9 Total harmonic distortion as a function of frequency;  $P_o = 1$  W;  $V_p = 12$  V;  $R_L = 4 \Omega$ .



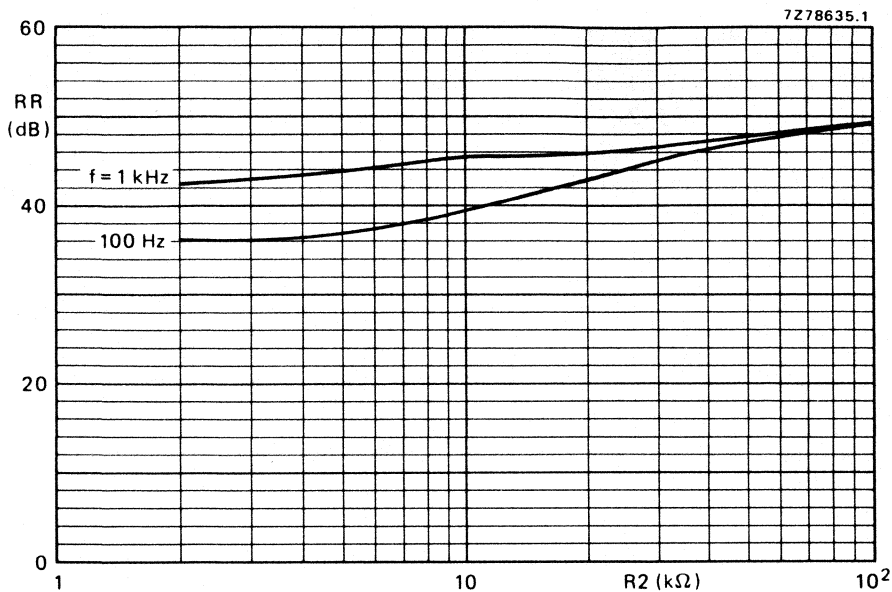


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4);  $R_S = 0$ ; typical values.

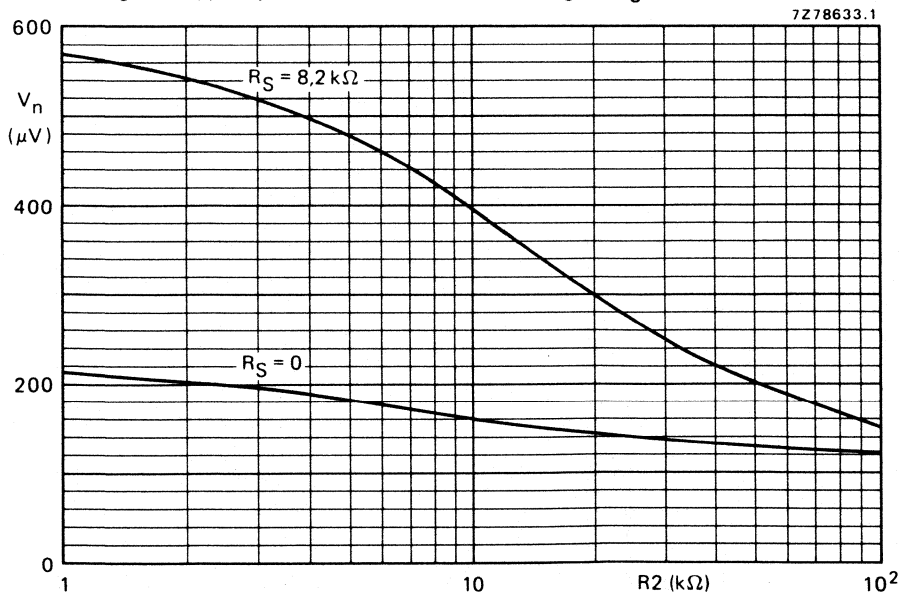


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

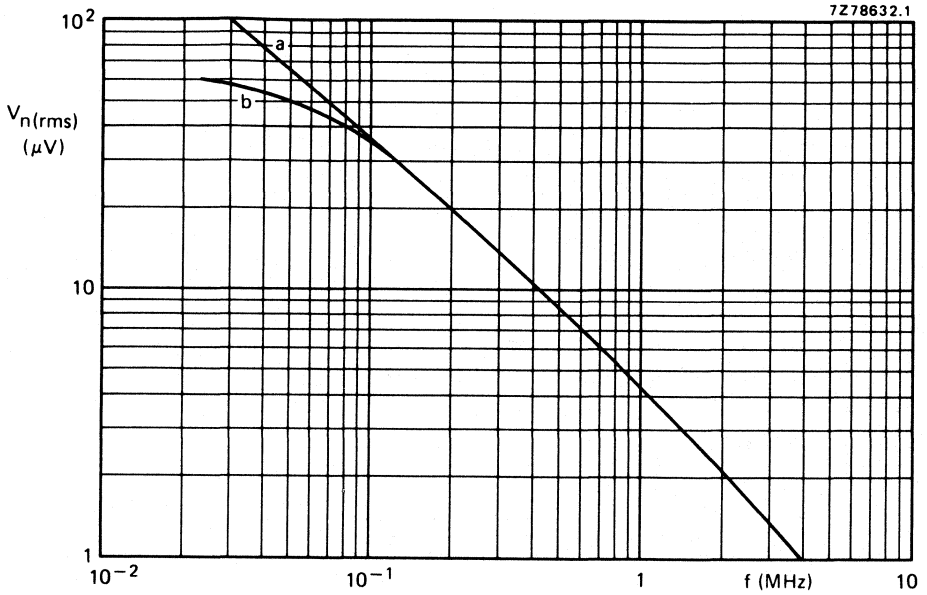


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier;  $B = 5$  kHz;  $R_S = 0$ ; typical values.

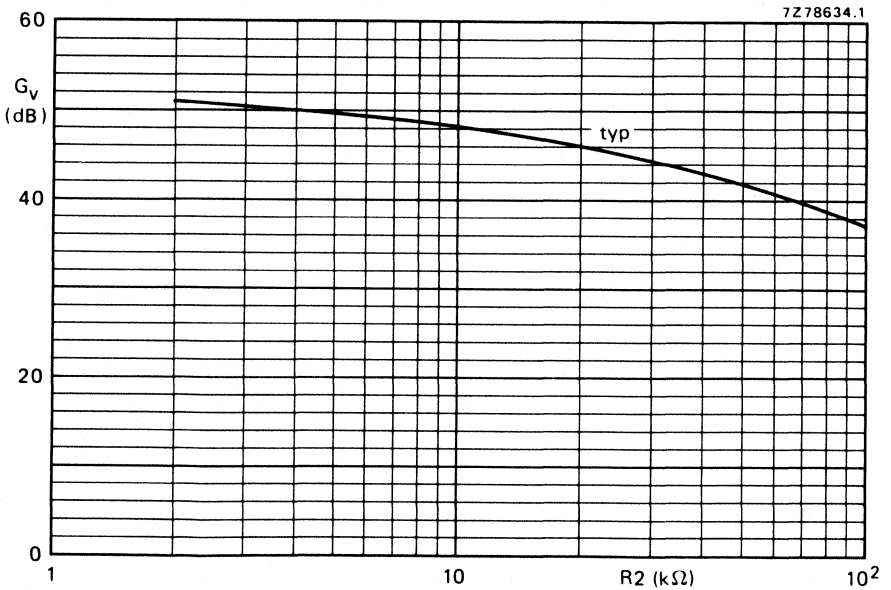


Fig. 13 Voltage gain as a function of  $R_2$  (see Fig. 4).

## RECORDING/PLAYBACK AND 2 W AUDIO POWER AMPLIFIER

### GENERAL DESCRIPTION

The TDA1016 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit incorporates the following features:

#### Features

- Power amplifier/monitor amplifier
- Preamplifier/record and playback amplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer
- Short-circuit (up to 12 V a.c.) and thermal protection.

### QUICK REFERENCE DATA

Supply voltage range	$V_p$	3,6 to 15 V
Supply current; total quiescent at $V_p = 6$ V	$I_{tot}$	typ. 10 mA
Operating ambient temperature range	$T_{amb}$	-25 to 150 °C

#### Power amplifier

Output power at $d_{tot} = 10\%$ $V_p = 6$ V; $R_L = 4 \Omega$	$P_o$	typ.	1 W
$V_p = 9$ V; $R_L = 4 \Omega$	$P_o$	typ.	2 W
Closed loop gain	$G_c$	typ.	36 dB

#### Preamplifier

Open loop gain	$G_o$	min.	70 dB
Minimum closed loop voltage gain	$G_{c \min}$	min.	35 dB
Output voltage at $d_{tot} = 1\%$	$V_o$	min.	1 V

#### Automatic Level Control (A.L.C.)

Gain variation for $\Delta V_i = 40$ dB	$\Delta G_v$	typ.	2 dB
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#### Stabilized supply voltage

Output voltage	$V_{5-16}$	typ.	2,6 V
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### PACKAGE OUTLINE

16-lead DIL; plastic, with internal heat spreader (SOT-38WE-2).

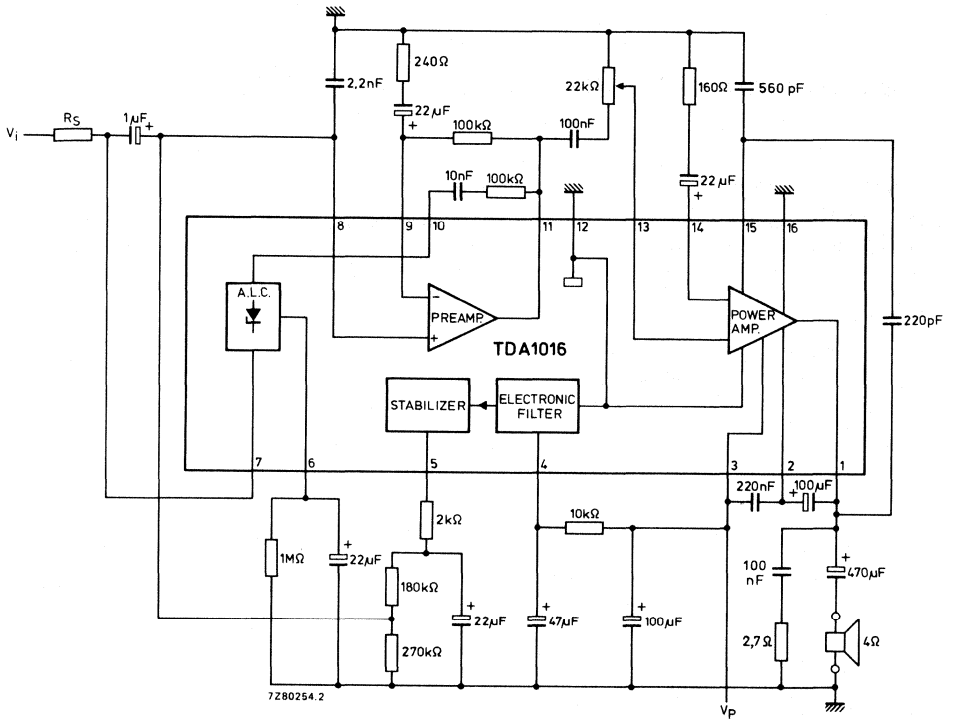


Fig. 1 Block diagram with external components; also used as test circuit.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_p$	max.	18 V
Repetitive peak output current	$I_{ORM}$	max.	1 A
Non-repetitive peak output current (pin 1)	$I_{OSM}$	max.	2 A
Total power dissipation			see derating curve Fig. 2
A.C. short-circuit duration of load during sinewave drive; $V_p = 12$ V	$t_{sc}$	max.	100 hours
Crystal temperature	$T_c$	max.	150 °C
Storage temperature range	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature range	$T_{amb}$		-25 to + 150 °C

**THERMAL RESISTANCE**

The power derating curve (Fig. 2) is based on the following data

From junction to ambient  $R_{thj-a} = 55$  K/W

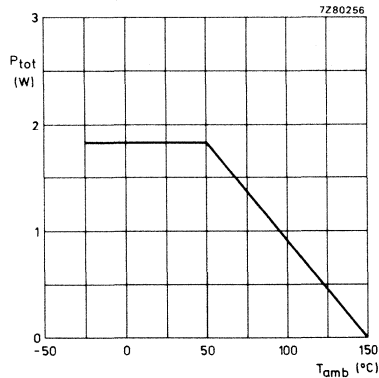


Fig. 2 Power derating curve.



## CHARACTERISTICS

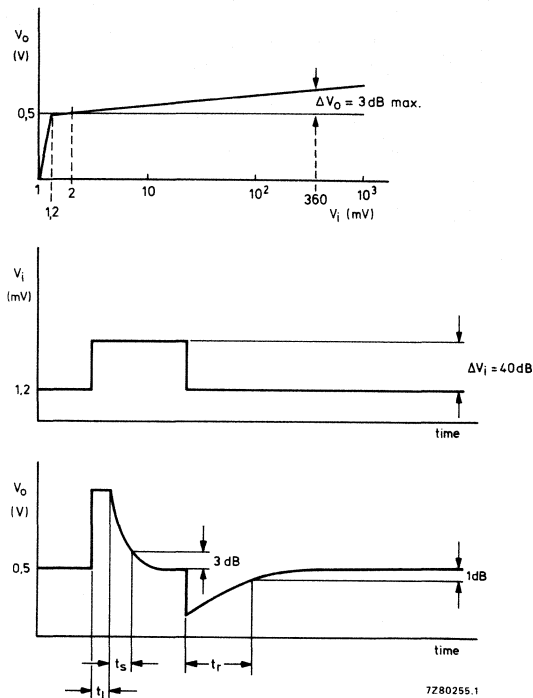
$V_p = 6 \text{ V}$ ;  $R_L = 4 \Omega$ ;  $f = 1 \text{ kHz}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 3)</b>					
Supply voltage	$V_p$	3,6	6	15	V
Supply current; total quiescent at $V_p = 6 \text{ V}$	$I_{\text{tot}}$	—	10	—	mA
<b>Power amplifier</b>					
Output power at $d_{\text{tot}} = 10\%*$ $V_p = 6 \text{ V}$	$P_o$	—	1	—	W
$V_p = 9 \text{ V}$	$P_o$	—	2	—	W
Closed loop voltage gain	$G_c$	—	36	—	dB
Total harmonic distortion at $P_o = 0,5 \text{ W}$	$d_{\text{tot}}$	—	—	1	%
Input impedance	$ Z_i $	0,5	—	—	M $\Omega$
Ripple rejection at $f = 100 \text{ Hz}$ ( $R_S = 0 \Omega$ )	RR	40	50	—	dB
Noise output voltage (r.m.s. value) $R_S = 0 \Omega$ ; $B = 60 \text{ Hz to } 15 \text{ kHz}$	$V_{n(\text{rms})}$	—	90	200	$\mu\text{V}$
Noise output voltage at $500 \text{ kHz}$ $R_S = 0 \Omega$ ; $B = 5 \text{ kHz}$	$V_n$	—	8	—	$\mu\text{V}$
<b>Preamplifier</b>					
Open loop voltage gain at $f = 10 \text{ kHz}$	$G_o$	70	78	—	dB
Closed loop voltage gain	$G_c$	—	52	—	dB
Minimum closed loop voltage gain (when changing $R_f$ )	$G_{c \text{ min}}$	35	—	—	dB
Output voltage at $d_{\text{tot}} = 1\%$	$V_o$	1	—	—	V
Output voltage with A.L.C. $V_i = 2 \text{ mV}$	$V_o$	0,45	0,5	0,55	V
Total harmonic distortion with A.L.C. $V_i = 2 \text{ mV}$	$d_{\text{tot}}$	—	—	1	%
$V_i = 360 \text{ mV}$	$d_{\text{tot}}$	—	—	3	%
Signal-to-noise ratio related to $V_i = 1,2 \text{ mV}$ ; $R_S = 1 \text{ k}\Omega$ ; $B = 60 \text{ Hz to } 15 \text{ kHz}$	S/N	—	60	—	dB
Input impedance	$ Z_i $	100	—	—	k $\Omega$
Ripple rejection at $f = 100 \text{ Hz}$ ; $R_S = 0 \Omega$	RR	50	54	—	dB
Output impedance **	$ Z_o $	—	—	50	$\Omega$

\* Measured with an ideal coupling capacitor connected to the speaker load.

\*\*  $I_p$  (effective value) must not exceed 1 mA.

parameter	symbol	min.	typ.	max.	unit
<b>Automatic Level Control (A.L.C.) (see Fig. 3) **</b>					
Gain variation for $\Delta V_i = 45$ dB	$\Delta G_V$	—	2	3	dB
Limiting time*	$t_l$	—	—	50	ms
Level setting time*	$t_s$	—	—	50	ms
Recovery time* $\blacktriangle$	$t_r$	—	100	—	s
<b>Voltage stabilizer</b>					
Output voltage	$V_{11-15}$	—	2,6	—	V
Load current	$I_{11}$	—	—	1,5	mA
Ripple rejection at $f = 100$ Hz	RR	40	—	—	dB

Fig. 3 Typical A.L.C. curve with  $R_S = 10$  k $\Omega$ .

- \* At  $\Delta V_i = 40$  dB with respect to  $V_i = 1,2$  mV.
- \*\* A.L.C. tracking in stereo anode pin 6 interconnected to an RC, time constant has a typical spread within 7 dB.
- $\blacktriangle$  Without a shunt resistor across A.L.C.  
With 1 M $\Omega$  or 2,2 M $\Omega$  across A.L.C. recovery time becomes 22 or 50 seconds.





## 12 W CAR RADIO POWER AMPLIFIER

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of  $V_P = 14,4$  V, an output power of 7 W can be delivered into a 4  $\Omega$  load and 12 W into 2  $\Omega$ .

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V ( $< 45$  V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

### QUICK REFERENCE DATA

Supply voltage range	$V_P$		6 to 18 V
Repetitive peak output current	$I_{ORM}$	<	4 A
Output power at $d_{tot} = 10\%$ (with bootstrap)			
$V_P = 14,4$ V; $R_L = 2 \Omega$	$P_O$	>	10 W
$V_P = 14,4$ V; $R_L = 4 \Omega$	$P_O$	typ.	12 W
$V_P = 14,4$ V; $R_L = 8 \Omega$	$P_O$	typ.	7 W
	$P_O$	typ.	3,5 W
Output power at $d_{tot} = 10\%$ (without bootstrap)			
$V_P = 14,4$ V; $R_L = 4 \Omega$	$P_O$	>	4,5 W
Input impedance			
preamplifier (pin 8)	$ Z_i $	typ.	40 k $\Omega$
power amplifier (pin 6)	$ Z_i $	typ.	40 k $\Omega$
Total quiescent current at $V_P = 14,4$ V	$I_{tot}$	typ.	30 mA
Stand-by current	$I_{sb}$	<	1 mA
Storage temperature range	$T_{stg}$		-55 to + 150 $^{\circ}$ C
Crystal temperature	$T_c$	max.	150 $^{\circ}$ C

### PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

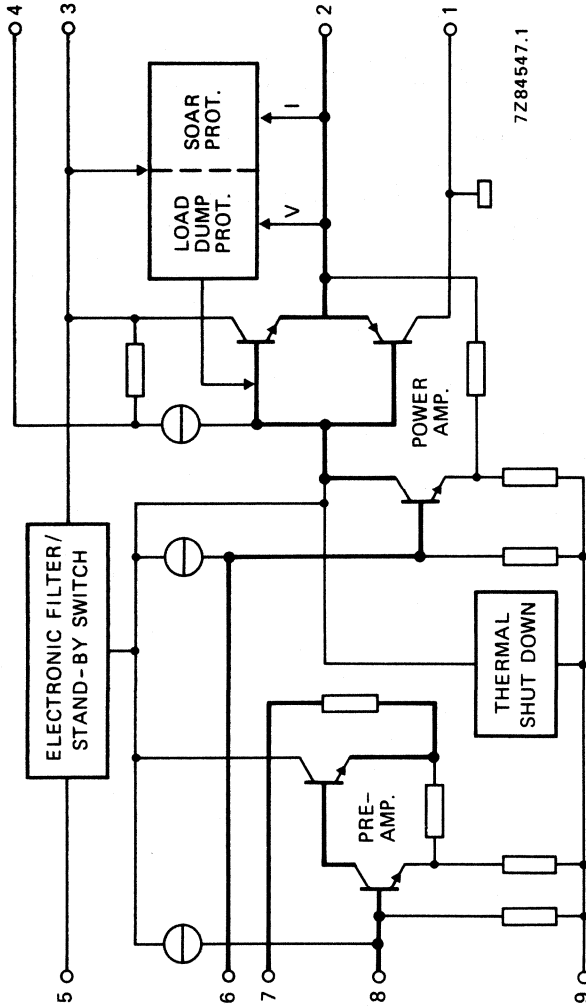


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

**PINNING**

- 1. Negative supply (substrate)
- 2. Output power stage
- 3. Positive supply ( $V_p$ )
- 4. Bootstrap
- 5. Ripple rejection filter
- 6. Input power stage
- 7. Output preamplifier
- 8. Input preamplifier
- 9. Negative supply



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 3)	V <sub>p</sub>	max.	18 V
Supply voltage; non-operating	V <sub>p</sub>	max.	28 V
Supply voltage; load dump	V <sub>p</sub>	max.	45 V
Non-repetitive peak output current	I <sub>OSM</sub>	max.	6 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T <sub>stg</sub>	-55 to + 150 °C	
Crystal temperature	T <sub>c</sub>	max.	150 °C
Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); V <sub>p</sub> = 14,4 V	t <sub>sc</sub>	max.	100 hours

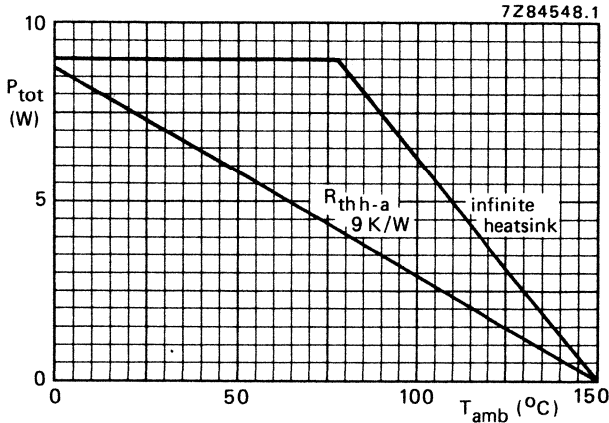


Fig. 2 Power derating curves.

**HEATSINK DESIGN EXAMPLE**

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in  $2\ \Omega$  at  $V_p = 14,4\text{ V}$

maximum sine-wave dissipation: 5,2 W

$T_{amb} = 60\text{ °C}$  maximum

$$R_{th\ j-a} = R_{th\ j-tab} + R_{th\ tab-h} + R_{th\ h-a} = \frac{150 - 60}{5,2} = 17,3\text{ K/W}$$

Since  $R_{th\ j-tab} + R_{th\ tab-h} = 8\text{ K/W}$ ,  $R_{th\ h-a} = 17,3 - 8 \approx 9\text{ K/W}$ .

**D.C. CHARACTERISTICS**

Supply voltage range (pin 3)	$V_P$		6 to 18 V
Repetitive peak output current	$I_{ORM}$	<	4 A
Total quiescent current	$I_{tot}$	typ.	30 mA
at $V_P = 14,4$ V	$I_{tot}$	typ.	40 mA
at $V_P = 18$ V			

**A.C. CHARACTERISTICS**

$T_{amb} = 25$  °C;  $V_P = 14,4$  V;  $R_L = 4$   $\Omega$ ;  $f = 1$  kHz; unless otherwise specified; see also Fig. 3

Output power at $d_{tot} = 10\%$ ; with bootstrap (note 1)	$P_o$	>	10 W
$V_P = 14,4$ V; $R_L = 2$ $\Omega$		typ.	12 W
$V_P = 14,4$ V; $R_L = 4$ $\Omega$	$P_o$	>	6 W
$V_P = 14,4$ V; $R_L = 8$ $\Omega$	$P_o$	typ.	7 W
$V_P = 14,4$ V; $R_L = 8$ $\Omega$	$P_o$	typ.	3,5 W
Output power at $d_{tot} = 1\%$ ; with bootstrap (note 1)	$P_o$	typ.	9,5 W
$V_P = 14,4$ V; $R_L = 2$ $\Omega$	$P_o$	typ.	6 W
$V_P = 14,4$ V; $R_L = 4$ $\Omega$	$P_o$	typ.	3 W
$V_P = 14,4$ V; $R_L = 8$ $\Omega$			
Output voltage (r.m.s. value)	$V_{O(rms)}$	typ.	5 V
$R_L = 1$ k $\Omega$ ; $d_{tot} = 0,5\%$			
Output power at $d_{tot} = 10\%$ ; without bootstrap	$P_o$	>	4,5 W
Voltage gain			
preamplifier (note 2)	$G_{v1}$	typ.	17,7 dB
			16,7 to 18,7 dB
power amplifier	$G_{v2}$	typ.	29,5 dB
			28,5 to 30,5 dB
total amplifier	$G_{v tot}$	typ.	47 dB
			46,2 to 48,2 dB
Input impedance			
preamplifier	$ Z_i $	typ.	40 k $\Omega$
			28 to 52 k $\Omega$
power amplifier	$ Z_i $	typ.	40 k $\Omega$
			28 to 52 k $\Omega$
Output impedance			
preamplifier	$ Z_o $	typ.	2,0 k $\Omega$
			1,4 to 2,6 k $\Omega$
power amplifier	$ Z_o $	typ.	50 m $\Omega$
Output voltage (r.m.s. value) at $d_{tot} = 1\%$			
preamplifier (note 2)	$V_{O(rms)}$	>	1 V
		typ.	1,5 V
Frequency response	B		50 Hz to 25 kHz
Noise output voltage (r.m.s. value; note 3)			
$R_S = 0$ $\Omega$	$V_{n(rms)}$	typ.	0,3 mV
		<	0,5 mV
$R_S = 8,2$ k $\Omega$	$V_{n(rms)}$	typ.	0,5 mV
		<	1,0 mV



Ripple rejection (note 4)  
at  $f = 100 \text{ Hz}$ ;  $C_2 = 1 \mu\text{F}$

RR typ. 44 dB

at  $f = 1 \text{ kHz to } 10 \text{ kHz}$

RR > 48 dB  
typ. 54 dB

Bootstrap current at onset of clipping (pin 4)

$R_L = 4 \Omega$  and  $2 \Omega$

$I_4$  typ. 40 mA

Stand-by current (note 5)

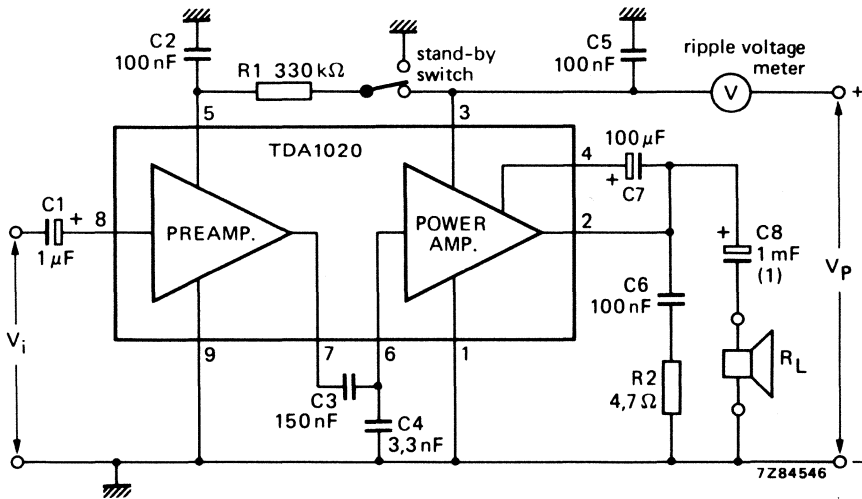
$I_{sb}$  < 1 mA

Crystal temperature for  $-3 \text{ dB gain}$

$T_c$  > 150 °C

**Notes**

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of  $40 \text{ k}\Omega$ .
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is  $2 \text{ V}$ ; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).



(1) With  $R_L = 2 \Omega$ , preferred value of  $C_8 = 2200 \mu\text{F}$ .

Fig. 3 Test circuit.



## SIGNAL-SOURCES SWITCH

The TDA1028 is a quadruple operational amplifier connected as an impedance converter. Each amplifier has 2 switchable inputs which are protected by clamping diodes. The input currents are independent of the switch position and the outputs are short-circuit protected.

The device is intended as an electronic four-channel signal-sources switch in a.f. amplifiers.

## QUICK REFERENCE DATA

Supply voltage range (pin 9)	$V_p$		6 to 23 V
Operating ambient temperature	$T_{amb}$		-30 to + 80 °C
Supply voltage (pin 9)	$V_p$	typ.	20 V
Current consumption (pins 4, 5, 12, 13 unloaded)	$I_g$	typ.	2,9 mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6 V
Voltage gain	$G_v$	typ.	1
Total harmonic distortion	$d_{tot}$	typ.	0,01 %
Crosstalk	$\alpha$	typ.	70 dB
Signal-to-noise ratio	S/N	typ.	120 dB



## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

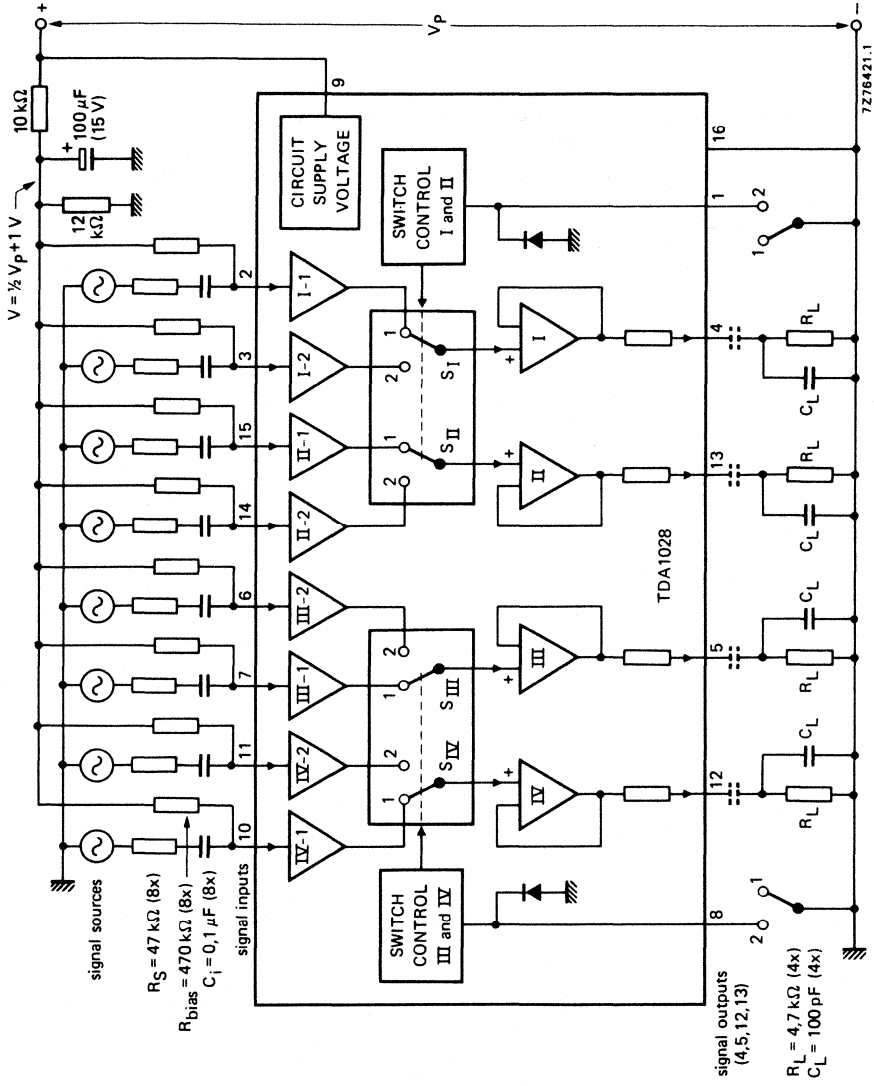


Fig. 1 Block diagram.



## SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

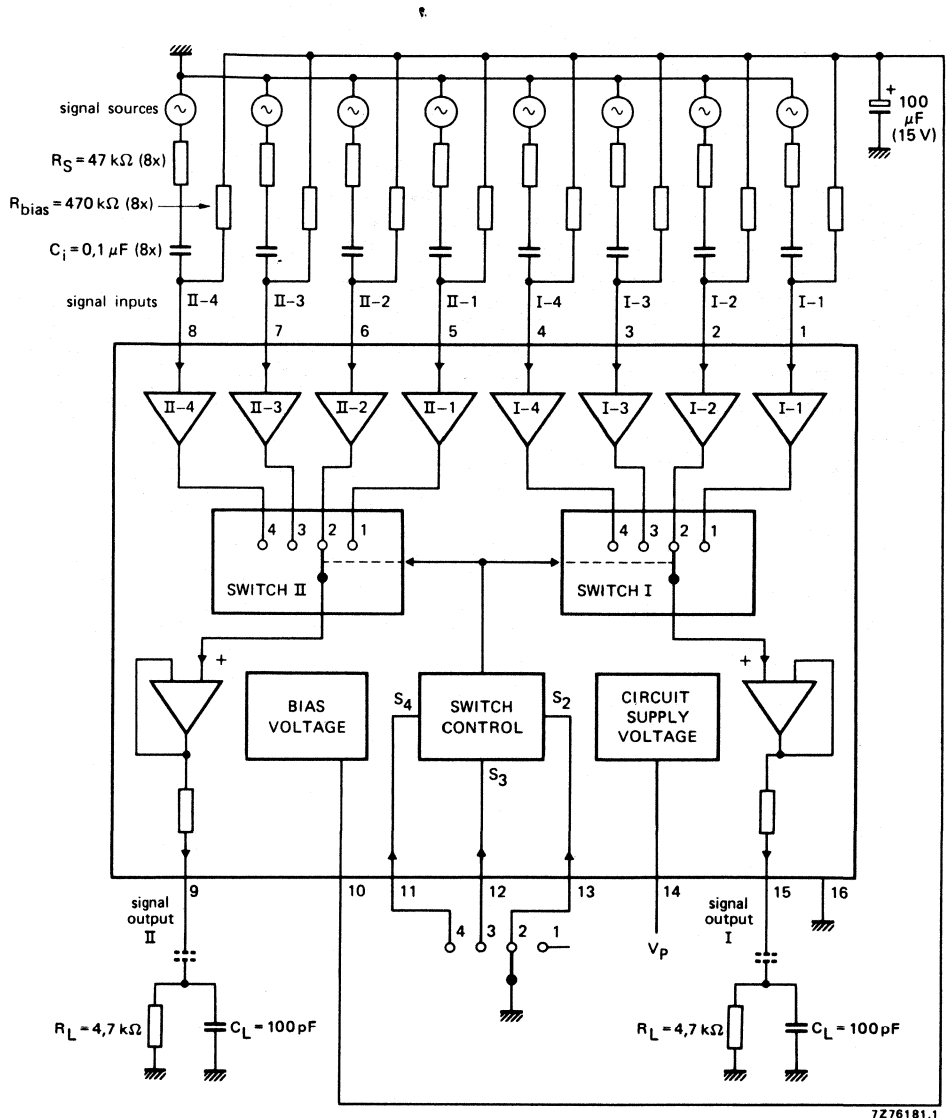
### QUICK REFERENCE DATA

Supply voltage range (pin 14)	$V_p$		6 to 23 V
Operating ambient temperature	$T_{amb}$		-30 to + 80 °C
Supply voltage (pin 14)	$V_p$	typ.	20 V
Current consumption	$I_{14}$	typ.	3,5 mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6 V
Voltage gain	$G_v$	typ.	1
Total harmonic distortion	$d_{tot}$	typ.	0,01 %
Crosstalk	$\alpha$	typ.	70 dB
Signal-to-noise ratio	S/N	typ.	120 dB



### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



7Z76181.1

Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	$V_P$	max.	23 V
Input voltage (pins 1 to 8)	$V_I$	max.	$V_P$
	$-V_I$	max.	0,5 V
Switch control voltage (pins 11, 12 and 13)	$V_S$		0 to 23 V
Input current	$\pm I_I$	max.	20 mA
Switch control current	$-I_S$	max.	50 mA
Total power dissipation	$P_{tot}$	max.	800 mW
Storage temperature	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature	$T_{amb}$		-30 to + 80 °C

**CHARACTERISTICS** $V_P = 20$  V;  $T_{amb} = 25$  °C; unless otherwise specified

Current consumption without load; $I_G = I_{15} = 0$	$I_{14}$	typ.	3,5 mA
			2 to 5 mA
Supply voltage range (pin 14)	$V_P$		6 to 23 V

**Signal inputs**

Input offset voltage of switched-on inputs $R_S \leq 1$ k $\Omega$	$V_{io}$	typ.	2 mV
		<	10 mV
Input offset current of switched-on inputs	$I_{io}$	typ.	20 nA
		<	200 nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	$I_{io}$	typ.	20 nA
		<	200 nA
Input bias current independent of switch position	$I_i$	typ.	250 nA
		<	950 nA
Capacitance between adjacent inputs	$C$	typ.	0,5 pF
D.C. input voltage range	$V_I$		3 to 19 V
Supply voltage rejection ratio; $R_S \leq 10$ k $\Omega$	SVRR	typ.	100 $\mu$ V/V
Equivalent input noise voltage $R_S = 0$ ; $f = 20$ Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5 $\mu$ V
Equivalent input noise current $f = 20$ Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05 nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S = 1$ k $\Omega$ ; $f = 1$ kHz	$\alpha$	typ.	100 dB



**CHARACTERISTICS** (continued)

**Signal amplifier**

Voltage gain of a switched-on input  
at  $I_g = I_{15} = 0; R_L = \infty$

$G_V$  typ. 1

Current gain of a switched-on amplifier

$G_i$  typ.  $10^5$

**Signal outputs**

Output resistance (pins 9 and 15)

$R_O$  typ. 400  $\Omega$

Output current capability at  $V_p = 6$  to 23 V

$\pm I_g; \pm I_{15}$  typ. 5 mA

Frequency limit of the output voltage

$V_{i(p-p)} = 1$  V;  $R_S = 1$  k $\Omega$ ;  $R_L = 10$  M $\Omega$ ;  $C_L = 10$  pF

f typ. 1,3 MHz

Slew rate (unity gain);  $\Delta V_{9-16}/\Delta t$ ;  $\Delta V_{15-16}/\Delta t$

$R_L = 10$  M $\Omega$ ;  $C_L = 10$  pF

S typ. 2 V/ $\mu$ s

**Bias voltage**

D.C. output voltage

$V_{10-16}$  typ. 11 V \*  
10,2 to 11,8 V

Output resistance

$R_{10-16}$  typ. 8,2 k $\Omega$

**Switch control**

switched-on inputs	interconnected pins	control voltages		
		$V_{11-16}$	$V_{12-16}$	$V_{13-16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at  $V_{SL} \leq 1,5$  V.

**Control inputs** (pins 11, 12 and 13)

Required voltage

HIGH

$V_{SH} > 3,3$  V \*\*

LOW

$V_{SL} < 2,1$  V

Input current

HIGH (leakage current)

$I_{SH} < 1$   $\mu$ A

LOW (control current)

$-I_{SL} < 250$   $\mu$ A

\*  $V_{10-16}$  is typically  $0,5 \cdot V_{14-16} + 1,5 \cdot V_{BE}$ .

\*\* Or control inputs open ( $R_{11,12,13-16} > 33$  M $\Omega$ ).

## APPLICATION INFORMATION

$V_P = 20 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; measured in Fig. 1;  $R_S = 47 \text{ k}\Omega$ ;  $C_i = 0,1 \text{ }\mu\text{F}$ ;  $R_{\text{bias}} = 470 \text{ k}\Omega$ ;  $R_L = 4,7 \text{ k}\Omega$ ;  $C_L = 100 \text{ pF}$  (unless otherwise specified)

Voltage gain	$G_V$	typ.	-1,5 dB	
Output voltage variation when switching the inputs	$\Delta V_{9-16}$	} typ.	10 mV	
	$\Delta V_{15-16}$		< 100 mV	
Total harmonic distortion over most of signal range (see Fig. 4)	$d_{\text{tot}}$	typ.	0,01 %	
		$V_i = 5 \text{ V}$ ; $f = 1 \text{ kHz}$	typ.	0,02 %
		$V_i = 5 \text{ V}$ ; $f = 20 \text{ Hz to } 20 \text{ kHz}$	typ.	0,03 %
Output signal handling $d_{\text{tot}} = 0,1\%$ ; $f = 1 \text{ kHz}$ (r.m.s. value)	$V_{o(\text{rms})}$	>	5,0 V	
		typ.	5,3 V	
Noise output voltage (unweighted) $f = 20 \text{ Hz to } 20 \text{ kHz}$ (r.m.s. value)	$V_{n(\text{rms})}$	typ.	5 $\mu\text{V}$	
Noise output voltage (weighted) $f = 20 \text{ Hz to } 20 \text{ kHz}$ (in accordance with DIN 45405)	$V_n$	typ.	12 $\mu\text{V}$	
Amplitude response $V_i = 5 \text{ V}$ ; $f = 20 \text{ Hz to } 20 \text{ kHz}$ ; $C_i = 0,22 \text{ }\mu\text{F}$	$\Delta V_{9-16}$ ; $\Delta V_{15-16}$ }	} <	0,1 dB *	
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $f = 1 \text{ kHz}$	$\alpha$	typ.	75 dB **	
Crosstalk between switched-on inputs and the outputs of the other channels	$\alpha$	typ.	90 dB **	

\* The lower cut-off frequency depends on values of  $R_{\text{bias}}$  and  $C_i$ .

\*\* Depends on external circuitry and  $R_S$ . The value will be fixed mostly by capacitive crosstalk of the external components.



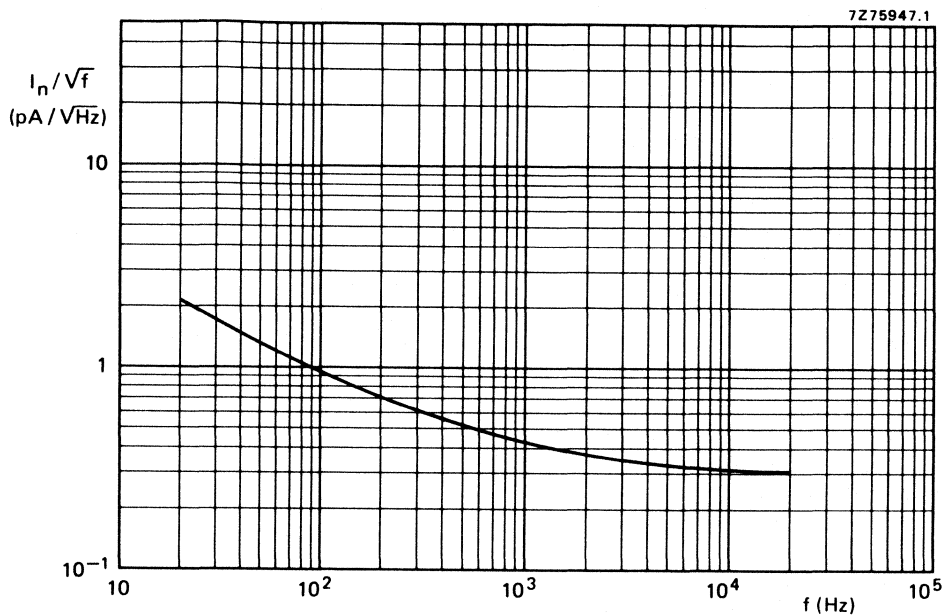


Fig. 2 Equivalent input noise current.

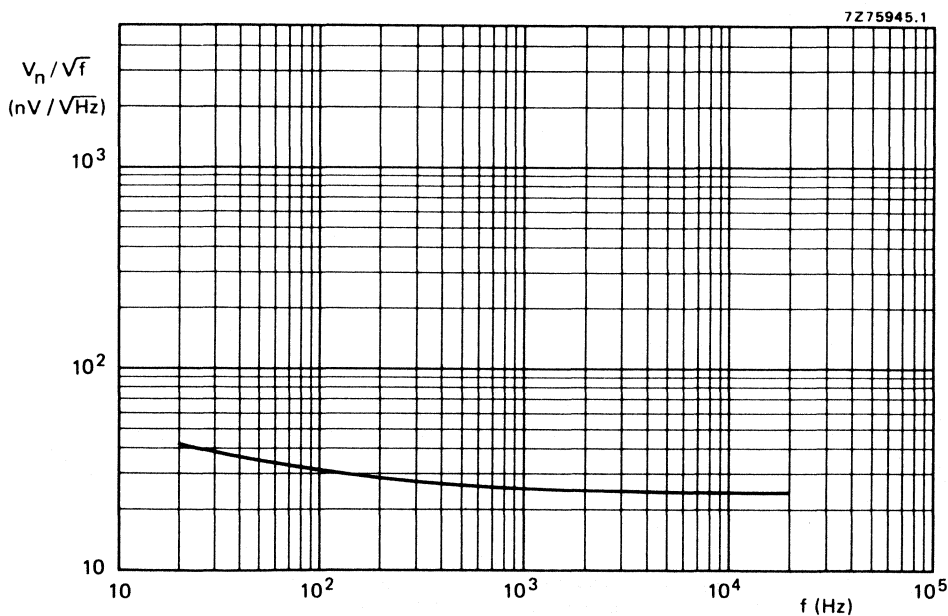


Fig. 3 Equivalent input noise voltage.

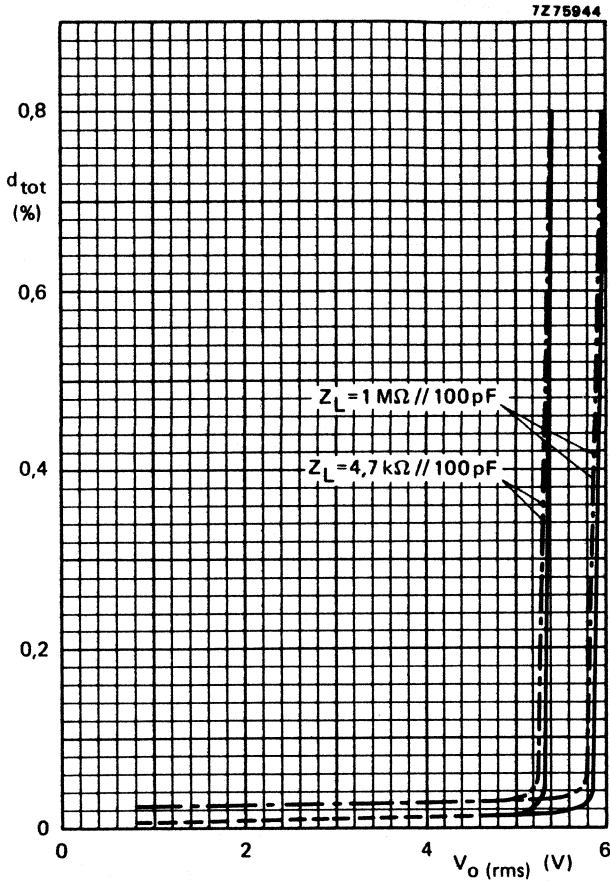


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.  
—  $f = 1\text{ kHz}$ ; - - -  $f = 20\text{ kHz}$ .

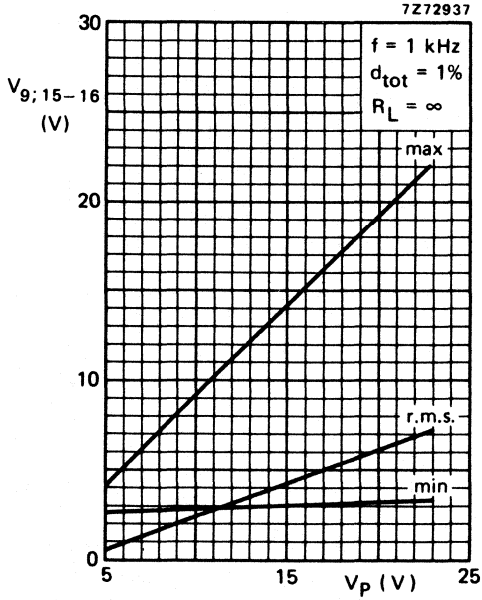


Fig. 5 Output voltage as a function of supply voltage.

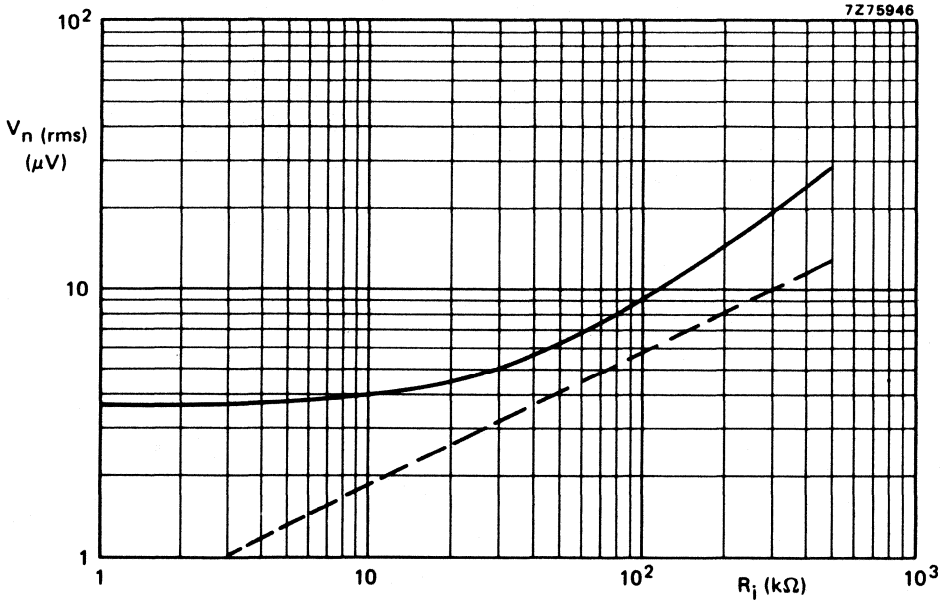


Fig. 6 Noise output voltage as a function of input resistance;  $G_V = 1$ ;  $f = 20 \text{ Hz to } 20 \text{ kHz}$ .  
 —  $V_n \text{ (output)}$ ; - - -  $V_n \text{ (R}_i\text{)}$ .



## APPLICATION NOTES

## Input protection circuit and indication

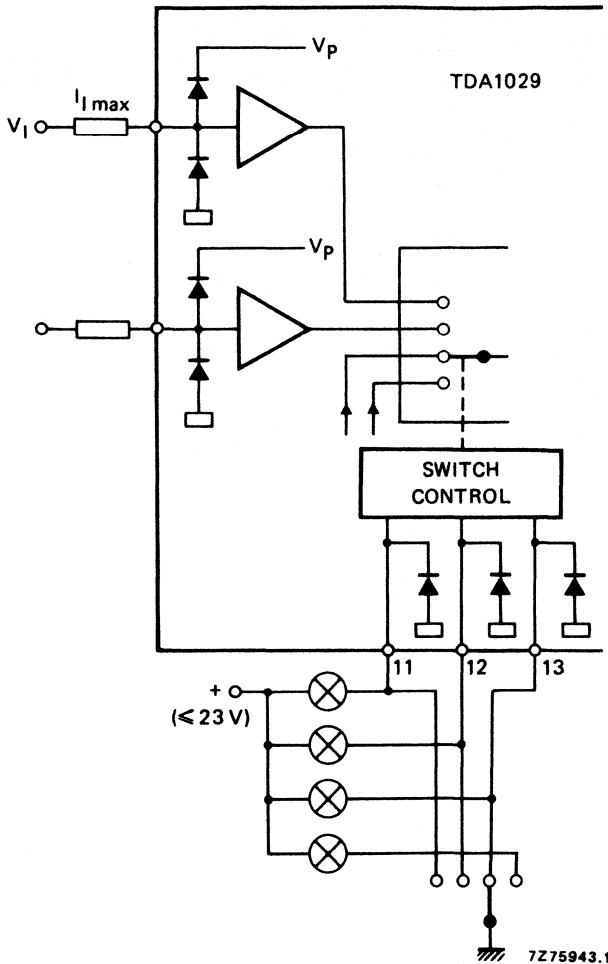


Fig. 7 Circuit diagram showing input protection and indication.

**Unused signal inputs**

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

**Circuits with standby operation**

The control inputs (pins 11, 12 and 13) are high-ohmic at  $V_{SH} \leq 20\text{ V}$  ( $I_{SH} \leq 1\ \mu\text{A}$ ), as well as, when the supply voltage (pin 14) is switched off.

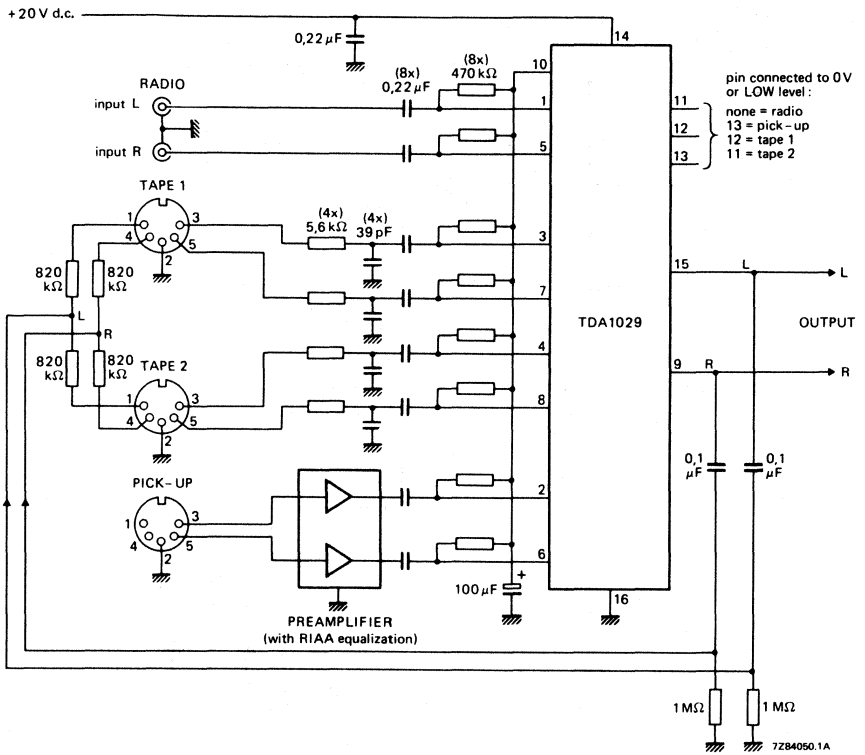


Fig. 8 TDA1029 connected as a four input stereo source selector.

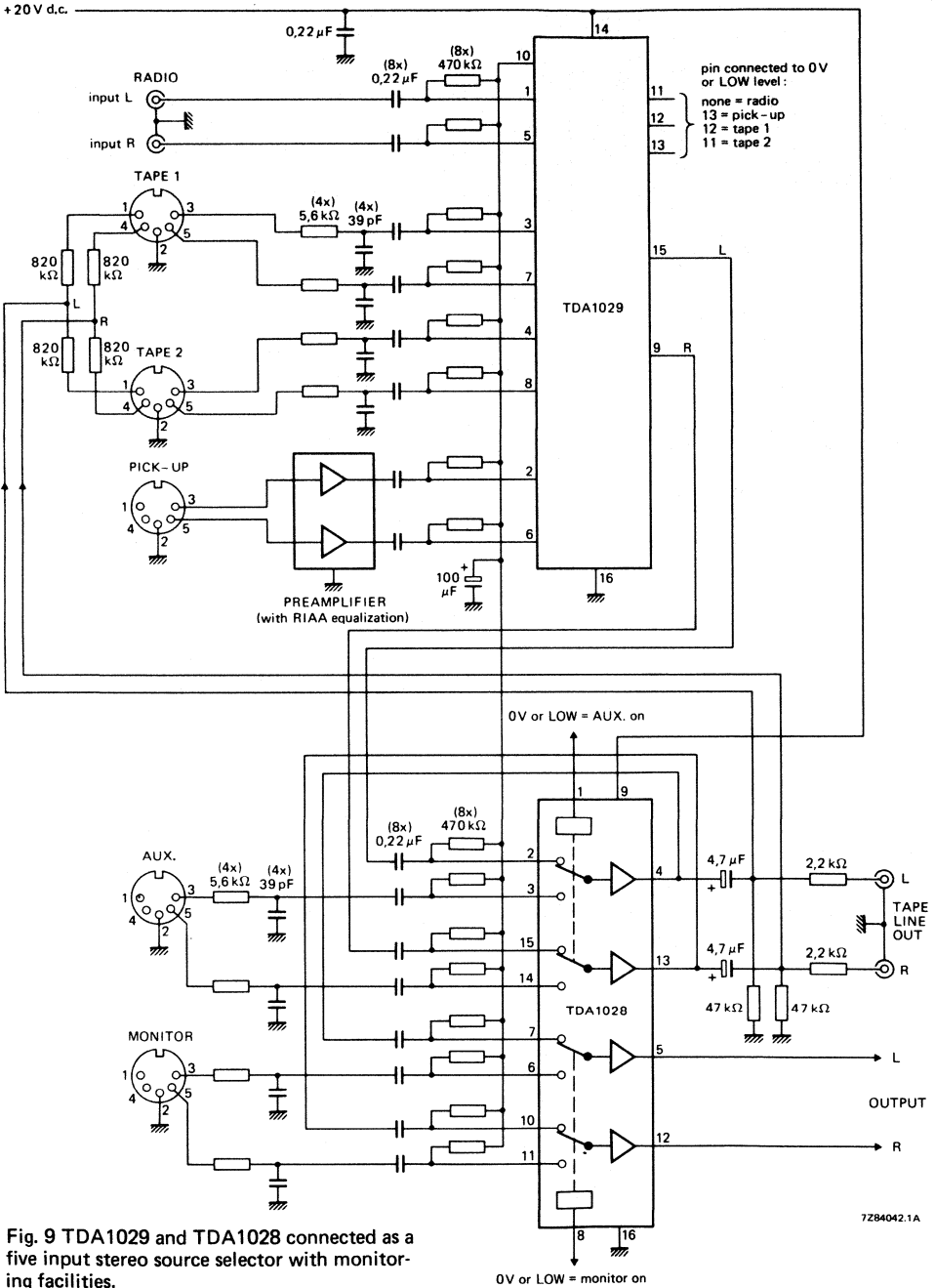


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

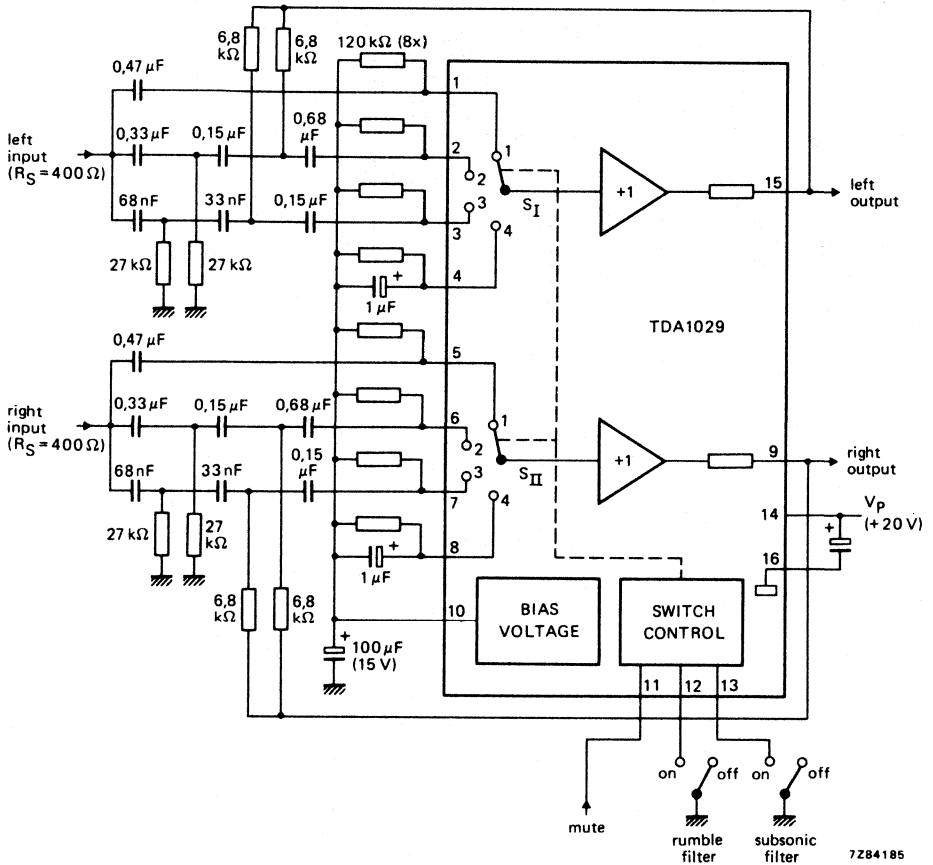


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	V11-16	V12-16	V13-16
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

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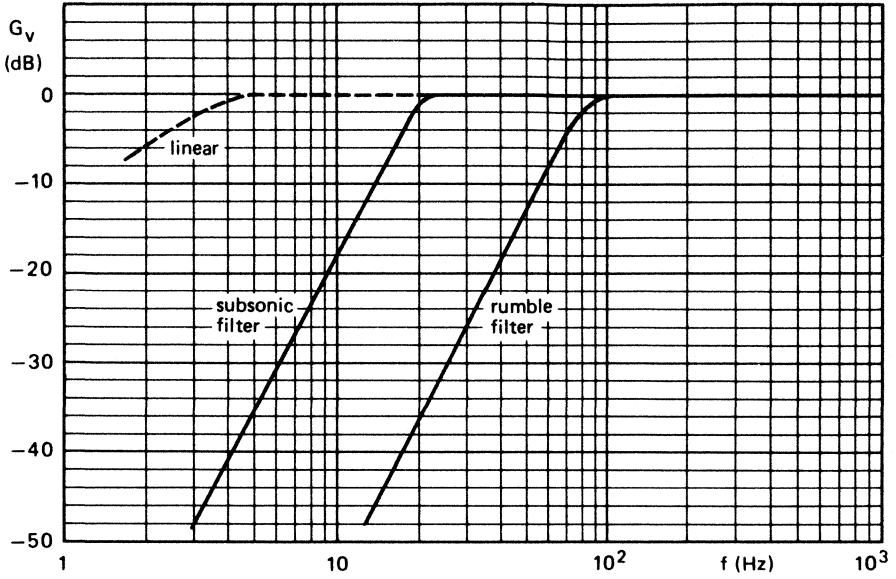


Fig. 11 Frequency response curves for the circuit of Fig. 10.





## MOTOR SPEED REGULATOR WITH THERMAL SHUT-DOWN

The TDA1059B is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

### QUICK REFERENCE DATA

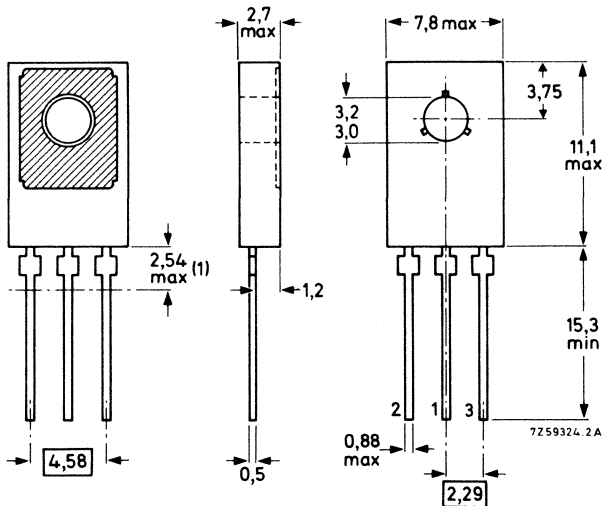
Supply voltage	$V_P = V_{2-1}$	typ.	9 V
			3,3 to 16 V
Internal reference voltage	$V_{ref}$	typ.	1,3 V
Drop-out voltage	$V_{3-1}$	typ.	1,8 V
Limited output current	$I_{3lim}$	typ.	0,6 A
Multiplication coefficient	k	typ.	9

### PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.

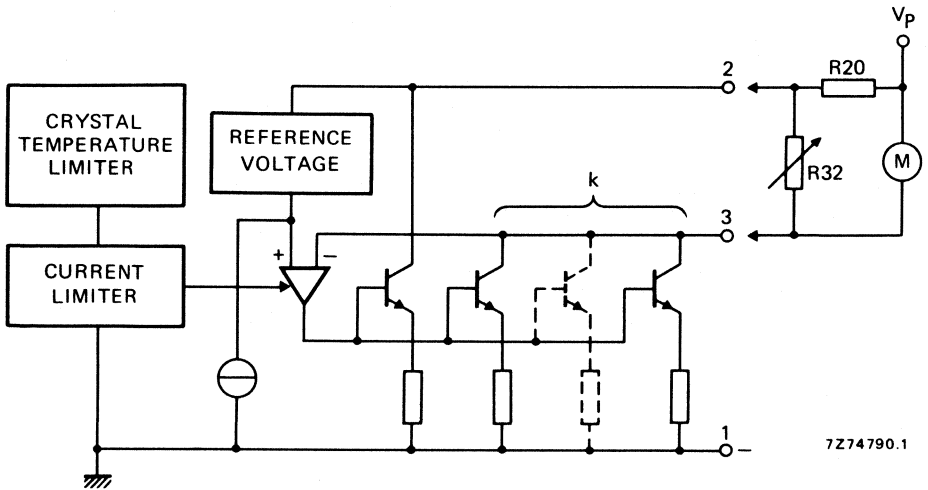


Fig. 2 Functional diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{2-1}$	max.	16 V
Storage temperature	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature (see Fig. 3 and note)	$T_{amb}$		-25 to + 130 °C

**THERMAL RESISTANCE**

From junction to case	$R_{th\ j-c}$	=	10 K/W
From junction to ambient	$R_{th\ j-a}$	=	100 K/W

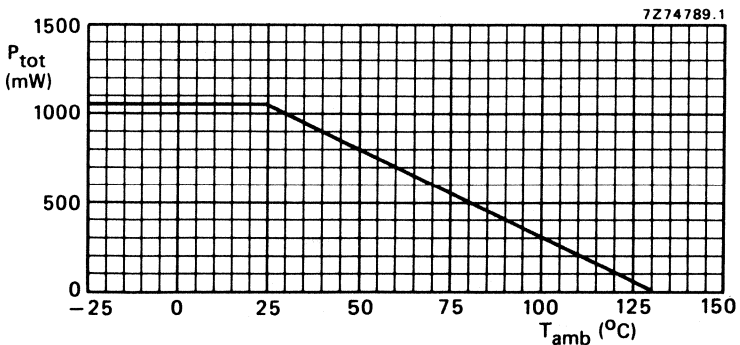


Fig. 3 Power derating curve.

**Note**

At ambient temperatures above 130 °C, the crystal temperature limiter decreases the internal power consumption.

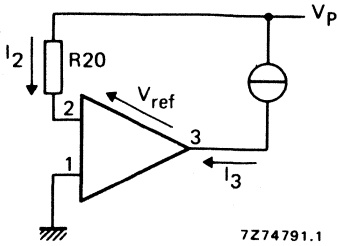


## CHARACTERISTICS

$V_P = 9 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ;  $R_{20} = 0$ ; heatsink with  $R_{\text{th}} = 100 \text{ K/W}$  and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4.

		min.	typ.	max.
Supply voltage	$V_P = V_{2-1}$	3,3	9	16 V
Internal reference voltage $V_P = 3,3 \text{ V}$ ; $I_3 = 80 \text{ mA}$	$V_{\text{ref}}$	1,24	1,3	1,36 V
Drop-out voltage $I_3 = 80 \text{ mA}$ ; $\Delta V_{\text{ref}} = 5\%$	$V_{3-1}$	—	1,8	2,06 V
Quiescent current; $I_3 = 0$	$I_q$	1,8	2,3	2,8 mA
Limited output current*	$I_{3\text{lim}}$	0,3	0,6	1 A
Multiplication coefficient $I_3 = 50 \text{ mA} \pm 10 \text{ mA}$	$k = \frac{\Delta I_3}{\Delta I_2}$	8,5	9	9,5
Line regulation				
$V_P = 3,3 \text{ to } 16 \text{ V}$ at $I_3 = 50 \text{ mA}$				
reference voltage variation	$\frac{\Delta V_{\text{ref}}}{V_{\text{ref}}} / \Delta V_P$	-0,115	0	+ 0,115 %/V
multiplication coefficient variation $I_3 = 50 \pm 10 \text{ mA}$	$\frac{\Delta k}{k} / \Delta V_P$	—	0,86	— %/V
input current variation; $I_3 = 50 \text{ mA}$	$\frac{\Delta I_2}{\Delta V_P}$	-15	0	+ 20 $\mu\text{A/V}$
Load regulation				
reference voltage variation $I_3 = 20 \text{ to } 80 \text{ mA}$	$\frac{\Delta V_{\text{ref}}}{V_{\text{ref}}} / \Delta I_3$	0	19	38,5 %/A
multiplication coefficient variation $I_3 = 30 \pm 10 \text{ to } 70 \pm 10 \text{ mA}$	$\frac{\Delta k}{k} / \Delta I_3$	-0,075	0	+ 0,075 %/mA
Temperature coefficient				
$I_3 = 50 \text{ mA}$ ; $T_{\text{amb}} = -15 \text{ to } +65 \text{ }^\circ\text{C}$				
reference voltage variation	$\frac{\Delta V_{\text{ref}}}{V_{\text{ref}}} / \Delta T_{\text{amb}}$	-0,03	0	+ 0,03 %/K
multiplication coefficient variation $\Delta I_3 = \pm 10 \text{ mA}$	$\frac{\Delta k}{k} / \Delta T_{\text{amb}}$	—	0,008	— %/K
input current variation	$\frac{\Delta I_2}{\Delta T_{\text{amb}}}$	-2	0	+ 2 $\mu\text{A/K}$

\* If the motor is stopped by a mechanical brake, the current limitation is effective in the supply voltage range. If the motor is short-circuited, the TDA1059B will be damaged if the supply voltage is higher than 10 V due to parasitic oscillations.

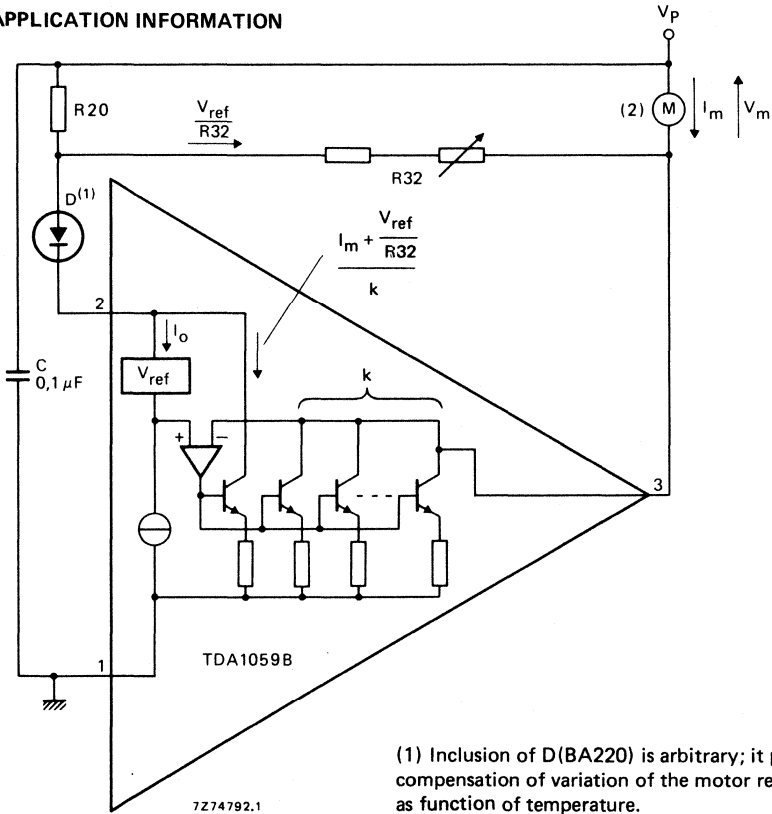


Note

For start operation:  $V_{ref}$  must start with final  $V_p = 6,7\text{ V}$  and a time constant of  $3\tau = 100\text{ ms}$  in which  $\tau = R.C$ ;  $R$  = source impedance,  $C$  = by-pass capacitor.

Fig. 4 Test circuit.

APPLICATION INFORMATION



(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806;  $n = 2000\text{ rev/min}$ ;  $R_{20} = 180\ \Omega (\pm 2\%)$ ;  $R_{32} = 100\ \Omega + 100\ \Omega$  (variable).

Fig. 5 Example of using the TDA1059B in a d.c. motor speed regulation circuit.

**Motor equations**

$$\begin{aligned}
 E_m &= \alpha_1 n & \text{where: } \alpha_1, \alpha_2 &= \text{motor constant} \\
 I_m &= \alpha_2 r & n &= \text{number of revolutions} \\
 V_m &= E_m + R_m I_m & r &= \text{motor torque} \\
 & & E_m &= \text{back electromotive force} \\
 & & R_m &= \text{motor resistance}
 \end{aligned}$$

The back electromotive force ( $E_m$ ) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left( \frac{R_{20}}{k} - R_m \right) I_m + V_{ref} \left\{ 1 + \frac{R_{20}}{R_{32}} \left( 1 + \frac{1}{k} \right) \right\} + R_{20} I_o$$

and including diode D, as:

$$E_m = \left( \frac{R_{20}}{k} - R_m \right) I_m + (V_{ref} + V_D) \left\{ 1 + \frac{R_{20}}{R_{32}} \left( 1 + \frac{1}{k} \right) \right\} + R_{20} I_o$$

Speed regulation is constant when  $E_m$  is independent of  $I_m$  variations; this will be obtained when  $R_{20} = kR_m$ .

$E_m$ , and therefore the motor speed, is regulated by  $R_{32}$ . A practical condition for stability is  $R_{20} < kR_m$ .





## MOTOR SPEED REGULATOR

The TDA1059C is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

## QUICK REFERENCE DATA

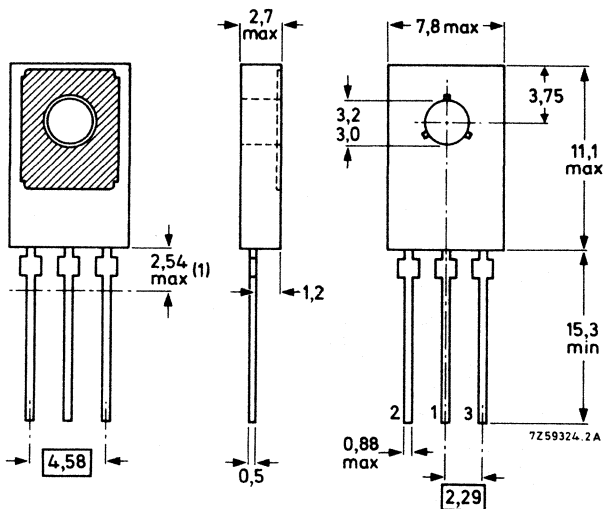
Supply voltage	$V_P = V_{2-1}$	typ. 9 V 2,5 to 16 V
Internal reference voltage	$V_{ref}$	typ. 1,1 V
Drop-out voltage	$V_{3-1}$	typ. 1,0 V
Limited output current	$I_{3lim}$	typ. 0,6 A
Multiplication coefficient	k	typ. 9

## PACKAGE OUTLINE

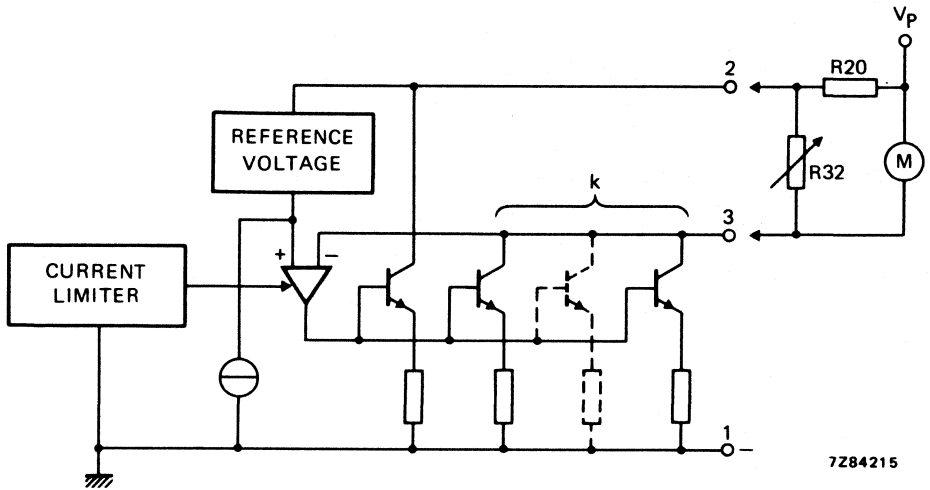
Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.



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Fig. 2 Functional diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p = V_{2-1}$	max.	16 V
Storage temperature	$T_{stg}$		-55 to +150 °C
Operating ambient temperature (see Fig. 3)	$T_{amb}$		-25 to +150 °C

**THERMAL RESISTANCE**

From junction to case	$R_{th\ j-c}$	=	10 K/W
From junction to ambient	$R_{th\ j-a}$	=	100 K/W

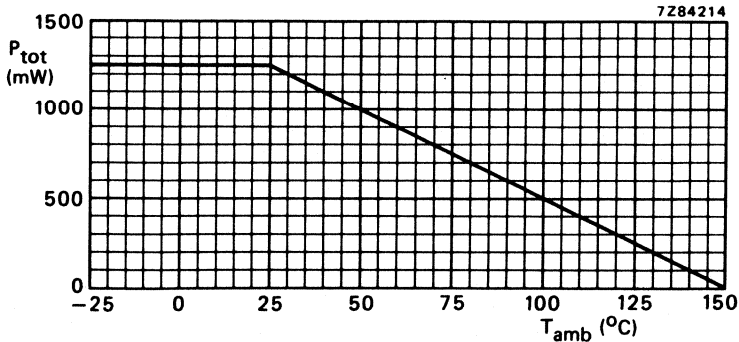


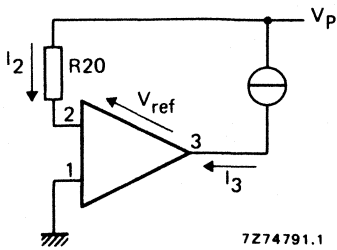
Fig. 3 Power derating curve.

**CHARACTERISTICS**

$V_P = 9\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $R_{20} = 0$ ; heatsink with  $R_{th} = 100\text{ K/W}$  and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4

		min.	typ.	max.
Supply voltage	$V_P = V_{2-1}$	2,5	9	15 V
Internal reference voltage $V_P = 2,5\text{ V}$ ; $I_3 = 80\text{ mA}$	$V_{ref}$	1,05	1,1	1,15 V
Drop-out voltage $I_3 = 80\text{ mA}$ ; $\Delta V_{ref} = 2\%$	$V_{3-1}$	—	1,03	1,25 V
Quiescent current; $I_3 = 0$	$I_q$	2,2	2,7	3,2 mA
Limited output current	$I_{3lim}$	0,3	0,45	1 A
Multiplication coefficient $I_3 = 50\text{ mA} \pm 10\text{ mA}$	$k = \frac{\Delta I_3}{\Delta I_2}$	8,5	9	9,5
Line regulation $V_P = 2,5\text{ to }15\text{ V}$ at $I_3 = 50\text{ mA}$				
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_P$	0,04	0,18	0,22 %/V
multiplication coefficient variation $I_3 = 50 \pm 10\text{ mA}$	$\frac{\Delta k}{k} / \Delta V_P$	—	0,86	— %/V
input current variation; $I_3 = 50\text{ mA}$	$\frac{\Delta I_2}{\Delta V_P}$	0	15	30 $\mu\text{A/V}$
Load regulation				
reference voltage variation $I_3 = 20\text{ to }80\text{ mA}$	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_3$	0	30	45,5 %/A
multiplication coefficient variation $I_3 = 30 \pm 10\text{ to }70 \pm 10\text{ mA}$	$\frac{\Delta k}{k} / \Delta I_3$	—	0,04	— %/mA
Temperature coefficient $I_3 = 50\text{ mA}$ ; $T_{amb} = -15\text{ to }+65\text{ }^\circ\text{C}$				
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$	-0,036	0	+0,036 %/K
multiplication coefficient variation $\Delta I_3 = \pm 10\text{ mA}$	$\frac{\Delta k}{k} / \Delta T_{amb}$	—	0,008	— %/K
input current variation	$\frac{\Delta I_2}{\Delta T_{amb}}$	—	4	— $\mu\text{A/K}$



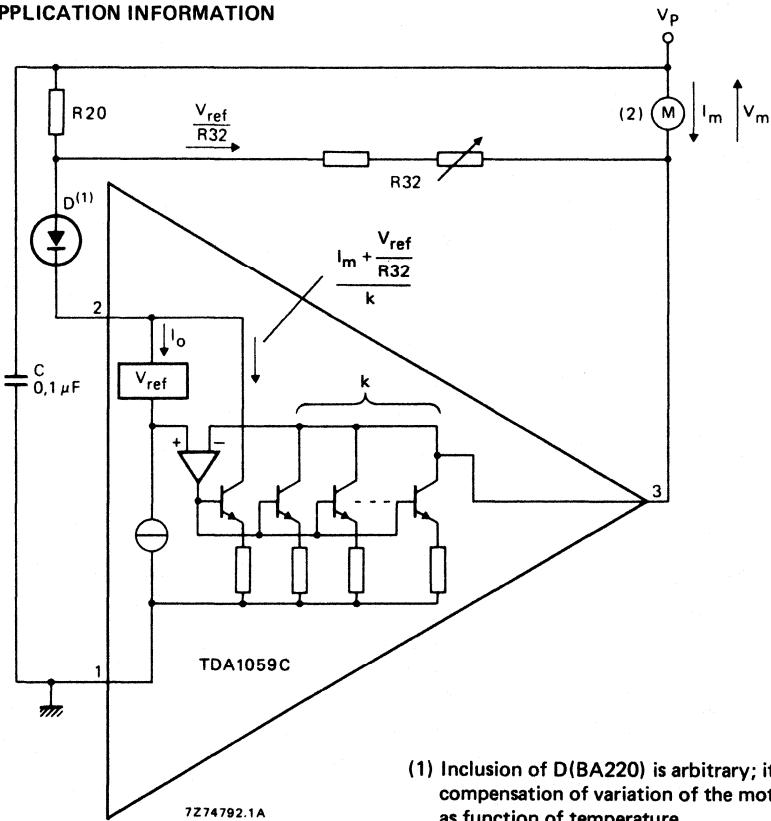


**Note**

For start operation:  $V_{ref}$  must start with final  $V_P = 6\text{ V}$  and a time constant of  $3\tau = 100\text{ ms}$  in which  $\tau = R.C.$ ;  $R$  = source impedance,  $C$  = by-pass capacitor.

Fig. 4 Test circuit.

**APPLICATION INFORMATION**



(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806;  $n = 2000\text{ rev/min}$ ;  $R20 = 180\ \Omega (\pm 2\%)$ ;  $R32 = 39\ \Omega + 47\ \Omega$  (variable).

Fig. 5 Example of using the TDA1059C in a d.c. motor speed regulation circuit.



**Motor equations**

$E_m = \alpha_1 n$                       where:  $\alpha_1, \alpha_2 =$  motor constant  
 $I_m = \alpha_2 r$                          $n =$  number of revolutions  
 $V_m = E_m + R_m I_m$                  $r =$  motor torque  
     $E_m =$  back electromotive force  
     $R_m =$  motor resistance

The back electromotive force ( $E_m$ ) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left( \frac{R_{20}}{k} - R_m \right) I_m + V_{ref} \left\{ 1 + \frac{R_{20}}{R_{32}} \left( 1 + \frac{1}{k} \right) \right\} + R_{20} \cdot I_o$$

and including diode D, as:

$$E_m = \left( \frac{R_{20}}{k} - R_m \right) I_m + \left( V_{ref} + V_D \right) \left\{ 1 + \frac{R_{20}}{R_{32}} \left( 1 + \frac{1}{k} \right) \right\} + R_{20} \cdot I_o$$

Speed regulation is constant when  $E_m$  is independent of  $I_m$  variations; this will be obtained when  $R_{20} = kR_m$ .

$E_m$ , and therefore the motor speed, is regulated by R32. A practical condition for stability is  $R_{20} < kR_m$ .





## AM RECEIVER CIRCUIT

The TDA1072 is a monolithic integrated AM receiver circuit provided with the following functions:

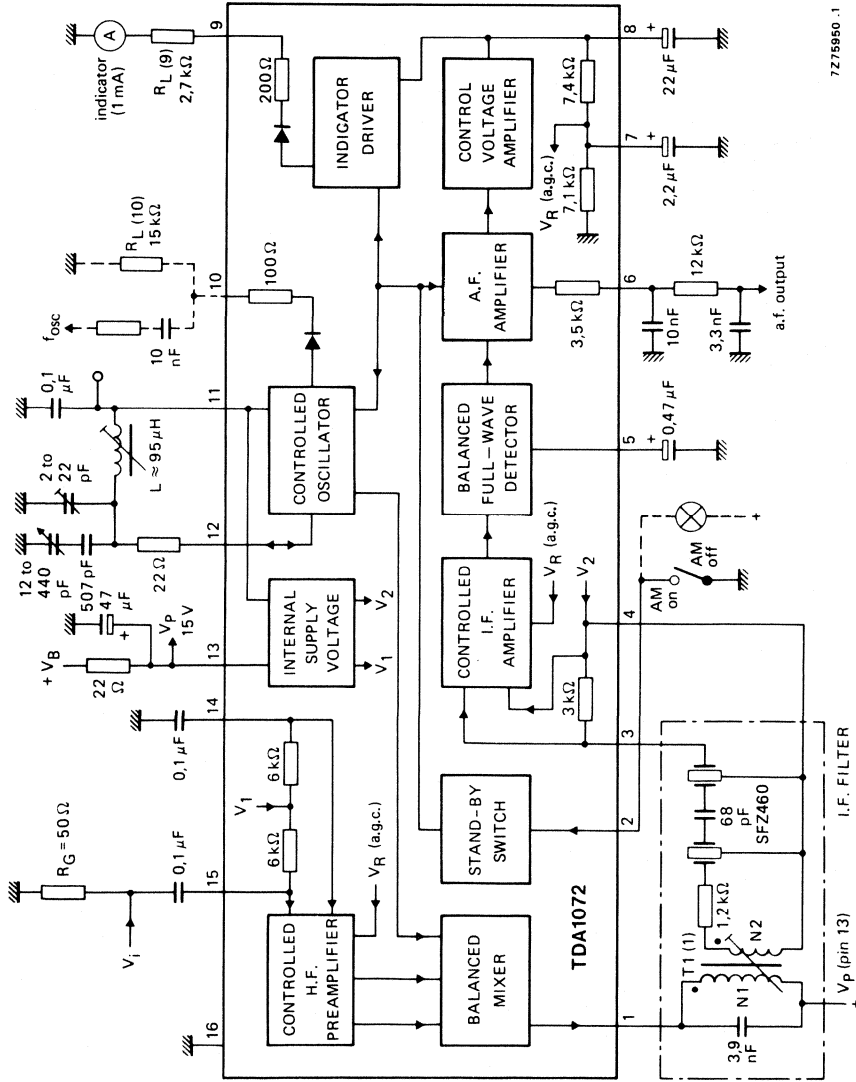
- controlled h.f. preamplifier
- multiplicative balanced mixer
- separate oscillator with amplitude control
- i.f. amplifier with gain control
- balanced full-wave detector
- a.f. preamplifier
- internal a.g.c. voltage
- amplifier for field-strength indication
- electronic stand-by on/off switch

## QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_p$	typ.	15 V
Supply current	$I_p$	typ.	22 mA
H.F. input voltage			
$S + N/N = 6$ dB	$V_i$	typ.	2,2 $\mu V$
$S + N/N = 26$ dB	$V_i$	typ.	30 $\mu V$
H.F. input voltage; $d_{tot} = 3\%$ ; $m = 80\%$	$V_i$	typ.	650 mV
A.F. output voltage; $V_i = 2$ mV	$V_o$	typ.	340 mV
Total distortion	$d_{tot}$	typ.	0,5 %
Input voltage range for $\Delta V_o = 6$ dB	$\Delta V_i$	typ.	91 dB
Oscillator frequency range	$f_{osc}$		0,6 to 31 MHz
Oscillator voltage amplitude	$V_{osc}$	typ.	140 mV
Field-strength indication range	$\Delta V_i$	typ.	100 dB
-----			
Supply voltage range	$V_p$		7,5 to 18 V
Ambient temperature range	$T_{amb}$		-30 to +80 °C

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



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(1) T1 : N1/N2 = 34/9; O<sub>0</sub> = 65; Q<sub>L</sub> = 700 Ω at R<sub>L</sub>(3) = 3 kΩ; Z<sub>11</sub> = 5.2 kΩ.

Fig. 1 Block diagram with external components; used as test circuit.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-16}$	max.	23 V
Voltage on pin 2	$V_{2-16}$		0 to 23 V
<b>H.F. inputs</b>			
Voltages between:			
pins 14 and 15	$\pm V_{14-15}$	max.	12 V
pins 14 and 16	$V_{14-16}$	max.	$V_P$ V
pins 15 and 16	$V_{15-16}$	max.	$V_P$ V
Or currents:			
pin 14	$\pm I_{14}$	max.	10 mA
pin 15	$\pm I_{15}$	max.	10 mA
Storage temperature range	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature range	$T_{amb}$		-30 to + 80 °C

**CHARACTERISTICS**

$V_P = 15$  V;  $T_{amb} = 25$  °C;  $f_i = 1$  MHz (h.f.),  $R_G = 50$   $\Omega$ ;  $f_m = 0,4$  kHz;  $m = 30\%$ ;  
i.f. frequency = 460 kHz; unless otherwise specified

Supply voltage range (pin 13)	$V_P$		7,5 to 18 V
Supply current; without load ( $I_{L(11)} = 0$ )	$I_P$	typ.	22 mA 15 to 30 mA

**H.F. preamplifier and mixer**

D.C. input voltages	$V_{14-16}; V_{15-16}$	typ.	2,75 ( $4V_{BE}$ ) V
Input impedance			
$V_i < 300$ $\mu$ V	$Z_{i(14-16)}; Z_{i(15-16)}$	typ.	6 k $\Omega$ 6 pF
$V_i > 10$ mV	$Z_{i(14-16)}; Z_{i(15-16)}$	typ.	9 k $\Omega$ 2,5 pF
Output impedance			
	$Z_{o(1-16)}$	>	200 k $\Omega$ 4 pF
Maximum conversion conductance	$S_M$	typ.	5,5 mA/V*
Maximum i.f. output voltage (peak-to-peak value)	$V_{o(1)(p-p)}$	typ.	2,8 V
Output current capability	$I_{o(1)}$	typ.	1 mA
Control range of preamplifier	$\Delta S_M$	typ.	30 dB
Maximum h.f. input voltage (peak-to-peak value)	$V_{i(14-15)(p-p)}$	typ.	2,8 V

\*  $S_M$  is defined as  $I_{o(1)}/V_i$ .

**CHARACTERISTICS** (continued)**Oscillator**

Frequency range	$f_{osc(12)}$	0,6 to 31 MHz
Oscillator impedance range	$Z_L(12)$	1 to 200 k $\Omega$
Controlled oscillator amplitude	$V_{osc(12)}$	typ. 140 mV < 200 mV
D.C. output voltage ( $I_{L(11)} = 0$ )	$V_{11-16}$	typ. $V_p - 1,3$ V
Output load current range	$-I_{L(11)}$	0 to 15 mA
Output resistance; $I_{L(11)} = 5 \pm 0,5$ mA	$R_{O(11)}$	typ. 7 $\Omega$

**Oscillator frequency output** (pin 10)

Output voltage (peak-to-peak value) $R_{10-16} = 15$ k $\Omega$ ( $R_{L(10)}$ )	$V_{O(10)(p-p)}$	typ. 200 mV
Output resistance	$R_{O(10)}$	typ. 150 $\Omega$
Allowable output current (peak value)	$I_{O(10)M}$	< 2 mA

**I.F. amplifier and a.f. stage**

D.C. input voltages	$V_{3-16}; V_{4-16}$	typ. 2 V typ. 3 k $\Omega$
Input impedance	$Z_i(3)$	2,4 to 3,9 k $\Omega$ typ. 4 pF
Max. i.f. input voltage; $m = 80\%$ ; $d_{tot} = 3\%$	$V_i(3)$	typ. 75 mV
Control range; $V_o = -6$ dB	$\Delta V_i$	typ. 62 dB
A.F. output voltage; $V_i(3) = 2$ mV; without load	$V_{O(6)}$	typ. 350 mV
A.F. output resistance	$R_{O(6)}$	typ. 3,5 k $\Omega$

**Field-strength indication**

D.C. indicator voltage $V_i = 0$ ; $R_{L(9)} = 2,7$ k $\Omega$	$V_{9-16}$	typ. 0 mV < 140 mV
$V_i = 500$ mV; $R_{L(9)} = 2,7$ k $\Omega$	$V_{9-16}$	typ. 2,8 V 2,5 to 3,1 V
Output current capability	$-I_g$	> 1,2 mA
Output resistance; $-I_g = 0,5$ mA	$R_{O(9)}$	typ. 250 $\Omega$
Leakage voltage at the output; $\pm I_g \leq 1$ $\mu$ A; at AM switch off ( $V_{2-16} \geq 3,5$ V)	$V_{9-16}$	typ. 6 V

**Stand-by switch**

Switching voltage	$V_{2-16}$	typ.	2,6 V
Required control voltage*			
AM on	$V_{2-16}$	<	2 V
AM off	$V_{2-16}$	>	3,5 V**
Input current			
AM on; switching current	$-I_2$	<	100 $\mu$ A
AM off; leakage current ( $V_{2-16} = V_{3-16}$ )	$\pm I_2$	<	1 $\mu$ A

**APPLICATION INFORMATION**

$V_P = 15$  V;  $T_{amb} = 25$  °C; measured in Fig. 1;  $f_i = 1$  MHz (h.f.);  $f_m = 0,4$  kHz;  $m = 30\%$ ; unless otherwise specified

**H.F. input voltage**

S + N/N = 6 dB	$V_i$	typ.	2,2 $\mu$ V
S + N/N = 10 dB	$V_i$	typ.	3,5 $\mu$ V
S + N/N = 26 dB	$V_i$	typ.	30 $\mu$ V
S + N/N = 46 dB	$V_i$	typ.	550 $\mu$ V

**H.F. input voltage for a.g.c. operation**

$V_i$	typ.	14 $\mu$ V
-------	------	------------

**Control range for  $\Delta V_O = 6$  dB**

reference value $V_i = 500$ mV	$\Delta V_i$	typ.	91 dB
--------------------------------	--------------	------	-------

**Maximum h.f. input voltage**

$d_{tot} = 3\%$ ; $m = 80\%$	$V_i$	typ.	0,65 V
$d_{tot} = 3\%$ ; $m = 30\%$	$V_i$	typ.	0,9 V
$d_{tot} = 10\%$ ; $m = 30\%$	$V_i$	typ.	1,3 V

**A.F. output voltage;  $V_i = 2$  mV**

$V_O$	typ.	340 mV
-------	------	--------

**Change of a.f. output voltage;  $V_i = 2$  mV**

$\Delta V_O$	typ.	$\pm 2$ dB
--------------	------	------------

**H.F. input voltage;  $V_O = 60$  mV**

$V_i$	typ.	4 $\mu$ V
-------	------	-----------

**Total distortion of a.f. output voltage**

$V_i = 2$ mV; $m = 80\%$	$d_{tot}$	typ.	0,5 %
$V_i = 500$ mV; $m = 80\%$	$d_{tot}$	typ.	1,8 %
		<	3 %

**Signal plus noise-to-noise ratio of a.f. output voltage**

$V_i = 2$ mV	S + N/N	typ.	50 dB
--------------	---------	------	-------

**I.F. bandwidth ( $-3$  dB)**

B	typ.	4,6 kHz
---	------	---------

**I.F. selectivity**

$\Delta f = \pm 9$ kHz	$S(9)$	typ.	30 dB
$\Delta f = \pm 36$ kHz	$S(36)$	typ.	60 dB

\* At allowable ambient temperature range and supply voltage range.

\*\* Also achieved at open input.

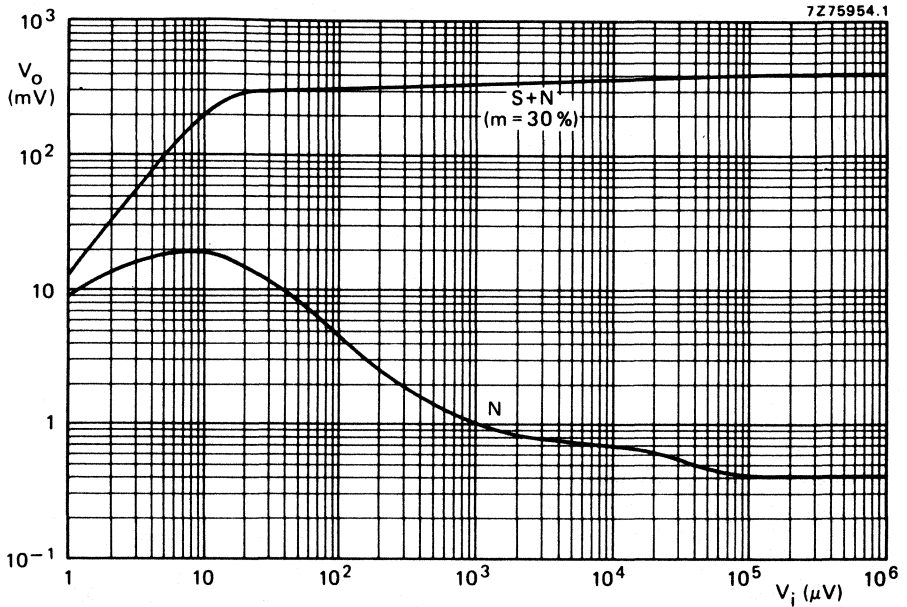


Fig. 2 A.F. output voltage as a function of h.f. input voltage;  $f_i = 1$  MHz (h.f.);  $R_G = 50 \Omega$ ;  $f_m = 0,4$  kHz.

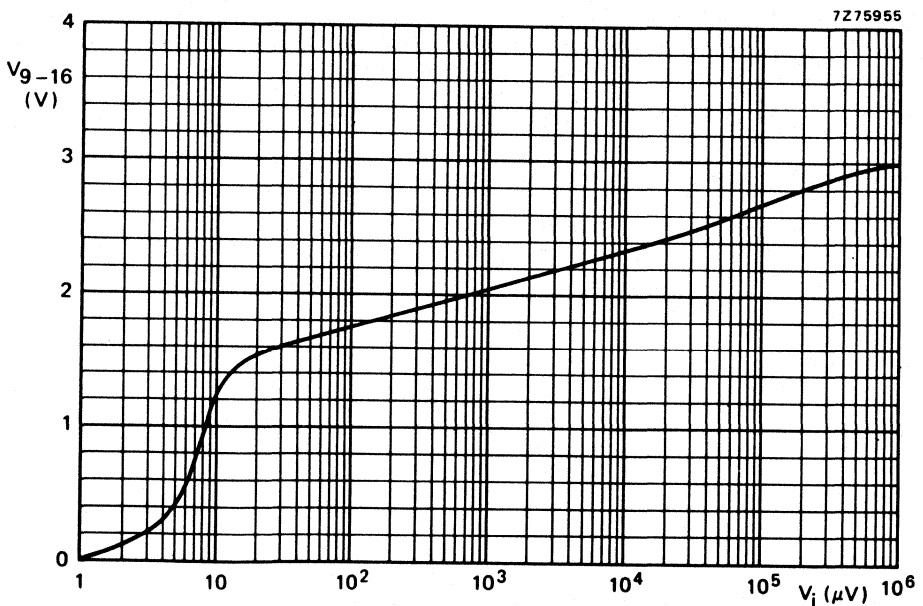


Fig. 3 Indication voltage as a function of h.f. input voltage;  $R_{g-16} = 2,7$  k $\Omega$ .



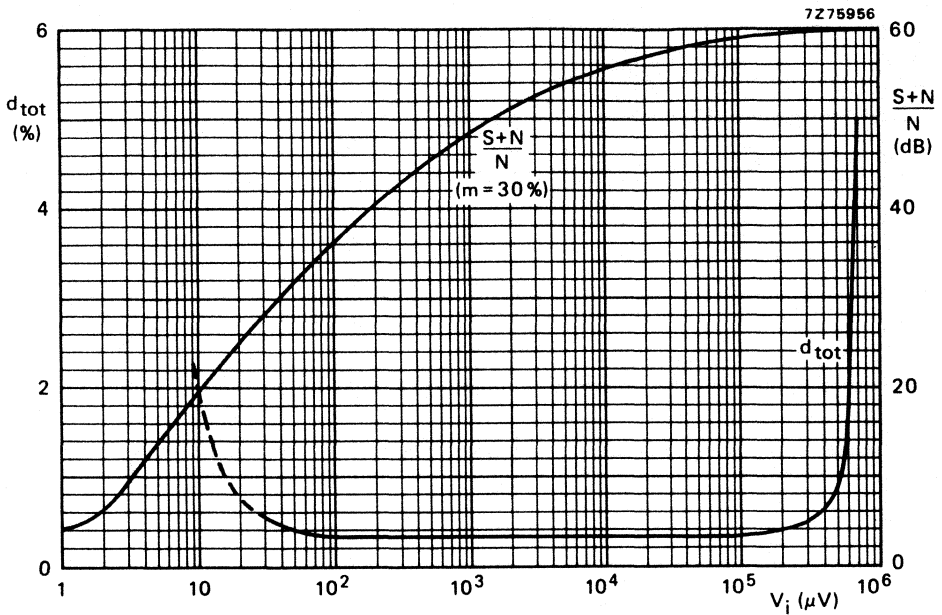


Fig. 4 Total distortion and signal plus noise-to-noise ratio as a function of h.f. input voltage; for  $d_{tot}$ :  $f_m = 0,4$  kHz;  $m = 80\%$ .

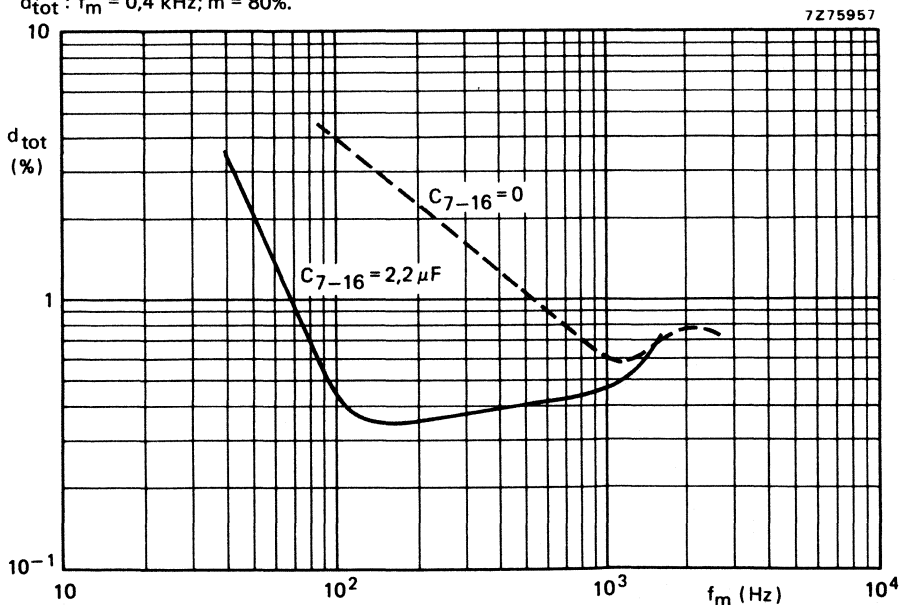


Fig. 5 Total distortion as a function of the modulation frequency;  $V_i = 10$  mV;  $f_i = 1$  MHz;  $m = 80\%$ .  $C_{8-16} = 22 \mu F$ .

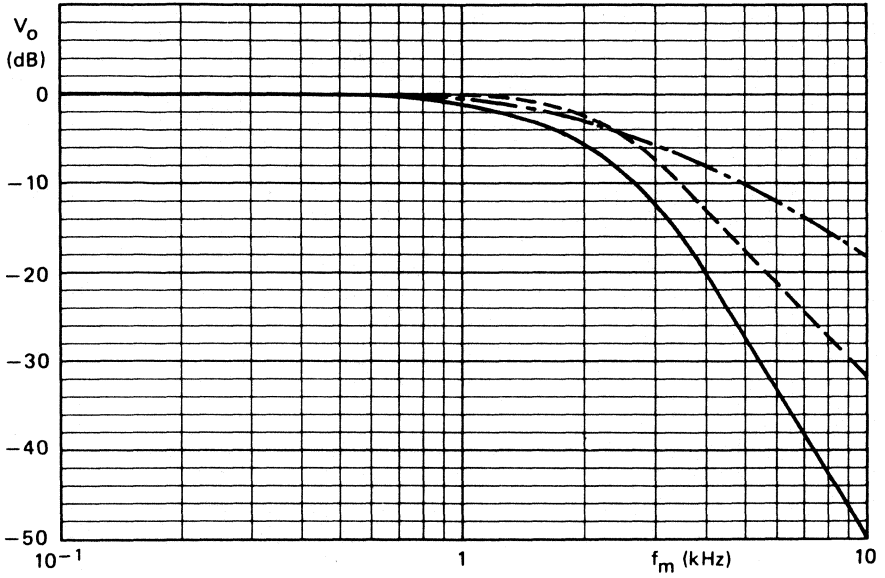
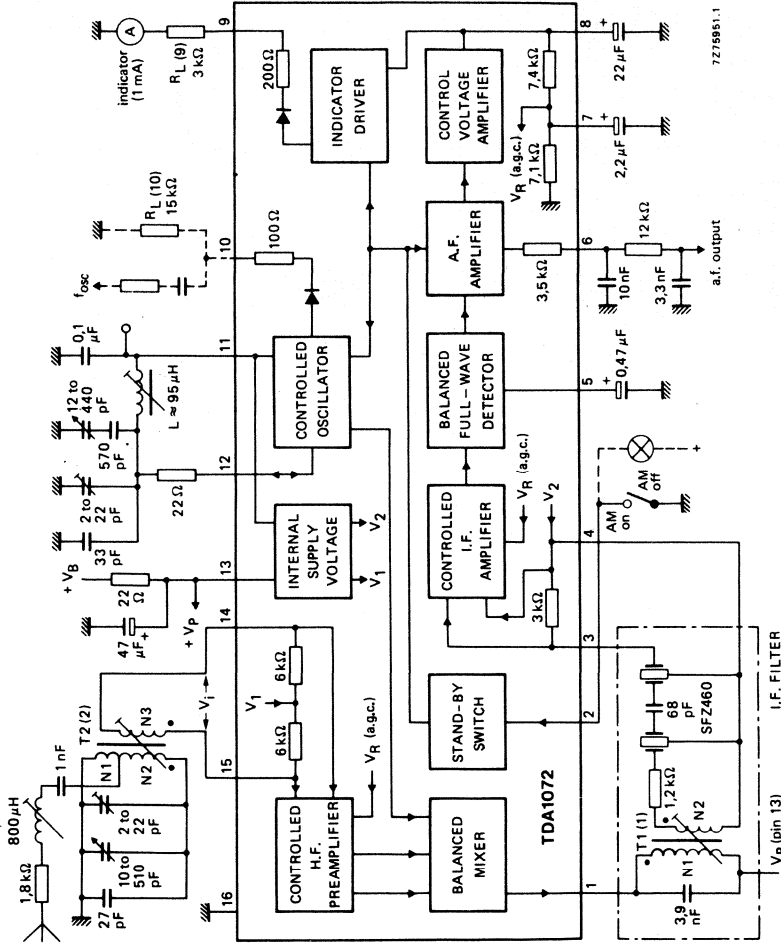


Fig. 6 Frequency responses (wobbled) for various conditions:

- with a.f. and i.f. filter
- - - with i.f. filter
- . - with a.f. filter





(1) T1 : N1/N2 = 34/9; Q<sub>0</sub> = 65; Z<sub>21</sub> = 700 Ω at R<sub>L</sub>(3) = 3 kΩ; Z<sub>11</sub> = 5.2 kΩ.  
 (2) T2 : N1/N2/N3 = 14/67/17; L = 175 μH; Q<sub>0</sub> = 145; Q<sub>L</sub> = 50 (f = 1 MHz); V<sub>i</sub>/V<sub>G</sub> = -6 dB.

Fig. 7 Application circuit diagram of an AM-MW receiver with two double variable tuning capacitors; f<sub>i</sub> = 510 to 1620 kHz (h.f.); f<sub>j</sub> = 460 kHz (i.f.).

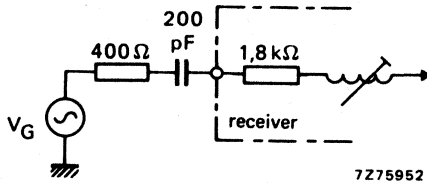
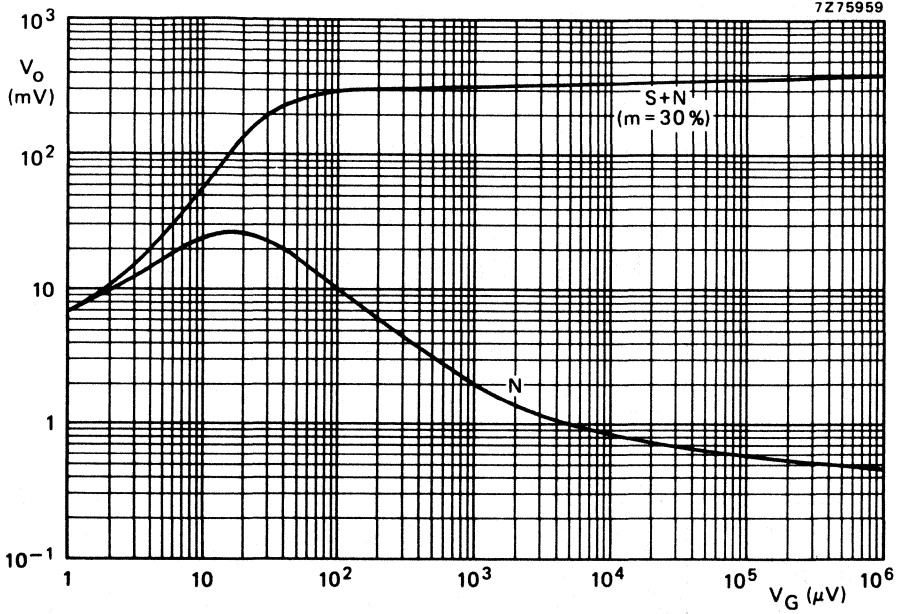


Fig. 8 A.F. output voltage as a function of the h.f. generator input voltage;  $f_i = 1$  MHz (h.f.);  $f_m = 0,4$  kHz.

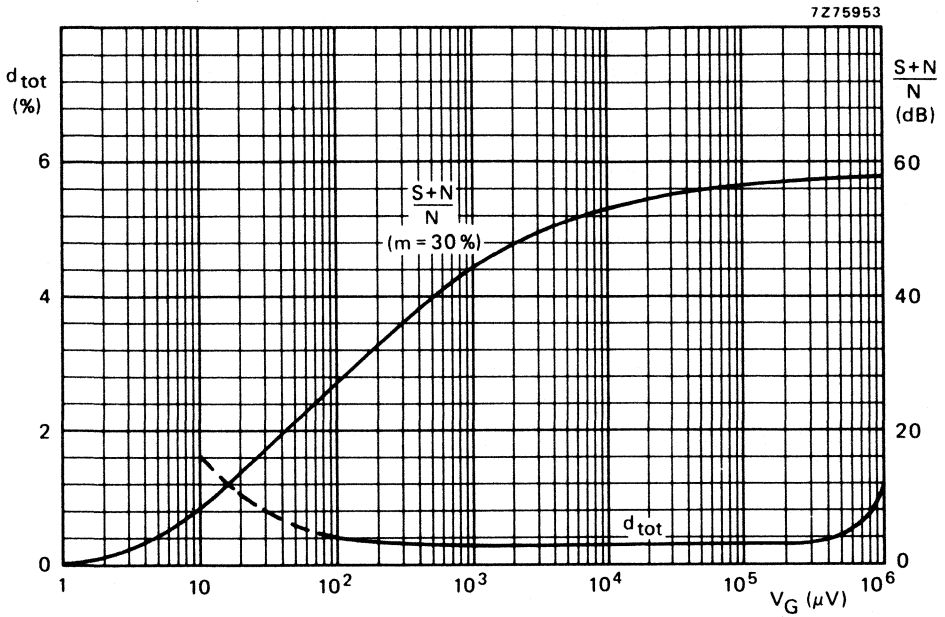


Fig. 9 Total distortion and signal plus noise-to-noise ratio as a function of h.f. generator input voltage; for  $d_{\text{tot}}$  :  $f_m = 0,4$  kHz;  $m = 80\%$ .





## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1074A

# DUAL TANDEM ELECTRONIC POTENTIOMETER CIRCUIT

## GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can perform bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

## Features

- High impedance inputs to both 'ends' of each electronic potentiometer
- Ganged potentiometers track within 0,5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7,5 V with reduced input and output signal levels

## QUICK REFERENCE DATA

Supply voltage (pin 11)	$V_p$	typ.	20 V
Supply current (pin 11)	$I_p$	typ.	22 mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	max.	6 V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	max.	6 V
Total harmonic distortion	THD	typ.	0,05 %
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50 $\mu$ V
Control range	$\Delta\alpha$	typ.	110 dB
Cross-talk attenuation (L/R)	$\alpha_{ct}$	typ.	80 dB
Ripple rejection (100 Hz)	$\alpha_{100}$	typ.	46 dB
Tracking of ganged potentiometers	$\Delta G_v$	typ.	0,5 dB
-----			
Supply voltage range	$V_p$		7,5 to 23 V
Operating ambient temperature range	$T_{amb}$		-30 to +80 °C

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

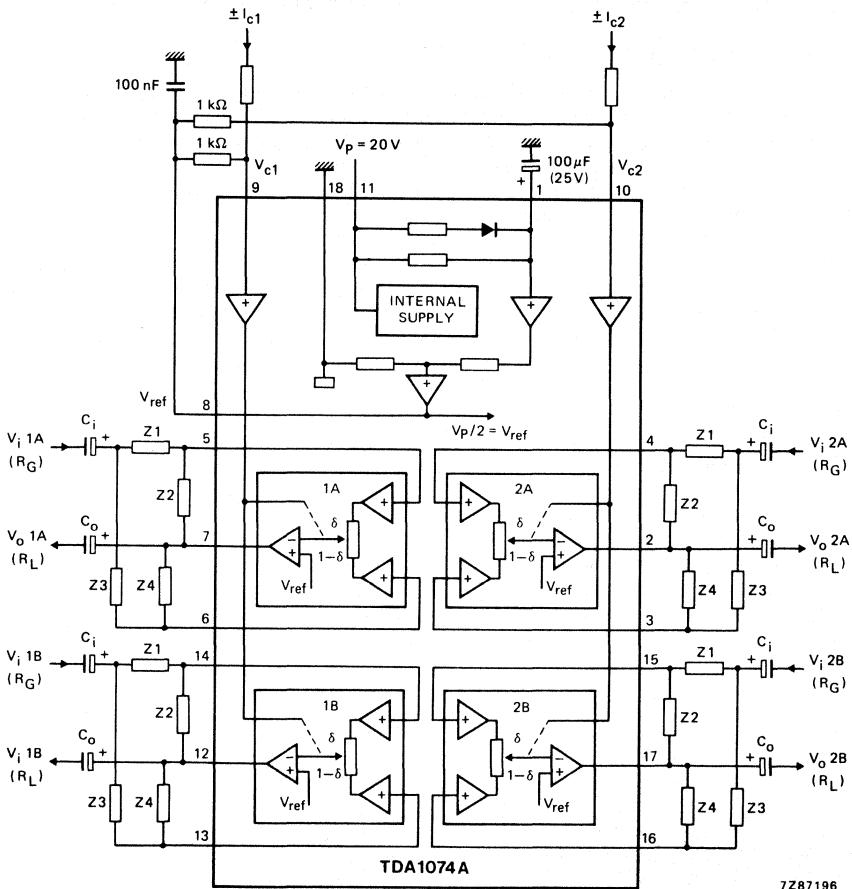


Fig. 1 Block diagram and basic external components;  $I_{c1}$  (at pin 9) and  $I_{c2}$  (at pin 10) are control input currents;  $V_{c1}$  (at pin 9) and  $V_{c2}$  (at pin 10) are control input voltages with respect to  $V_{ref} = V_p/2$  at pin 8;  $Z_1 = Z_2 = Z_3 = Z_4 = 22 \text{ k}\Omega$ ; the input generator resistance  $R_G = 60 \Omega$ ; the output load resistance  $R_L = 4,7 \text{ k}\Omega$ ; the coupling capacitors at the inputs and outputs are  $C_i = 2,2 \mu\text{F}$  and  $C_o = 10 \mu\text{F}$  respectively.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_p$	max.	23 V
Control voltages (pins 9 and 10)	$\pm V_{c1}; \pm V_{c2}$	max.	1 V
Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16	$V_i$		0 to $V_p$ V
Total power dissipation	$P_{tot}$	max.	800 mW
Storage temperature range	$T_{stg}$		-55 to +150 °C
Operating ambient temperature range	$T_{amb}$		-30 to +80 °C

**THERMAL RESISTANCE**

From crystal to ambient	$R_{th\ cr-a}$	=	80 K/W
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**REMARK**

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

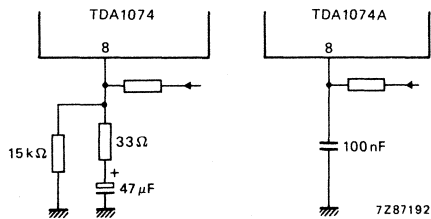


Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.



## APPLICATION INFORMATION

## Treble and bass control circuit

$V_P = 20\text{ V}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ; measured in Fig. 3;  $R_G = 60\ \Omega$ ;  $R_L > 4,7\ \text{k}\Omega$ ;  $C_L < 30\ \text{pF}$ ;  $f = 1\ \text{kHz}$ ; with a linear frequency response ( $V_{C1} = V_{C2} = 0\ \text{V}$ ); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current (without load)	$I_P$	14	22	30	mA
Frequency response (-1 dB) $V_{C1} = V_{C2} = 0\ \text{V}$	$f$	10	—	20 000	Hz
Voltage gain at linear frequency response ( $V_{C1} = V_{C2} = 0\ \text{V}$ )	$G_V^*$	—	0	—	dB
Gain variation at $f = 1\ \text{kHz}$ at maximum bass/treble boost or cut at $\pm V_{C1} = \pm V_{C2} = 120\ \text{mV}$	$\Delta G_V^*$	—	$\pm 1$	—	dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{C2} = 120\ \text{mV}$		—	17,5	—	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{C2} = 120\ \text{mV}$		—	17,5	—	dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{C1} = 120\ \text{mV}$		—	16	—	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{C1} = 120\ \text{mV}$		—	16	—	dB
Total harmonic distortion at $V_{O(\text{rms})} = 300\ \text{mV}$ $f = 1\ \text{kHz}$ (measured selectively)	THD	—	0,002	—	%
$f = 20\ \text{Hz}$ to $20\ \text{kHz}$	THD	—	0,005	—	%
at $V_{O(\text{rms})} = 5\ \text{V}$ $f = 1\ \text{kHz}$	THD	—	0,015	0,1	%
$f = 20\ \text{Hz}$ to $20\ \text{kHz}$	THD	—	0,05	0,1	%
Signal level at THD = 0,7% (input and output)	$V_{i; o(\text{rms})}$	5,5	6,2	—	V
Power bandwidth at reference level $V_{O(\text{rms})} = 5\ \text{V}$ (-3 dB); THD = 0,1%	B	—	40	—	kHz
Output noise voltages signal plus noise (r.m.s. value); $f = 20\ \text{Hz}$ to $20\ \text{kHz}$	$V_{\text{no}(\text{rms})}$	—	75	—	$\mu\text{V}$
noise (peak value); weighted to DIN 45 405; CCITT filter	$V_{\text{no}(\text{m})}$	—	160	230	$\mu\text{V}$

\*  $G_V = V_O/V_i$ .

Treble and bass control circuit

parameter	symbol	min.	typ.	max.	unit
Cross-talk attenuation (stereo) f = 1 kHz	$\alpha_{ct}$	—	86	—	dB
f = 20 Hz to 20 kHz	$\alpha_{ct}$	—	80	—	dB
Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1\text{ mV}$	$-\alpha_{ct}$	—	20	—	dB
Ripple rejection at f = 100 Hz; $V_P(rms) < 200\text{ mV}$	$\alpha_{100}$	—	46	—	dB

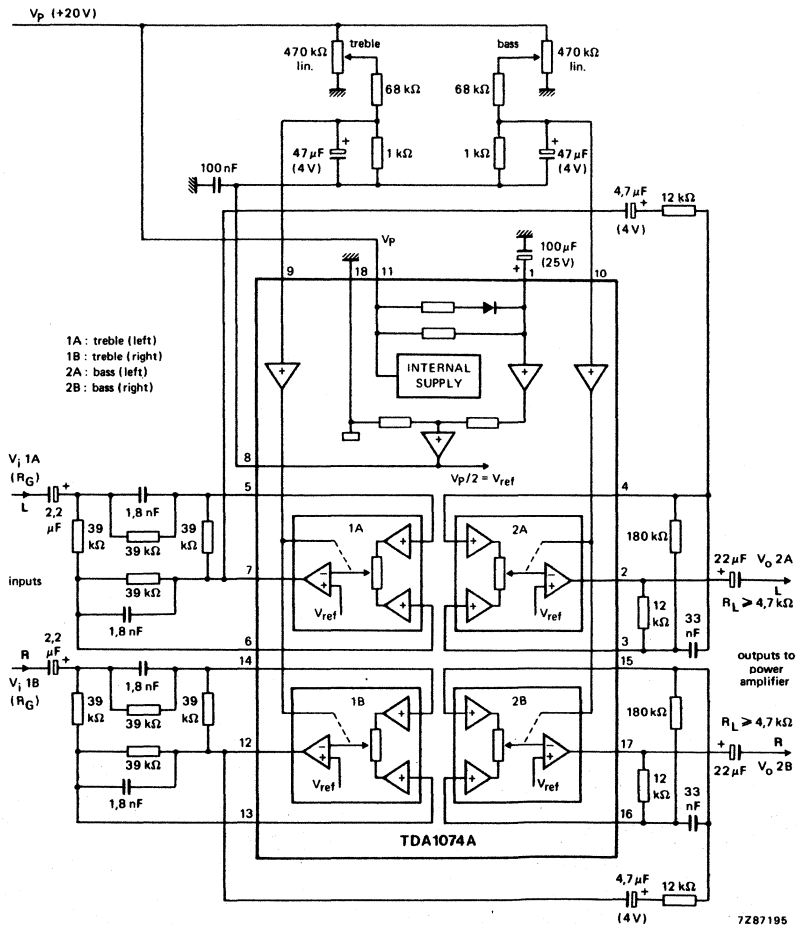


Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

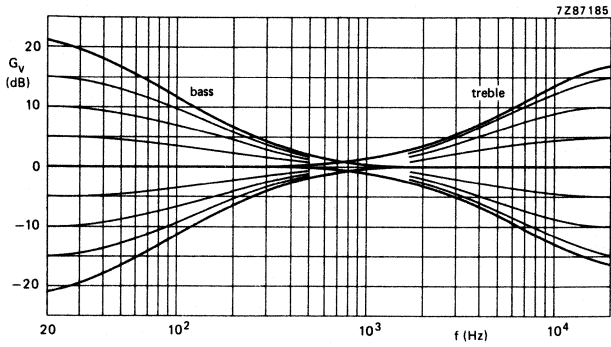


Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

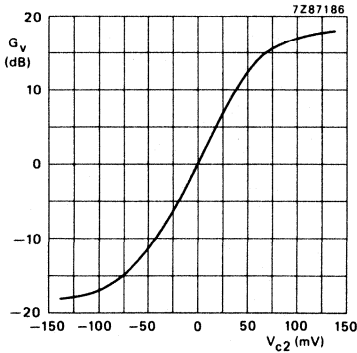


Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage ( $V_{c2}$ );  $f = 40$  Hz.

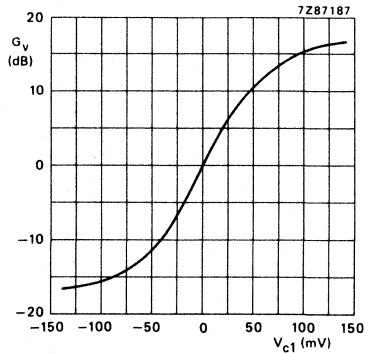
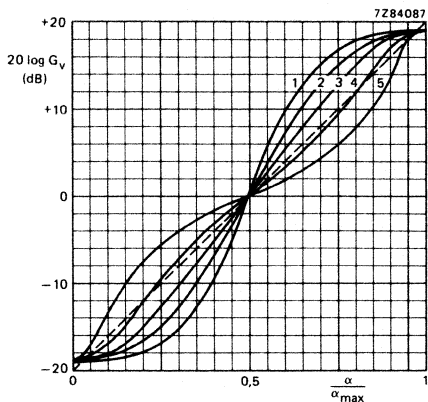


Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage ( $V_{c1}$ );  $f = 16$  kHz.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 7 Voltage gain ( $G_V = V_O/V_i$ ) control curves as a function of the angle of rotation ( $\alpha$ ) of a linear potentiometer (R); for curve numbers see table above;  $f = 40 \text{ Hz to } 16 \text{ kHz}$ .

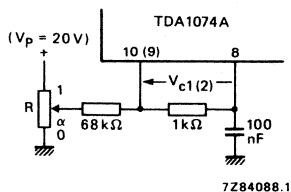


Fig. 8 Circuit diagram for measuring curves in Fig. 7.

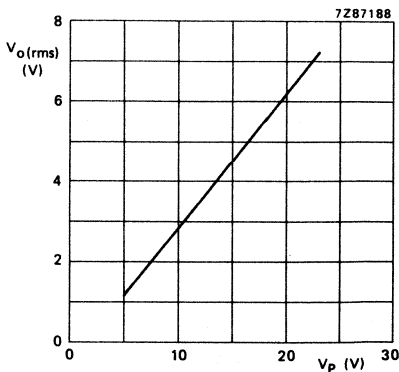


Fig. 9 Output signal level as a function of  $V_p$ ; THD = 0,7%;  $f = 1 \text{ kHz}$ ;  $V_{c1} = V_{c2} = 0 \text{ V}$ .

APPLICATION INFORMATION (continued)

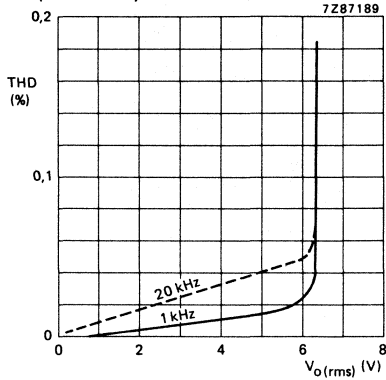


Fig. 10 Total harmonic distortion as a function of the output level;  $V_P = 20\text{ V}$ ;  $R_L = 4,7\text{ k}\Omega$ ;  $V_{C1} = V_{C2} = 0\text{ V}$  (linear,  $G_{V\text{tot}} = 1$ ). —  $f = 1\text{ kHz}$ ; - - -  $f = 20\text{ kHz}$ .

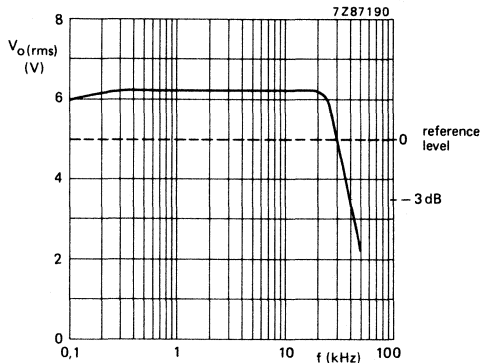


Fig. 11 Power bandwidth at THD = 0,1%; reference level is 5 V (r.m.s.).

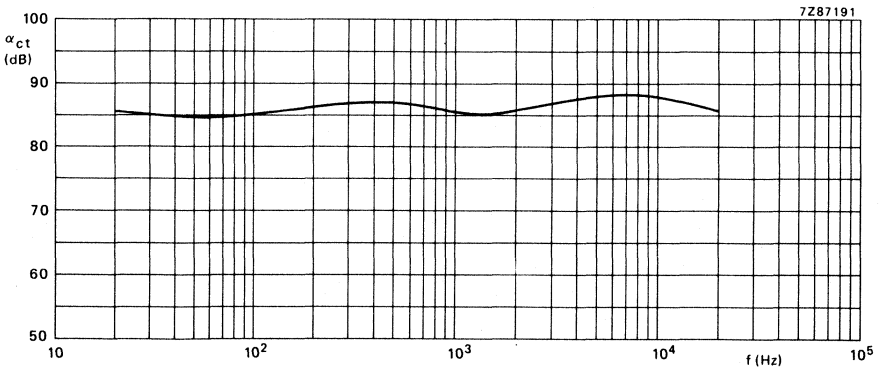
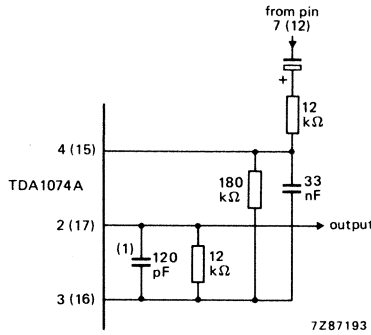


Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting ( $V_{C1} = V_{C2} = 0\text{ V}$ );  $V_i = 5\text{ V}$ ;  $R_G = 60\ \Omega$ ;  $R_L = 4,7\text{ k}\Omega$ .

**Application recommendations**

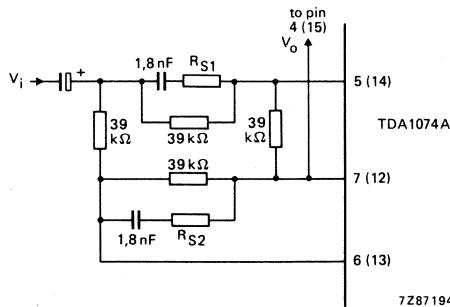
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
  - a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
  - b. Unused control voltage inputs should be connected directly to pin 8 ( $V_{ref}$ ).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8 ( $V_{ref}$ ) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.



(1)  $f_{-3\text{dB}} = 110 \text{ kHz}$  at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.



For  $R_{S1} = R_{S2} = 3,3 \text{ k}\Omega$ ;  $f_{-3\text{dB}} \cong 1 \text{ MHz}$  at linear setting

For  $R_{S1} = R_{S2} = 0 \Omega$ ;  $f_{-3\text{dB}} \cong 100 \text{ kHz}$  at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

DEVELOPMENT SAMPLE DATA







# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# TDA1506

## MOTOR REGULATOR AND FUNCTION CONTROLLER FOR CAR CASSETTE SYSTEMS

The TDA1506 is for car radio/cassette players. It incorporates the following functions:

- a motor speed regulator with a multiplication coefficient of  $k = 20,5$ ,
- an electronic motor stop, controlled by commutator pulses;
- protection circuitry to avoid restarting of the motor after the set is switched to radio reception;
- playback indication;
- tape-end indication with intermittent light;
- fast-wind/rewind circuitry;
- two separately stabilized voltage regulators for the playback amplifier stages;
- a stabilized output voltage for the radio part;
- an automatic switch for switching the preamplifier supply outputs to zero and the radio supply output to a high level at tape-end;
- an output signal for auto-reverse;
- short-circuit protection for all pins to ground at  $T_{amb} = 30\text{ }^{\circ}\text{C}$  maximum and between output and power supply pin;
- load dump protection.

During fast wind (or rewind) the voltage regulator for the second playback preamplifier is switched off. This feature allows application in an A.P.S.S. (Automatic Program Search System) set. At tape-end and at an externally chosen fixed time before motor stop, the automatic replay output gives a d.c. information signal. This signal may, e.g., be used to control the plunger in an automatic-reverse set. Automatic switching, with all switches to ground.

### QUICK REFERENCE DATA

Supply voltage range	$V_p$	10 to 16 V
Operating ambient temperature range		
at $V_p = 14,4\text{ V}$	$T_{amb}$	-20 to +80 $^{\circ}\text{C}$
at $V_p = 16\text{ V}$	$T_{amb}$	-20 to +60 $^{\circ}\text{C}$
<b>Motor regulator</b>		
Regulator supply voltage range	$V_{6-3}$	3,2 to 12 V
Internal reference voltage	$V_{ref} = V_{6-5}$	typ. 1,38 V
Drop-out voltage	$V_{4-3}$	< 1,8 V
Multiplication coefficient ( $\Delta I_4/\Delta I_6$ )	$k$	typ. 20,5
<b>Stabilization radio</b>		
Output voltage	$V_{11-8}$	> 8,5 V
Limited output current	$I_{11\text{ lim}}$	> 45 mA
<b>Stabilization preamplifier I</b>		
Output voltage	$V_{10-8}$	> 7,7 V
Limited output current	$I_{10\text{ lim}}$	> 2 mA
<b>Stabilization preamplifier II</b>		
Output voltage	$V_{9-8}$	> 8,7 V
Limited output current	$I_9\text{ lim}$	> 20 mA
<b>Lamp driver</b>		
Output voltage	$V_{2-8}$	> 13 V
Limited output current	$I_2\text{ lim}$	> 20 mA

PACKAGE OUTLINE 16-lead DIL; plastic power (SOT-38).

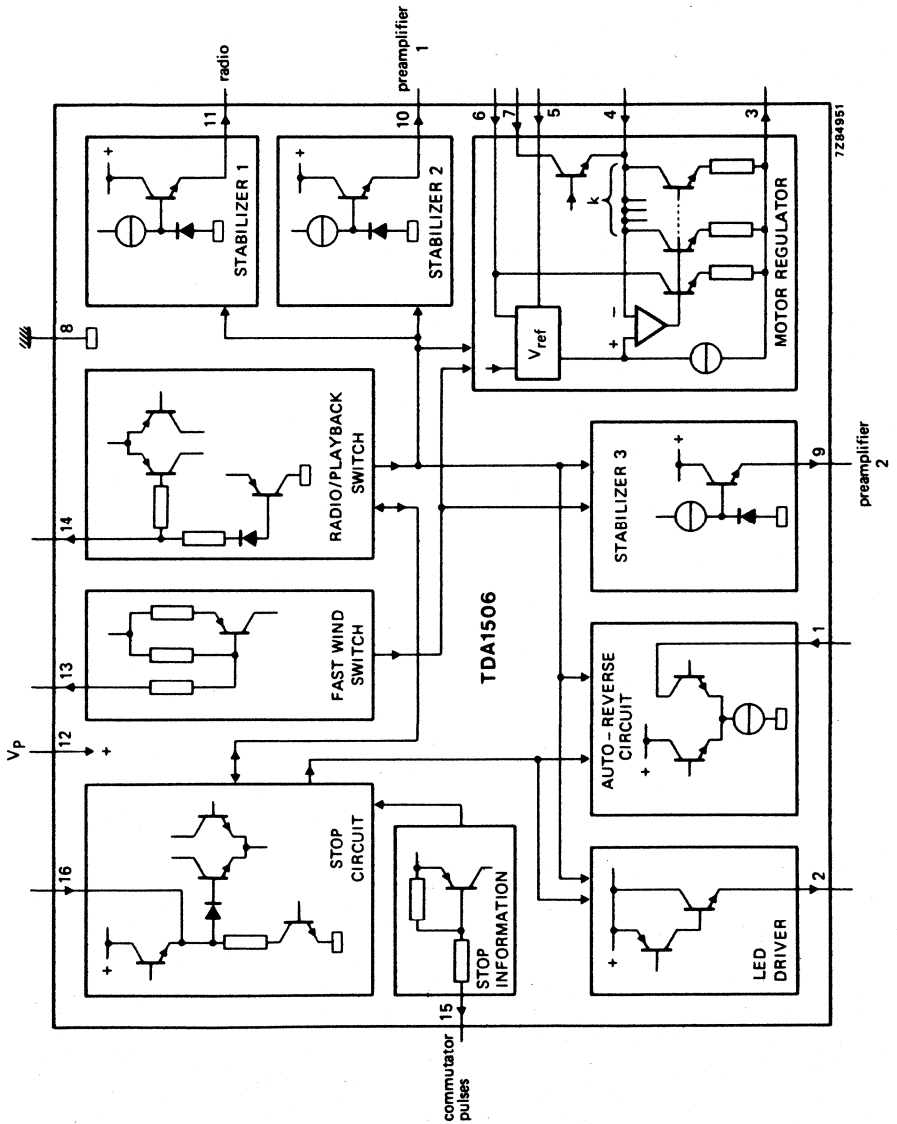


Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p$	max.	24 V
Limited output current	$I_{4 \text{ lim}}$	max.	1 A
Power dissipation	see Fig. 2		
Storage temperature range	$T_{\text{stg}}$	-65 to + 150 °C	
Junction temperature	$T_j$	max.	150 °C

**THERMAL RESISTANCE**

From junction to ambient  $R_{\text{th j-a}} = 55 \text{ K/W}$

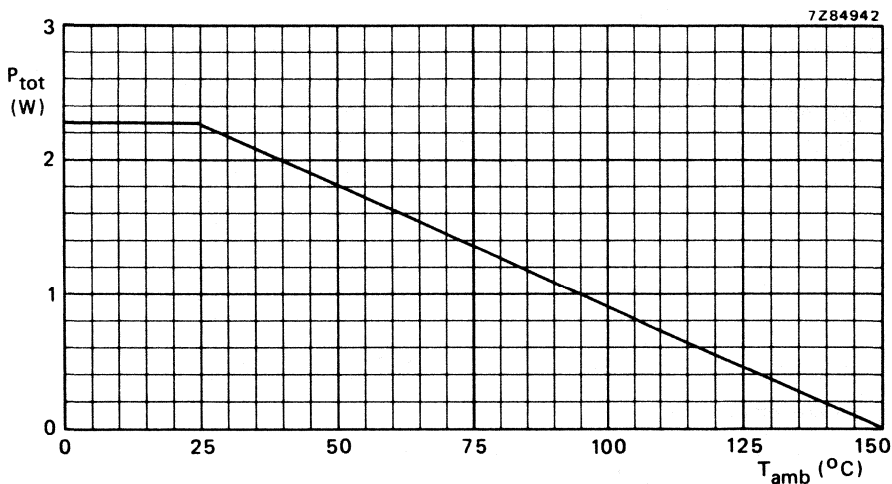


Fig. 2 Power derating curve.

Note to Fig. 2

$$P_{\text{tot}} = \frac{T_j \text{ max} - T_{\text{amb}}}{R_{\text{th j-a}}}$$

$P_{\text{tot}}$  in playback position (see Figure 3):

$$P_{\text{tot}} \approx I_{12} \times V_p + V_{4-3} \left( I_m + \frac{V_{\text{ref}}}{R_2} \right) + (V_{4-3} + V_{\text{ref}}) \left( \frac{I_4}{k} + I_q \right) - I_2 \times V_{2-8} - I_9 \times V_{9-8} - I_{10} \times V_{10-8}$$

$P_{\text{tot}}$  in radio reception is much lower than  $P_{\text{tot}}$  in playback.

DEVELOPMENT SAMPLE DATA



**CHARACTERISTICS**

$V_P = 14,4 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $I_4 = 70 \text{ mA}$ ;  $I_{11} = 45 \text{ mA}$ ;  $I_{10} = 0,3 \text{ mA}$ ;  $I_2 = 18 \text{ mA}$ ;  $I_9 = 2 \text{ mA}$ ; unless otherwise specified; see test circuit Fig. 3.

	symbol	min.	typ.	max.	unit	conditions
<b>General</b>						
Supply voltage	$V_P$	10 *	—	16	V	
Current consumption at playback	$I_{12}$	—	—	38	mA	$I_4 = 0$
at radio	$I_{12}$	—	—	64	mA	
<b>Motor regulator</b>						
Supply voltage	$V_{6-3}$	3,2	—	12	V	
Drop-out voltage	$V_{4-3}$	—	—	1,8	V	$\Delta V_{ref} = \pm 2\%$
Internal reference voltage	$V_{ref} = V_{6-5}$	1,32	1,38	1,44	V	$V_{6-3} = 8,7 \text{ V}$
Quiescent current	$I_q$	—	1,5	2,5	mA	$I_4 = 0$ ; $V_{6-3} = 8,7 \text{ V}$
Limited output current	$I_4 \text{ lim}$	0,5	—	—	A	$V_{6-3} = 8,7 \text{ V}$
Multiplication coefficient	$k = \Delta I_4 / \Delta I_6$	18,5	20,5	22,5		$V_{6-3} = 8,7 \text{ V}$ ; $\Delta I_4 = \pm 10 \text{ mA}$
Line regulation variation						
$V_{ref}$ versus $V_P$	$\frac{\Delta V_{ref}}{\Delta V_P} \times \frac{100\%}{V_{ref}}$	0	0,05	0,09	%/V	$V_P = 3,2 \text{ to } 12 \text{ V}$
$k$ versus $V_P$	$\frac{\Delta k}{\Delta V_P} \times \frac{100\%}{k}$	0	0,3	0,6	%/V	$V_P = 3,2 \text{ to } 12 \text{ V}$ ; $\Delta I_4 = \pm 10 \text{ mA}$
$I_q$ versus $V_P$	$\frac{\Delta I_q}{\Delta V_P} \times \frac{100\%}{I_q}$	—	1,25	—	%/V	$V_P = 3,2 \text{ to } 12 \text{ V}$ ; $I_4 = 0$
Load regulation variation						
$V_{ref}$ versus $I_4$	$\frac{\Delta V_{ref}}{\Delta I_4} \times \frac{100\%}{V_{ref}}$	-0,037	-0,018	—	%/mA	$I_4 = 20 \text{ to } 150 \text{ mA}$
$k$ versus $I_4$	$\frac{\Delta k}{\Delta I_4} \times \frac{100\%}{k}$	-0,02	0	+0,02	%/mA	$I_4 = 20 \text{ to } 150 \text{ mA}$ ; $\Delta I_4 = \pm 10 \text{ mA}$
<b>Temperature coefficient variation</b>						
$V_{ref}$ versus $T_{amb}$	$\frac{\Delta V_{ref}}{\Delta T_{amb}} \times \frac{100\%}{V_{ref}}$	0	0,025	0,045	%/K	$T_{amb} = -20 \text{ to } +80 \text{ }^\circ\text{C}$ ; $V_{6-3} = 8,7 \text{ V}$
$k$ versus $T_{amb}$	$\frac{\Delta k}{\Delta T_{amb}} \times \frac{100\%}{k}$	-0,016	0,008	0,032	%/K	$T_{amb} = -20 \text{ to } +80 \text{ }^\circ\text{C}$ ; $V_{6-3} = 8,7$ ; $\Delta I_4 = \pm 10 \text{ mA}$
$I_q$ versus $T_{amb}$	$\frac{\Delta I_q}{\Delta T_{amb}} \times \frac{100\%}{I_q}$	—	0,13	—	%/K	$T_{amb} = -20 \text{ to } +80 \text{ }^\circ\text{C}$ ; $V_{6-3} = 8,7 \text{ V}$ ; $I_4 = 0$
Saturation voltage fast winding	$V_{7-4 \text{ sat}}$	—	0,18	—	V	$I_7 = 10 \text{ mA (max. } 50 \text{ mA)}$
Input current (pin 5)	$I_5$	—	19	—	$\mu\text{A}$	$V_{6-3} = 8,7 \text{ V}$

\* For starting conditions: min. 6 V.

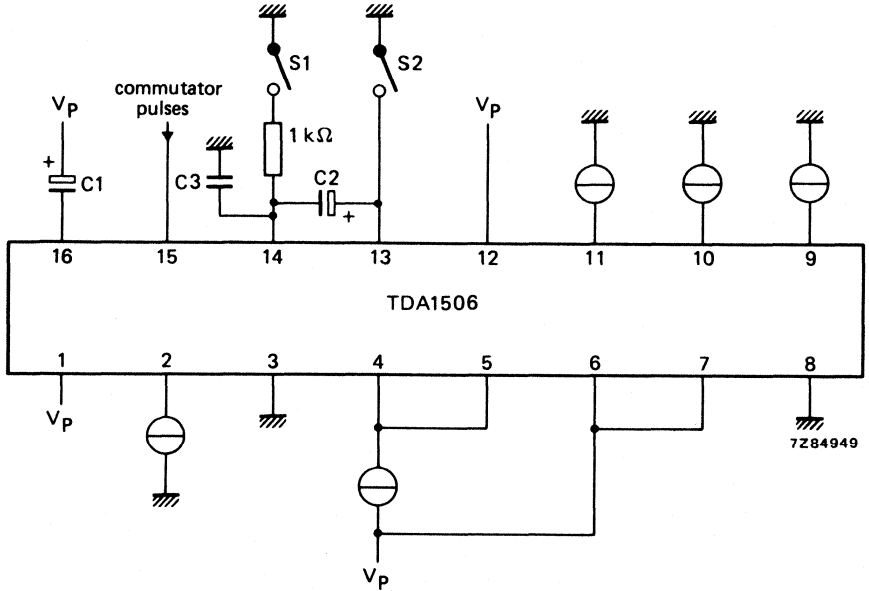
DEVELOPMENT SAMPLE DATA

	symbol	min.	typ.	max.	unit	conditions
<b>Automatic motor stop</b>						
Output current (pin 15)	$I_{15}$	0,4	—	0,9	mA	
Time constant	$t_{st}$	—	700	—	ms	$C1 = 47 \mu F \pm 1\%$ ; Fig. 4
Switching level	$V_{16-8}$	—	9	—	V	
<b>Stabilization radio</b>						
Output voltage	$V_{11-8}$	8,5	8,9	9,3	V	
Limited output current	$I_{11 \text{ lim}}$	45	—	—	mA	
Variation of $V_{11-8}$	$\Delta V_{11-8}$	—	—	200	mV	$V_p = 10,5$ to 16 V
		—	100	—	mV/V	$V_p = 10$ to 10,5 V
Leakage current	$I_{11}$	—	—	0,5	$\mu A$	$R_{11-8} = 100 \text{ k}\Omega$
	$I_{11}$	—	—	4	$\mu A$	$R_{11-8} = 100 \text{ k}\Omega$ $T_{amb} = 80 \text{ }^\circ\text{C}$
Temperature coefficient	$\Delta V_{11-8}/\Delta T_{amb}$	-2	0	+2	mV/K	$T_{amb} = -20$ to $+80 \text{ }^\circ\text{C}$
<b>Stabilization preamp. I</b>						
Output voltage	$V_{10-8}$	7,7	8,1	—	V	
Limited output current	$I_{10 \text{ lim}}$	2	—	—	mA	
Variation $V_{10-8}$ versus $V_p$	$\Delta V_{10-8}/\Delta V_p$	—	—	12	mV/V	$V_p = 10,5$ to 16 V
	$\Delta V_{10-8}/\Delta V_p$	—	5	—	mV/V	$V_p = 10$ to 10,5 V
<b>Stabilization preamp. II</b>						
Output voltage	$V_{9-8}$	8,5	9,1	—	V	
Output voltage	$V_{9-8}$	—	0	0,5	V	fast rewind
Limited output current	$I_{9 \text{ lim}}$	20	—	—	mA	
Variation $V_{9-8}$ versus $V_p$	$\Delta V_{9-8}/\Delta V_p$	—	—	12	mV/V	$V_p = 10,5$ to 16 V
	$\Delta V_{9-8}/\Delta V_p$	—	10	—	mV/V	$V_p = 10$ to 10,5 V
<b>Lamp driver</b>						
Output voltage	$V_{2-8}$	13	13,4	—	V	
Limited output current	$I_{2 \text{ lim}}$	20	—	—	mA	
Blinking time	$t_b$	—	0,5	—	s	$C1 = 47 \mu F$ ; Fig. 4
Rejection voltage supply	$\Delta V_p$	—	0,3	—	V	
<b>Automatic replay output</b>						
Output current; playback	$I_1$	—	—	10	$\mu A$	$V_{1-8} = V_p$
Output current; radio	$I_1$	300	500	—	$\mu A$	$V_{1-8} \geq 5 \text{ V}$
Delay time	$t_d$	—	380	—	ms	$C1 = 47 \mu F$ ; Fig. 4



CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit	conditions
<b>Radio playback switch</b>						
Switching levels to playback	$V_{14-8}$	—	—	2	V	} $V_p = 10$ to $16$ V } $T_{amb} = -20$ to $+80$ °C
to radio	$V_{14-8}$	3,5	—	—	V	
Input impedance	$ Z_{14-8} $	—	20	—	k $\Omega$	
Output current	$I_{14}$	—	200	—	$\mu$ A	$V_{14-8} = 0$
<b>Fast wind switch</b>						
Switching levels normal to fast	$V_{13-8}$	—	—	2	V	} $V_p = 10$ to $16$ V } $T_{amb} = -20$ to $+80$ °C
fast to normal	$V_{13-8}$	6	—	—	V	
Output voltage; playback	$V_{13-8}$	—	6,8	—	V	
Output current; fast wind	$I_{13}$	—	500	—	$\mu$ A	$V_{13-8} = 0$
Output impedance	$ Z_{13-8} $	—	13	—	k $\Omega$	



S1 closed: playback  
 S1 open: radio reception  
 S2 closed: fast speed  
 S2 open: normal speed

C2 is only used with sets on which a fast rewind key is available ( $C2 = 2,2 \mu F$ ).  
 C1 is  $200 \mu F$  maximum (typ.  $47 \mu F$ ).  
 C3 =  $100$  nF.

Fig. 3 Test circuit.

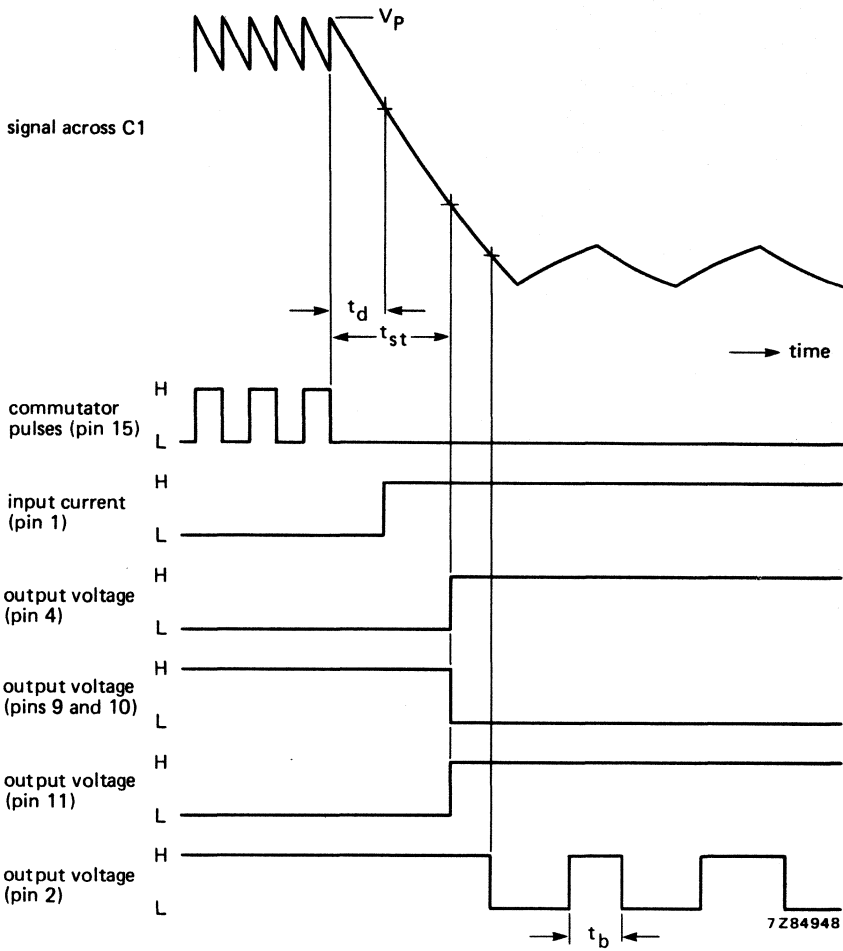


Fig. 4 Waveforms showing signal levels and time constants.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

APPLICATION INFORMATION

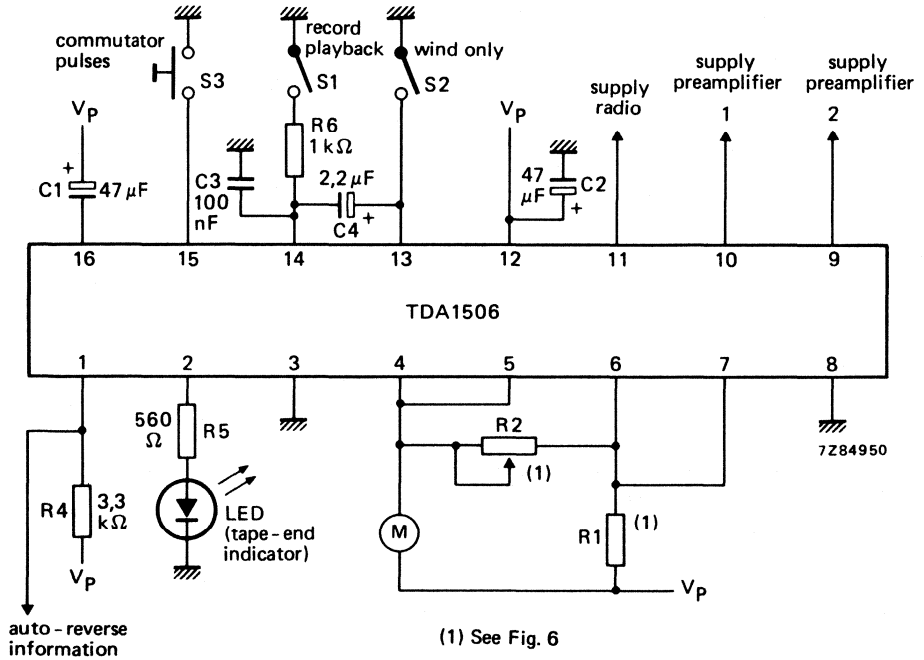
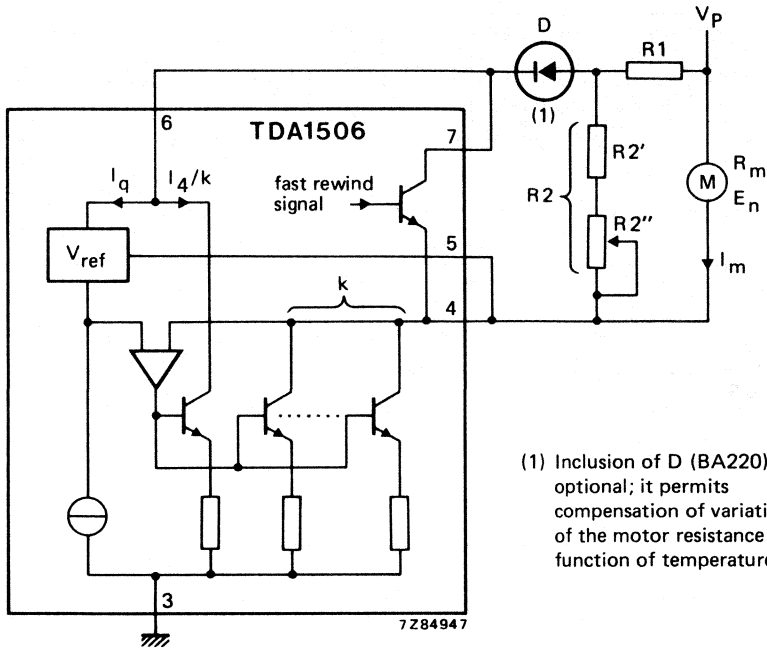


Fig. 5 Typical simplified application circuit diagram.





(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 6 Example of using the TDA1506 (only the motor regulation part is shown) in a d.c. motor speed regulation circuit.

Notes to Fig. 6

$$R_2 = R_2' + R_2''$$

$$E_n = n \times C \times \phi$$

$$I_m = T \times \frac{2\pi}{60} \times \frac{1}{C \cdot \phi}$$

where: n = speed in revolutions per minute

C = motor constant

phi = magnetic flux

E\_n = electromotive force

T = motor torque

R\_m = motor resistance

E\_n can be expressed (excluding diode D) as:

$$E_n = I_m \left( \frac{R_1}{k} - R_m \right) + V_{ref} \left\{ 1 + \frac{R_1}{R_2} \left( 1 + \frac{1}{k} \right) \right\} + R_1 \times I_q$$

For optimal regulation (dn/dT = 0),  $\left( \frac{R_1}{k} - R_m \right)$  should be zero.

However, if  $R_1 = k \times R_m$ , the regulator will be oscillating, so for stability always  $R_1 < k \times R_m$ .

R\_2 is determined by:

$$R_2 = \frac{V_{ref} \times R_1 \times \left( 1 + \frac{1}{k} \right)}{E_n - (R_1 \times I_q) - V_{ref} - I_m \left( \frac{R_1}{k} - R_m \right)}$$

Example:

$$E_n = E_{2400} = 5,24 \text{ V} (\pm 12,2\%)$$

$$R_m = 25,6 \Omega (\pm 10\%)$$

$$n = 2400 \text{ rev/min}$$

$$T = 1,3 \text{ mNm}$$

$$R_1 = 430 \Omega$$

$$R_2' = 110 \Omega$$

$$R_2'' = 220 \Omega$$

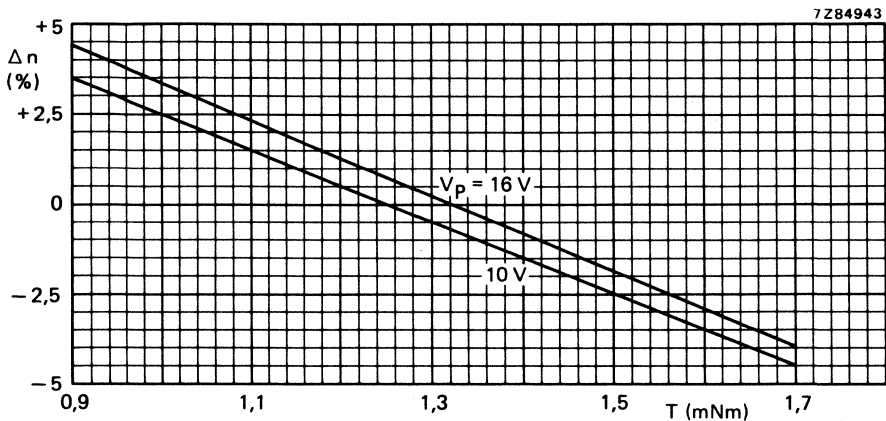


Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

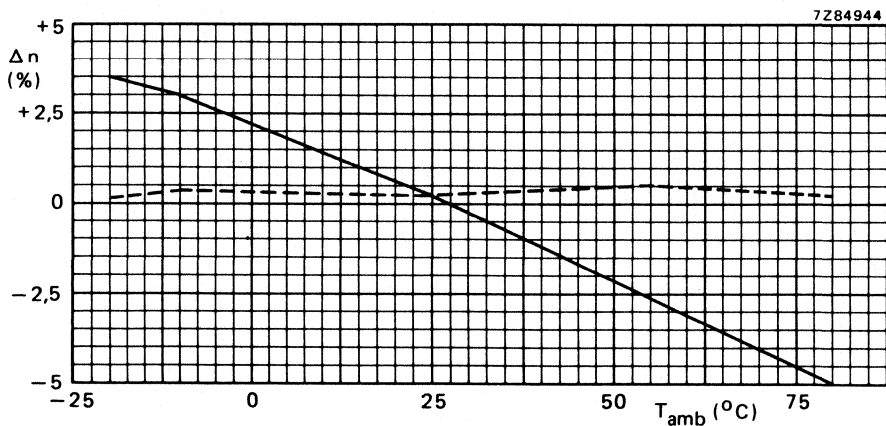


Fig. 8 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at  $T = 1,3\text{ mNm}$  nominal and  $V_p = 16\text{ V}$ .

—————: with diode D (see Fig. 6).

- - - - -: without diode.

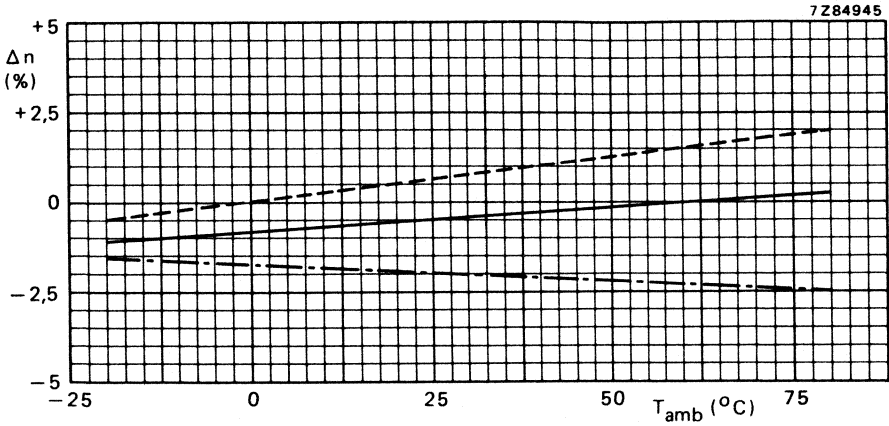


Fig. 9a V<sub>p</sub> = 10 V.

DEVELOPMENT SAMPLE DATA

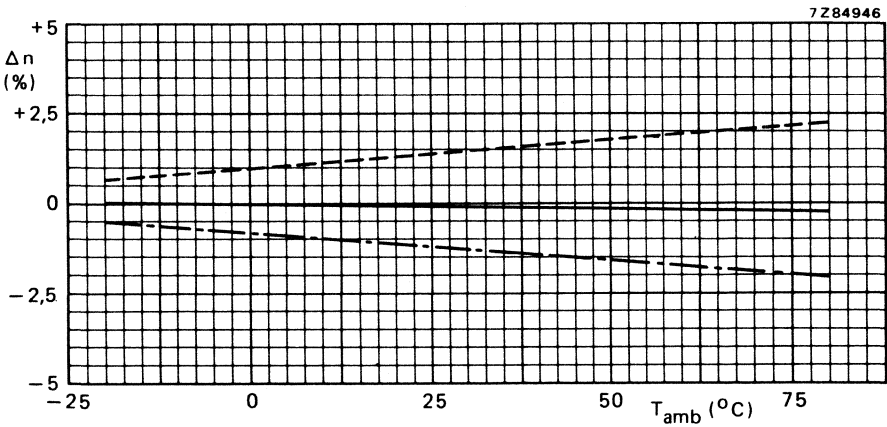


Fig. 9b V<sub>p</sub> = 16 V.

Fig. 9 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (see Fig. 6).

- : T = 1,17 mNm
- : T = 1,30 mNm
- · - · -: T = 1,43 mNm



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1508

# AUTO—REVERSE CAR RADIO CASSETTE—DECK STEERING CIRCUIT

## GENERAL DESCRIPTION

The TDA1508 is a monolithic integrated circuit generating the steering signals needed for an auto-reverse car radio cassette-deck.

The TDA1508 incorporates the following functions:

- RC-oscillator generating the 250 kHz system clock
- Logic block ( $I^2L$ )
- Power-on-reset circuit
- Input interface circuits
- Output interface circuits
- Two output voltage stabilizers
- 4 ms motor-pause-pulse
- Fast wind pulse
- Muting pulse
- 1024 ms clock pulse for cassette rotation control.

## QUICK REFERENCE DATA

Supply voltage range (pin 7)	$V_p$	10 to 18	V
Supply voltage range, standby (pin 12)	$V_{SB}$	3,5 to 18	V
Operating ambient temperature range	$T_{amb}$	-30 to +85	°C
-----			
Supply current (pin 7)	$I_p$	max.	15 mA
Supply current standby (pin 12)	$I_{SB}$	typ.	1,5 mA

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102).

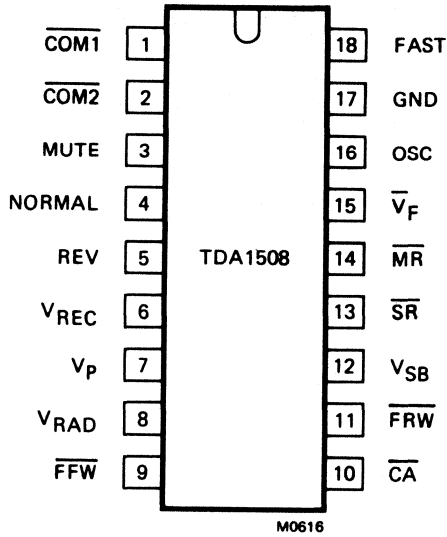
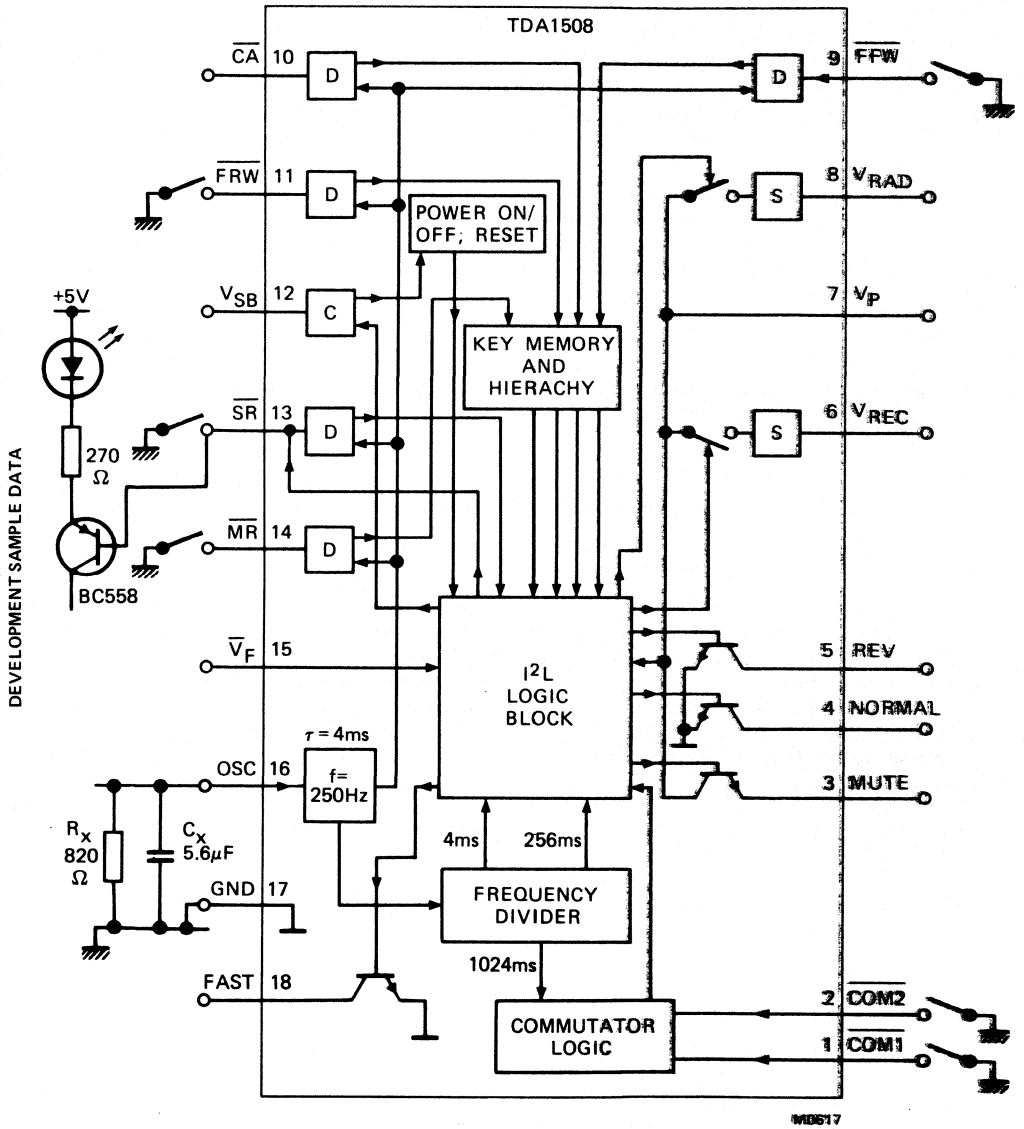


Fig.1 Pinning diagram

**PINNING**

- |                             |                          |                               |                              |
|-----------------------------|--------------------------|-------------------------------|------------------------------|
| 1. $\overline{\text{COM1}}$ | commutator logic input 1 | 10. $\overline{\text{CA}}$    | cassette contact input       |
| 2. $\overline{\text{COM2}}$ | commutator logic input 2 | 11. $\overline{\text{FRW}}$   | fast rewind input            |
| 3. MUTE                     | audio mute output        | 12. $V_{\text{SB}}$           | standby supply control input |
| 4. NORMAL                   | motor control output     | 13. $\overline{\text{SR}}$    | tape-end input               |
| 5. REV                      | motor control output     | 14. $\overline{\text{MR}}$    | manual reverse input         |
| 6. $V_{\text{REC}}$         | recording power supply   | 15. $\overline{V_{\text{F}}}$ | radio mode input             |
| 7. $V_{\text{p}}$           | linear part power supply | 16. OSC                       | oscillator RC input          |
| 8. $V_{\text{RAD}}$         | radio power supply       | 17. GND                       | ground                       |
| 9. $\overline{\text{FFW}}$  | fast forward wind input  | 18. FAST                      | motor control output         |



## FUNCTIONAL DESCRIPTION

### General

The circuit incorporates an I<sup>2</sup>L logic block which generates any specific control signal and delay time needed in the auto-reverse car radio cassette-deck. A power-on reset element resets the I<sup>2</sup>L logic block when the standby supply V<sub>SB</sub> is connected to the logic block. This standby voltage maintains the state of the logic part of the IC after the supply voltage for the linear part of the IC, V<sub>p</sub>, has been switched off. The circuit uses an external RC network with an on-chip oscillator to generate a 250 Hz system clock.

Input interface circuits convert the  $\overline{V_F}$ ,  $\overline{COM1}$ ,  $\overline{COM2}$ ,  $\overline{MR}$ ,  $\overline{FRW}$ ,  $\overline{FFW}$ ,  $\overline{SR}$  and  $\overline{CA}$  information to I<sup>2</sup>L logic levels; output interface circuits activate the open-collector outputs REV, NORMAL, FAST and  $\overline{SR}$ . The n-p-n transistor at the MUTE output is switched by logic levels from the I<sup>2</sup>L logic block. Two output voltage stabilizers, supplied from V<sub>p</sub> provide supply voltages for the radio part, V<sub>RAD</sub>, and for the cassette deck pre-amplifiers, V<sub>REC</sub>, respectively.

### Function

Each commutation applied to the cassette deck motor is preceded by a 4 ms motor-pause pulse. After any change in the direction of motor rotation a fast wind (FW) pulse (1020 ms) is generated. During the period of the FW pulse the motor supply voltage is increased, the motor speed also increasing at the same time.

### Input signals

Signal 'bounce' is suppressed by means of a 32 ms control pulse.

**$\overline{V_F}$  (pin 15)** A LOW at this input causes the deck to enter the radio mode, where it provides traffic information. The cassette motor stops in the radio mode.

**$\overline{SR}$  (pin 13)** A LOW at the  $\overline{SR}$  input sets a latch and activates a 2-bit counter. Pulses from  $\overline{COM1}$  and  $\overline{COM2}$  enable the end of tapeside A to be recognized. When the end of tapeside A has been recognized the motor will reverse and tapeside B will be played. When both tapesides have been played the deck will revert to the radio mode. A HIGH at the  $\overline{SR}$  input initiates the endless auto-reverse playback mode. The  $\overline{SR}$  input can be used to indicate the operating mode (single or auto-reverse). If an external transistor is used in conjunction with a suitable LED indicator, the LED will light up when the  $\overline{SR}$  input goes LOW in the single playback mode.

**$\overline{MR}$  (pin 14) manual reverse.** A LOW at the  $\overline{MR}$  input reverses the direction of the cassette.

**$\overline{FRW}$  (pin 11) fast rewind.** A LOW at the input causes the cassette to go into the fast rewind mode. When the  $\overline{FRW}$  key has been released (HIGH at pin 11) the cassette player continues in the playback mode.

**$\overline{FFW}$  (pin 9) fast forward wind.** A LOW at this pin starts the fast forward wind; releasing the  $\overline{FFW}$  key causes the cassette to re-enter the playback mode.

**$\overline{CA}$  (pin 10) cassette contact.** Inserting a cassette into the player gives a LOW at this input. The player will always start in the playback mode playing the sound track of the cassette which corresponds to the upper label of the cassette.

**$\overline{COM1}$  (pin 1) and  $\overline{COM2}$  (pin 2).** The impulses at these inputs arise from the rotation of the cassette turntables. In conjunction with signals at  $\overline{SR}$  the end of a tapeside can be recognized. The minimum rotational speed of the cassette turntables is also controlled using impulses at these pins. During a period of 1024 ms a minimum count of pulses has to be detected for continuous operation.

**V<sub>p</sub> (pin 7) supply voltage for linear part.** When V<sub>p</sub> is LOW the output functions (V<sub>REC</sub>, V<sub>RAD</sub>, NORMAL, REV, FAST,  $\overline{SR}$ -indication) are inactive. The switching levels for V<sub>p</sub> are shown in Fig. 5. The MUTE transistor remains active independent of the value of V<sub>p</sub>, when the audio mute is required.



**Output signals**

**FAST (pin 18), NORMAL (pin 4), REV (pin 5).** These open-collector outputs steer the motor control of the cassette deck.

**MUTE (pin 3).** The audio output of the cassette is muted in the radio mode and during any change in motor rotation (reverse, fast forward wind, etc). The n-p-n transistor (Fig.2) is switched to  $V_P$  when muting is required. The audio frequency is muted up to 128 ms after the change of mode or motor rotation.

**$V_{REC}$  (pin 6),  $V_{RAD}$  (pin 8).** These stabilized supply voltages are derived from  $V_P$  and provide power for the recording and radio part of the cassette system respectively. When  $V_{RAD}$  is active  $V_{REC}$  is switched off and when  $V_{REC}$  is active  $V_{RAD}$  is switched off.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage linear (pin 7)	$V_P = V_{7-17}$	max.	24	V
Supply voltage standby (pin 12)	$V_{SB} = V_{12-17}$	max.	24	V
All inputs (pins 1,2,9,10,11,13,14 and 15)	$V_{1,2,9,10,11,13,14,15-17}$	max.	24	V
All inputs (pins 3,4,5,6,8,13 and 18)	$V_{3,4,5,6,8,13,18-17}$	max.	24	V
Storage temperature range	$T_{stg}$		-55 to +150	°C
Operating ambient temperature range	$T_{amb}$		-30 to +85	°C



**CHARACTERISTICS**

Supply voltage  $V_P = 14\text{ V}$ ;  $V_{SB} = 18\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$

parameter	symbol	min.	typ.	max.	unit
<b>Linear supply (pin 7)</b>					
Supply voltage linear	$V_P$	10	14	18	V
Supply current linear for $I(V_{RAD})$ and $I(V_{REC}) = 0$	$I_P$	—	—	15	mA
<b>Supply standby (pin 12)</b>					
Supply voltage standby	$V_{SB}$	3,5	—	18	V
Supply current standby	$I_{SB}$	—	1,5	2,5	mA
Power-on-reset			see Fig.3		
Power-off-reset			see Fig.4		
Time constant of RC-combination at $V_{SB}$ for power-on-reset	$\tau$	300	—	—	$\mu\text{s}$
<b>Oscillator</b>					
Oscillator frequency ( $R_X = 820\text{ k}\Omega$ ; $C_X = 5,6\text{ nF}$ )	$f_{osc}$	—	250	—	Hz
Oscillator frequency drift over temperature and supply voltage range	$\Delta f_{osc}/f_{osc}$	-20	—	+20	%
External components	$R_X$	680	820	—	$\text{k}\Omega$
	$C_X$	—	5,6	22	nF
Oscillator a.c. voltage (peak-to-peak value)	$V_{osc(p-p)}$	—	—	1,0	V
<b>Inputs</b>					
$\overline{\text{COM1}}$ , $\overline{\text{FFW}}$ , $\overline{\text{FRW}}$ , $\overline{\text{MR}}$ $\overline{\text{COM2}}$ , $\overline{V_F}$ and $\overline{\text{SR}}$ $\overline{\text{CA}}$					
HIGH (inactive)	$V_{IH}$	2,5	—	$V_P$	V
(for $V_{IH} < V_P - 1.5\text{ V}$ )	$-I_{IH}$	50	100	200	$\mu\text{A}$
LOW (active)	$V_{IL}$	—	—	0,6	V
	$-I_{IL}$	50	100	200	$\mu\text{A}$

parameter	symbol	min.	typ.	max.	unit
<b>Outputs</b>					
NORMAL, REV (open collector)					
Output active saturation voltage ( $I_{sat} < 7 \text{ mA}$ )	$V_{4-17sat}$	—	—	0,3	V
	$V_{5-17sat}$	—	—	0,3	V
FAST					
Output active saturation voltage ( $I_{sat} < 25 \text{ mA}$ )	$V_{18-17sat}$	—	—	0,3	V
MUTE					
Output voltage (n-p-n transistor switched to $V_p$ )	$V_{3-17}$	—	$V_p-2$	—	V
Output current external resistor	$-I_3$	5	—	—	mA
MUTE					
Output inactive voltage	$V_{3-17}$	0	—	—	V
Output inactive current	$-I_3$	—	0	10	$\mu\text{A}$
SR as output stage (open collector)					
Saturation voltage at $I_{sat} = 1 \text{ mA}$	$V_{13-17sat}$	—	—	0,4	V
Inactive current	$-I_{13}$	—	—	10	$\mu\text{A}$
<b>Stabilized output voltages</b>					
$V_{RAD}$ voltage	$V_{6-17}$	8,1	8,5	8,9	V
$V_{REC}$ voltage	$V_{8-17}$	8,1	8,5	8,9	V
Output current (foldback)	$I_6$	45	—	—	mA
	$I_8$	45	—	—	mA
Ripple rejection, $f = 100 \text{ Hz}$ $V_p = 10 \text{ to } 18 \text{ V}$	$\frac{V_{6-17}}{V_{7-17}}$	—	—	20	mV/V
	$\frac{V_{8-17}}{V_{7-17}}$	—	—	20	mV/V
Temperature drift	$\frac{V_{6-17}}{T_{amb}}$	-2	—	+2	mV/K
	$\frac{V_{8-17}}{T_{amb}}$	-2	—	+2	mV/K
Input resistance ( $I = 50 \text{ mA}$ )	$R_i$	—	1	—	$\Omega$
Stabilizer inactive currents	$-I_{RAD}$	100	—	—	$\mu\text{A}$
	$-I_{REC}$	100	—	—	$\mu\text{A}$

DEVELOPMENT DRAWING



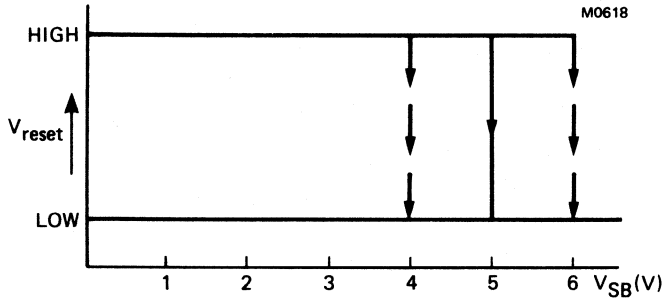


Fig.3 Power-on-reset.

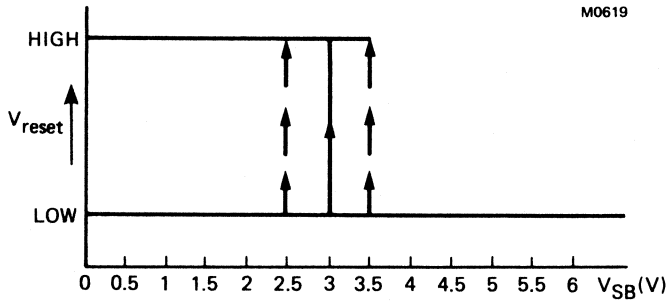


Fig.4 Power-off-reset.

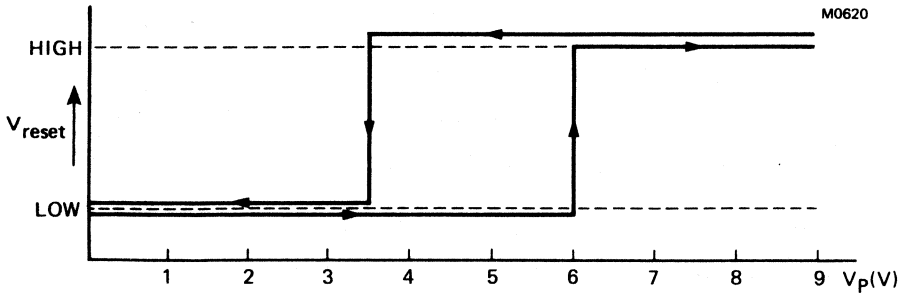


Fig.5 Switching levels for supply voltage monitoring.

## 24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1510 is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to  $1,6 \Omega$ ). At a supply voltage  $V_p = 14,4 \text{ V}$ , an output power of  $24 \text{ W}$  can be delivered into a  $4 \Omega$  BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers  $2 \times 12 \text{ W}$  into  $2 \Omega$  or  $2 \times 7 \text{ W}$  into  $4 \Omega$ .

Special features are:

- flexibility in use — stereo as well as mono BTL
- high output power
- low offset voltage at the output (important for BTL)
- large useable gain variation
- very good ripple rejection
- load dump protection
- a.c. short-circuit safe to ground
- thermal protection
- internal limited bandwidth for high frequencies
- low stand-by current possibility, to simplify required switches
- low number and small sized external components
- high reliability

### QUICK REFERENCE DATA

Supply voltage range (operating)	$V_p$		6 to 18 V
Supply voltage (non-operating)	$V_p$	max.	28 V
Supply voltage (non-operating; load dump protection)	$V_p$	max.	45 V
Repetitive peak output current	$I_{ORM}$	max.	4 A
Total quiescent current	$I_{tot}$	typ.	75 mA
Stand-by current	$I_{sb}$	<	2 mA
Switch-on current	$I_{so}$	typ.	0,35 mA
Input impedance	$ Z_i $	>	1 M $\Omega$
Storage temperature range	$T_{stg}$		-55 to + 150 °C
Crystal temperature	$T_c$	max.	150 °C
<b>Bridge tied load application (BTL)</b>	$V_p$	=	14,4   13,2 V
Output power at $R_L = 4 \Omega$ (with bootstrap)			
$d_{tot} = 0,5\%$	$P_o$	typ.	18   15 W
$d_{tot} = 10\%$	$P_o$	typ.	24   20 W
Supply voltage ripple rejection; $R_S = 0$ ; $f = 1 \text{ kHz}$	RR	typ.	50   50 dB
D.C. output offset voltage between the outputs	$ \Delta V_{5,g} $	<	50   50 mV
<b>Stereo application</b>			
Output power at $d_{tot} = 10\%$ (with bootstrap)			
$R_L = 4 \Omega$	$P_o$	typ.	7   6 W
$R_L = 2 \Omega$	$P_o$	typ.	12   10 W
Output power at $d_{tot} = 0,5\%$ (with bootstrap)			
$R_L = 4 \Omega$	$P_o$	typ.	5,5   4,5 W
$R_L = 2 \Omega$	$P_o$	typ.	9,0   7,5 W
Channel separation	$\alpha$	>	40   40 dB
Noise output voltage; $R_S = 10 \text{ k}\Omega$ ; according to IEC curve-A	$V_n$	typ.	0,2   0,2 mV

### PACKAGE OUTLINE

13-lead SIL; plastic power (SOT-141B).

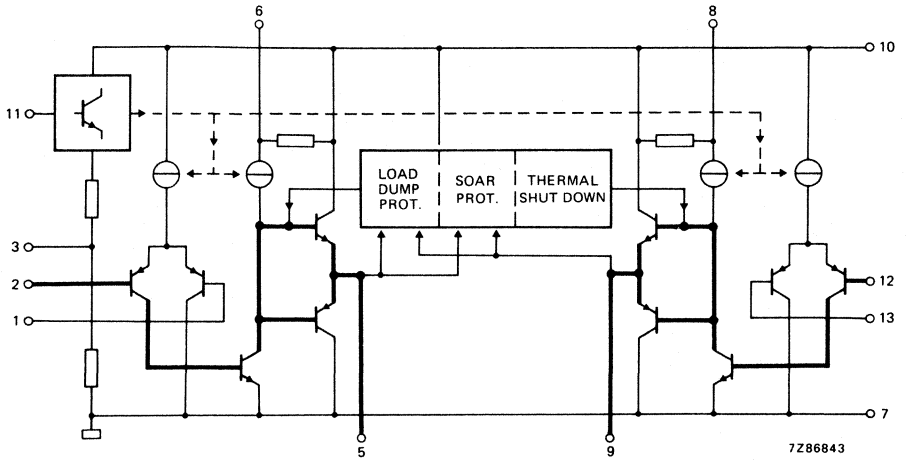


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.  
Pin 4 is internally connected.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V <sub>p</sub>	max.	18 V
Supply voltage; non-operating	V <sub>p</sub>	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V <sub>p</sub>	max.	45 V
Peak output current	I <sub>OM</sub>	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T <sub>stg</sub>	-55 to + 150 °C	
Crystal temperature	T <sub>c</sub>	max.	150 °C

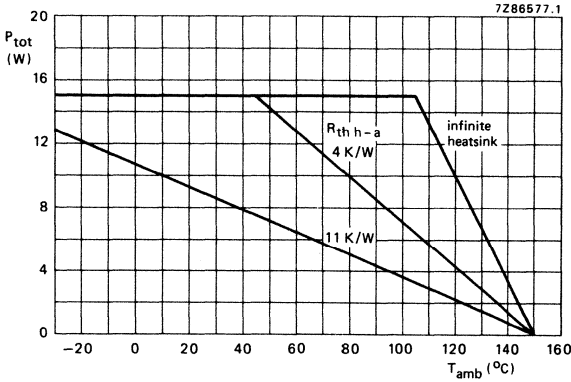


Fig. 2 Power derating curves.

**HEATSINK DESIGN EXAMPLE**

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)

maximum sine-wave dissipation: 12 W

T<sub>amb</sub> = 65 °C maximum

$$R_{th\ h-a} = \frac{150 - 65}{12} - 3 = 4\text{ K/W.}$$

2 x 7 W stereo (4 Ω)

maximum sine-wave dissipation: 6 W

T<sub>amb</sub> = 65 °C maximum

$$R_{th\ h-a} = \frac{150 - 65}{6} - 3 = 11\text{ K/W.}$$



**D.C. CHARACTERISTICS**

Supply voltage range (pin 10)	$V_P$		6 to 18 V
Repetitive peak output current	$I_{ORM}$	<	4 A
Total quiescent current	$I_{tot}$	typ. <	75 mA 150 mA
Stand-by current	$I_{sb}$	<	2 mA
Switch-on current (pin 11) at $V_{11} \leq V_{10}$ (note 1)	$I_{so}$	typ. <	0,35 mA 0,8 mA

**A.C. CHARACTERISTICS**

$T_{amb} = 25\text{ }^\circ\text{C}$ ;  $V_P = 14,4\text{ V}$ ;  $f = 1\text{ kHz}$ ; unless otherwise specified

**Bridge tied load application (BTL); see Fig. 3**

Output power at  $R_L = 4\text{ }\Omega$  (with bootstrap)

$V_P = 14,4\text{ V}$ ; $d_{tot} = 0,5\%$	$P_O$	>	15,5 W typ. 18,0 W
$V_P = 14,4\text{ V}$ ; $d_{tot} = 10\%$	$P_O$	>	20 W typ. 24 W
$V_P = 13,2\text{ V}$ ; $d_{tot} = 0,5\%$	$P_O$	typ.	15 W
$V_P = 13,2\text{ V}$ ; $d_{tot} = 10\%$	$P_O$	typ.	20 W
Open loop voltage gain	$G_O$	typ.	75 dB
Closed loop voltage gain (note 2)	$G_C$	typ.	40 ( $\pm 0,5$ ) dB
Frequency response at $-3\text{ dB}$ (note 3)	B		20 Hz to min. 20 kHz
Input impedance (note 4)	$ Z_i $	>	1 M $\Omega$
Noise output voltage (r.m.s. value) at $f = 20\text{ Hz}$ to 20 kHz	$V_{n(rms)}$	typ.	0,2 mV
$R_S = 0\text{ }\Omega$	$V_{n(rms)}$	typ. <	0,35 mV 0,8 mV
$R_S = 10\text{ k}\Omega$	$V_n$	typ.	0,25 mV
$R_S = 10\text{ k}\Omega$ ; according to IEC 179 curve A			
Supply voltage ripple rejection (note 5)	RR	>	42 dB typ. 50 dB
$f = 100\text{ Hz}$		<	50 mV typ. 2 mV
D.C. output offset voltage between the outputs	$ \Delta_{5-g} $		
Loudspeaker protection (if one of the 2 outputs is short-circuited to ground)			
maximum d.c. voltage (across the load)	$ \Delta V_{5-g} $	<	1 V
Power bandwidth; $-1\text{ dB}$ ; $d_{tot} = 0,5\%$	B		30 Hz to 40 kHz





**Stereo application;** see Fig. 4

Output power at  $d_{\text{tot}} = 10\%$ ; with bootstrap (note 6)

$$V_P = 14,4 \text{ V}; R_L = 4 \Omega$$

$P_o$	>	6 W
	typ.	7 W

$$V_P = 14,4 \text{ V}; R_L = 2 \Omega$$

$P_o$	>	10 W
	typ.	12 W

$$V_P = 13,2 \text{ V}; R_L = 4 \Omega$$

$P_o$	typ.	6 W
-------	------	-----

$$V_P = 13,2 \text{ V}; R_L = 2 \Omega$$

$P_o$	typ.	10 W
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Output power at  $d_{\text{tot}} = 0,5\%$ ; with bootstrap (note 6)

$$V_P = 14,4 \text{ V}; R_L = 4 \Omega$$

$P_o$	typ.	5,5 W
-------	------	-------

$$V_P = 14,4 \text{ V}; R_L = 2 \Omega$$

$P_o$	typ.	9,0 W
-------	------	-------

$$V_P = 13,2 \text{ V}; R_L = 4 \Omega$$

$P_o$	typ.	4,5 W
-------	------	-------

$$V_P = 13,2 \text{ V}; R_L = 2 \Omega$$

$P_o$	typ.	7,5 W
-------	------	-------

Output power at  $d_{\text{tot}} = 10\%$ ; without bootstrap

$$V_P = 14,4 \text{ V}; R_L = 4 \Omega \text{ (notes 6, 8 and 9)}$$

$P_o$	typ.	6 W
-------	------	-----

Frequency response;  $-3 \text{ dB}$  (note 3)

B	40 Hz to min. 20 kHz	
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Supply voltage ripple rejection (note 5)

$$f = 1 \text{ kHz}$$

RR	typ.	50 dB
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Channel separation;  $R_S = 10 \text{ k}\Omega$ ;  $f = 1 \text{ kHz}$

$\alpha$	>	40 dB
	typ.	50 dB

Closed loop voltage gain (note 7)

$G_c$	typ.	40 dB
-------	------	-------

Noise output voltage (r.m.s. value) at  $f = 20 \text{ Hz}$  to  $20 \text{ kHz}$

$$R_S = 0 \Omega$$

$V_{n(\text{rms})}$	typ.	0,15 mV
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$$R_S = 10 \text{ k}\Omega$$

$V_{n(\text{rms})}$	typ.	0,25 mV
---------------------	------	---------

$$R_S = 10 \text{ k}\Omega; \text{ according to IEC curve A}$$

$V_n$	typ.	0,2 mV
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## Notes

1. If  $V_{11} > V_{10}$ , then  $I_{11}$  must be  $\leq 10 \text{ mA}$ .
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. ←
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 k $\Omega$ .
5. Supply voltage ripple rejection measured with a source impedance of 0  $\Omega$  (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components. ←
8. A resistor of 56 k $\Omega$  between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100  $\mu\text{F}$  capacitor between pins 5 and 6 (or 8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

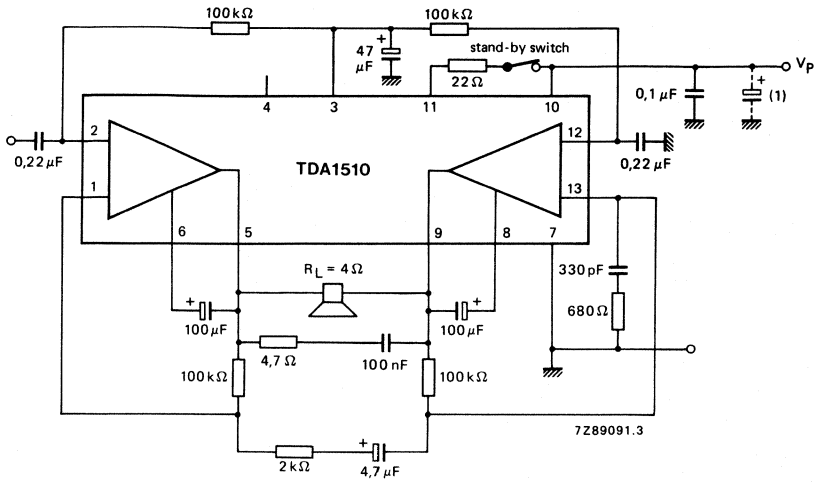


Fig. 3 Test and application circuit bridge tied load (BTL).

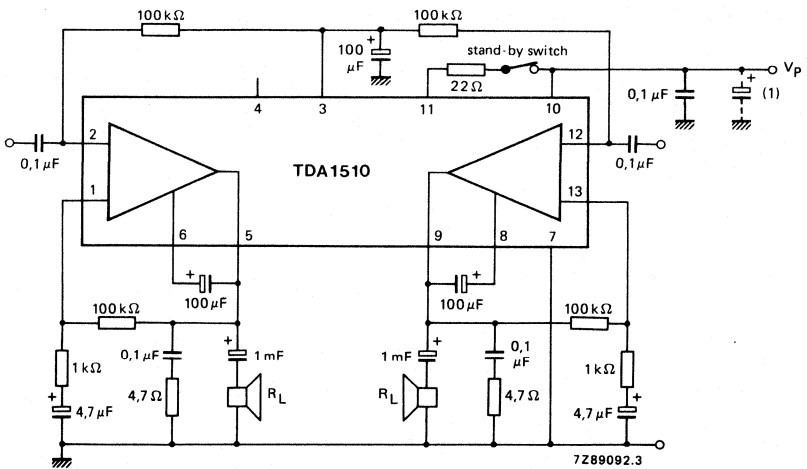


Fig. 4 Test and application circuit stereo mode.

(1) Belongs to power supply.

## 12 TO 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.

Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

### QUICK REFERENCE DATA

Supply voltage range	$V_p$	15 to 35 V
Total quiescent current at $V_p = 25$ V	$I_{tot}$	typ. 65 mA
Output power at $d_{tot} = 0,7\%$ sine-wave power		
$V_p = 25$ V; $R_L = 4 \Omega$	$P_o$	typ. 13 W
$V_p = 25$ V; $R_L = 8 \Omega$	$P_o$	typ. 7 W
music power		
$V_p = 32$ V; $R_L = 4 \Omega$	$P_o$	typ. 21 W
$V_p = 32$ V; $R_L = 8 \Omega$	$P_o$	typ. 12 W
Closed-loop voltage gain (externally determined)	$G_c$	typ. 30 dB
Input resistance (externally determined)	$R_i$	typ. 20 k $\Omega$
Signal-to-noise ratio at $P_o = 50$ mW	S/N	typ. 72 dB
Supply voltage ripple rejection at $f = 100$ Hz	RR	typ. 50 dB

### PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).

TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

**PINNING**

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply ( $V_p$ )
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

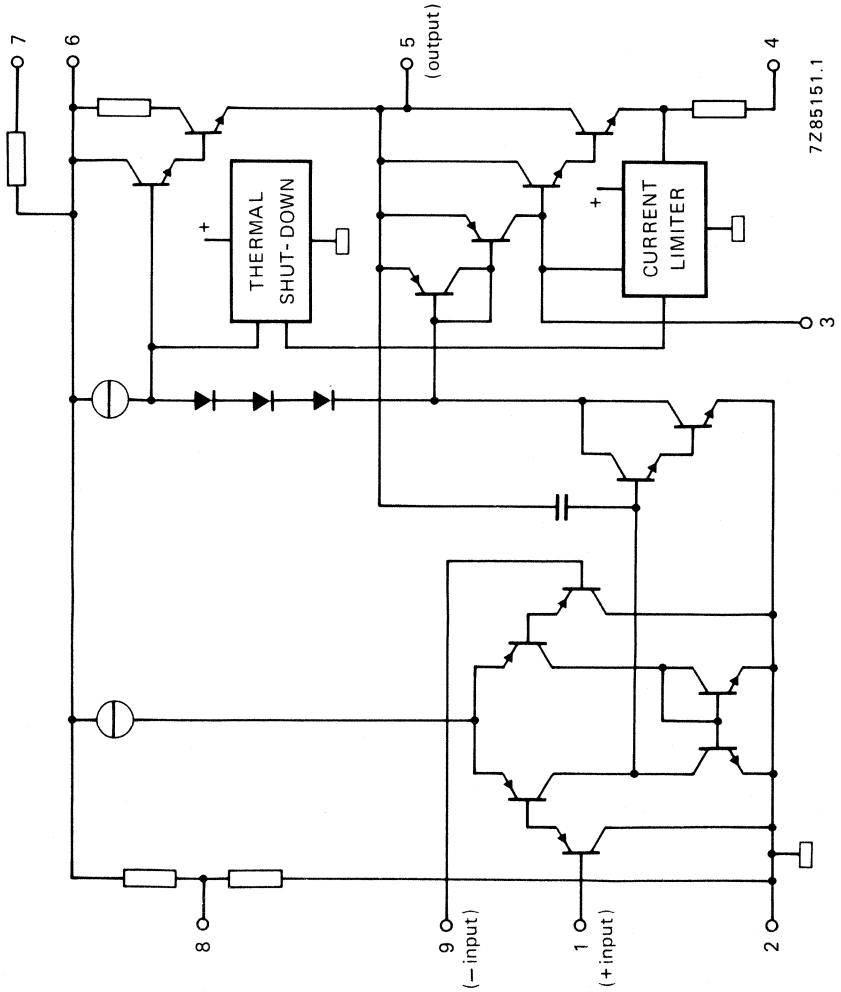


Fig. 1 Simplified internal circuit diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P$	max.	35 V
Repetitive peak output current	$I_{ORM}$	max.	3,2 A
Non-repetitive peak output current	$I_{OSM}$	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	$T_{stg}$	-55 to + 150 °C	
Operating ambient temperature	$T_{amb}$	-25 to + 150 °C	
A.C. short-circuit duration of load during full-load sine-wave drive			
$R_L = 0$ ; $V_P = 30$ V with $R_i = 4 \Omega$	$t_{sc}$	max.	100 hours

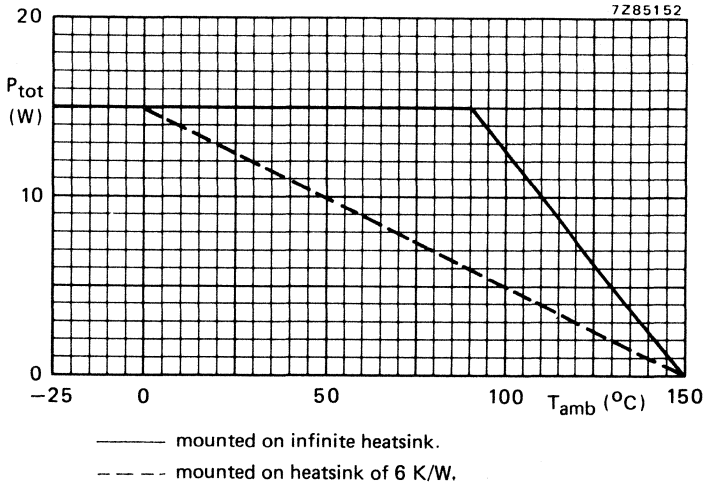


Fig. 2 Power derating curves.

**THERMAL RESISTANCE**

From junction to mounting base	$R_{th\ j-mb}$	typ.	3 K/W
		≤	4 K/W



**D.C. CHARACTERISTICS**

Supply voltage range	$V_p$		15 to 35 V
Total quiescent current at $V_p = 25$ V	$I_{tot}$	typ.	65 mA

**A.C. CHARACTERISTICS**

$V_p = 25$  V;  $R_L = 4 \Omega$ ;  $f = 1$  kHz;  $T_{amb} = 25$  °C; measured in test circuit of Fig. 3; unless otherwise specified

**Output power**

sine-wave power at  $d_{tot} = 0,7$  %

$R_L = 4 \Omega$	$P_o$	typ.	13 W
$R_L = 8 \Omega$	$P_o$	typ.	7 W

music power at  $V_p = 32$  V

$R_L = 4 \Omega$ ; $d_{tot} = 0,7$ %	$P_o$	typ.	21 W
$R_L = 4 \Omega$ ; $d_{tot} = 10$ %	$P_o$	typ.	25 W
$R_L = 8 \Omega$ ; $d_{tot} = 0,7$ %	$P_o$	typ.	12 W
$R_L = 8 \Omega$ ; $d_{tot} = 10$ %	$P_o$	typ.	15 W

Power bandwidth; $-1,5$ dB; $d_{tot} = 0,7$ %	B		40 Hz to 16 kHz
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**Voltage gain**

open-loop	$G_o$	typ.	74 dB
closed-loop	$G_c$	typ.	30 dB

**Input resistance (pin 1)**

Input resistance (pin 1)	$R_i$	>	100 k $\Omega$
Input resistance of test circuit (Fig. 3)	$R_i$	typ.	20 k $\Omega$

**Input sensitivity**

for $P_o = 50$ mW	$V_i$	typ.	16 mV
for $P_o = 10$ W	$V_i$	typ.	210 mV

**Signal-to-noise ratio**

at $P_o = 50$ mW; $R_S = 2$ k $\Omega$ ; $f = 20$ Hz to 20 kHz; unweighted	S/N	>	68 dB
---	-----	---	-------

weighted; measured according to IEC 173 (A-curve)

	S/N	typ.	76 dB
--	-----	------	-------

**Ripple rejection at  $f = 100$  Hz**

Ripple rejection at $f = 100$ Hz	RR	typ.	50 dB
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**Total harmonic distortion at  $P_o = 10$  W**

Total harmonic distortion at $P_o = 10$ W	$d_{tot}$	typ.	0,1 %
		<	0,3 %

**Output resistance (pin 5)**

Output resistance (pin 5)	$R_o$	typ.	0,1 $\Omega$
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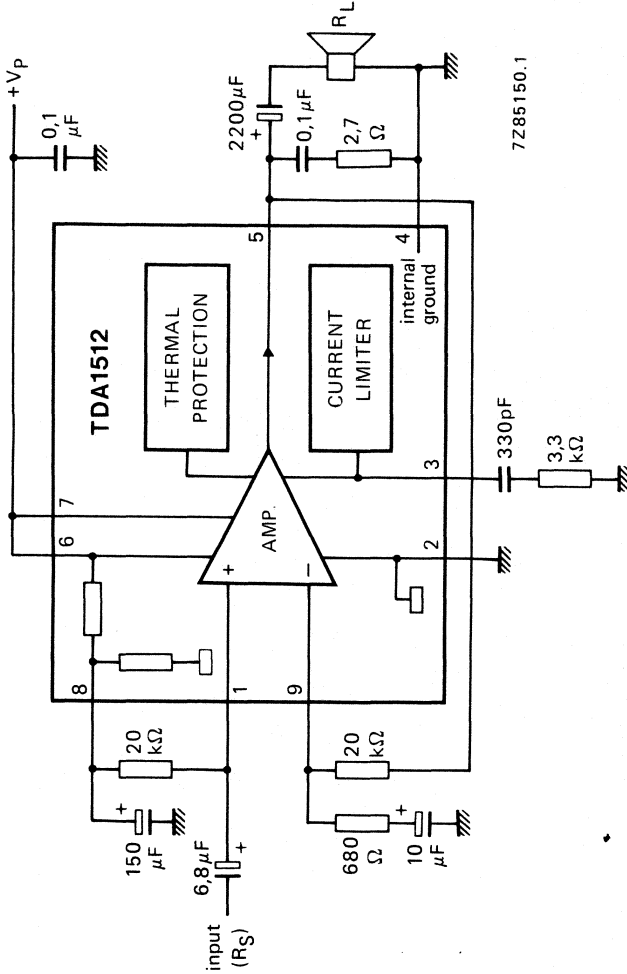


Fig. 3 Test circuit.



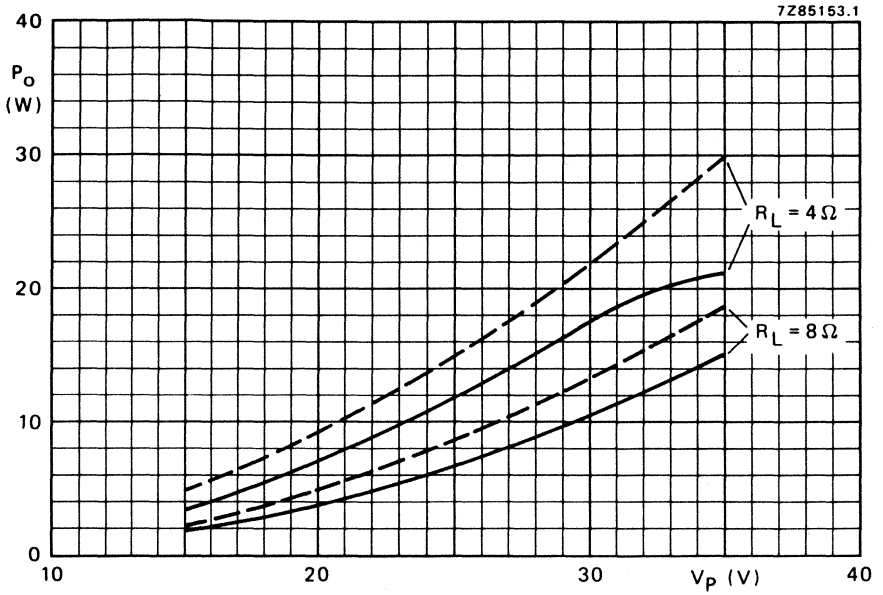


Fig. 4 Output power as a function of the supply voltage;  $f = 1\text{ kHz}$ ;  
—  $d_{tot} = 0,7\%$ ; - - -  $d_{tot} = 10\%$ .

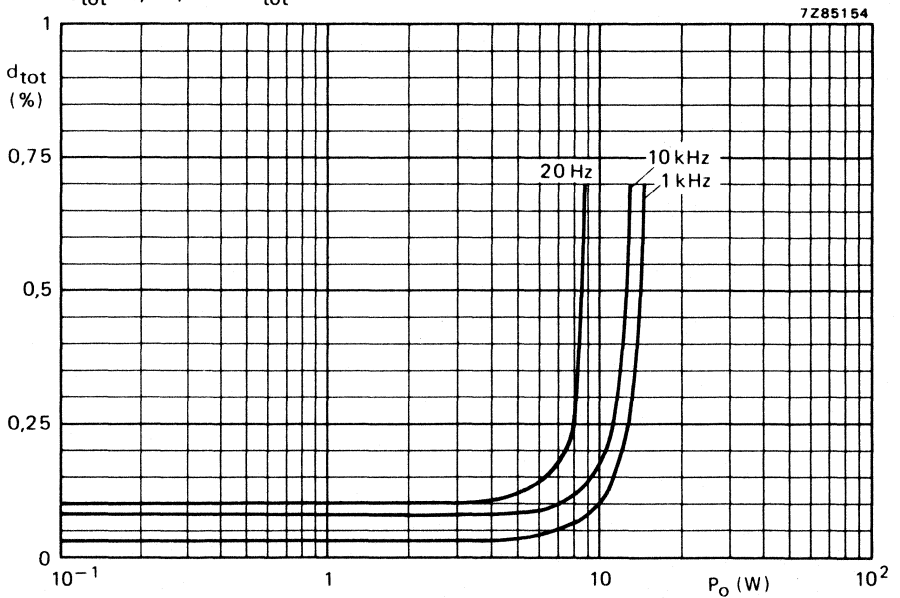


Fig. 5 Total harmonic distortion as a function of the output power.



## 21 W BTL OR 2 x 11 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515 is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6  $\Omega$ ). At a supply voltage  $V_p = 14,4$  V, an output power of 21 W can be delivered into a 4  $\Omega$  BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 11 W into 2  $\Omega$  or 2 x 6,5 W into 4  $\Omega$ .

Special features are:

- flexibility in use – mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1  $\mu$ A), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- a.c. and d.c. short-circuit safe to ground up to  $V_p = 18$  V
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

### QUICK REFERENCE DATA

Supply voltage range (operating)	$V_p$		6 to 18 V
Supply voltage (non-operating)	$V_p$	max.	28 V
Supply voltage (non-operating; load dump protection)	$V_p$	max.	45 V
Repetitive peak output current	$I_{ORM}$	max.	4 A
Total quiescent current	$I_{tot}$	typ.	75 mA
Stand-by current	$I_{sb}$	typ.	0 $\mu$ A
Switch-on current	$I_{so}$	<	100 $\mu$ A
Input impedance	$ Z_i $	>	1 M $\Omega$
<b>Bridge tied load application (BTL)</b>	$V_p$	=	14,4   13,2 V
Output power at $R_L = 4 \Omega$ (with bootstrap)	$P_o$	typ.	16   14 W
$d_{tot} = 0,5\%$	$P_o$	typ.	21   18 W
$d_{tot} = 10\%$	RR	typ.	50   50 dB
Supply voltage ripple rejection; $R_S = 0 \Omega$ ; $f = 100$ Hz	$ \Delta V_{5-g} $	<	50   50 mV
D.C. output offset voltage between the outputs			
<b>Stereo application</b>			
Output power at $d_{tot} = 10\%$ (with bootstrap)	$P_o$	typ.	6,5   6 W
$R_L = 4 \Omega$	$P_o$	typ.	11   10 W
$R_L = 2 \Omega$			
Output power at $d_{tot} = 0,5\%$ (with bootstrap)	$P_o$	typ.	5   4,5 W
$R_L = 4 \Omega$	$P_o$	typ.	8   7,5 W
$R_L = 2 \Omega$	$\alpha$	>	40   40 dB
Channel separation	$V_n$	typ.	0,2   0,2 mV
Noise output voltage; $R_S = 10$ k $\Omega$ ; according to IEC curve-A			

**PACKAGE OUTLINE** 13-lead SIL; plastic power (SOT-141B).

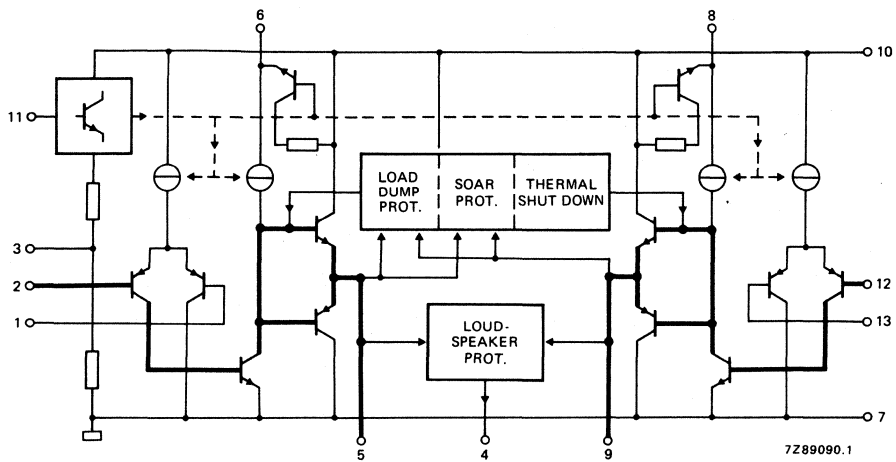


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V <sub>p</sub>	max.	18 V
Supply voltage; non-operating	V <sub>p</sub>	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V <sub>p</sub>	max.	45 V
Peak output current	I <sub>OM</sub>	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T <sub>stg</sub>	-55 to + 150 °C	
Crystal temperature	T <sub>c</sub>	max.	150 °C
A.C. and d.c. short-circuit safe voltage			max. 18 V
Reverse polarity			max. 10 V

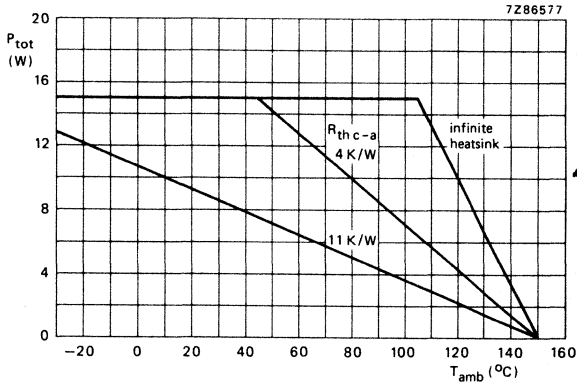


Fig. 2 Power derating curves.

**HEATSINK DESIGN EXAMPLE**

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

21 W BTL (4 Ω) or 2 x 11 W stereo (2 Ω)  
 maximum sine-wave dissipation: 12 W  
 T<sub>amb</sub> = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{12} - 3 = 4\text{ K/W.}$$

2 x 6,5 W stereo (4 Ω)  
 maximum sine-wave dissipation: 6 W  
 T<sub>amb</sub> = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{6} - 3 = 11\text{ K/W.}$$



## D.C. CHARACTERISTICS

Supply voltage range (pin 10)	$V_P$		6 to 18 V
Repetitive peak output current	$I_{ORM}$	<	4 A
Total quiescent current	$I_{tot}$	typ.	75 mA
Switching level 11 : OFF	$V_{11}$	<	1,8 V
ON	$V_{11}$	>	3 V
Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1,8$ V)	$ Z_{OFF} $	>	100 k $\Omega$
Stand-by current at $V_{11} = 0$ to 0,8 V	$I_{sb}$	typ. <	1 $\mu$ A 200 $\mu$ A
Switch-on current (pin 11) at $V_{11} \leq V_{10}$ (note 1)	$I_{so}$	typ. <	10 $\mu$ A 100 $\mu$ A

## A.C. CHARACTERISTICS

$T_{amb} = 25$  °C;  $V_P = 14,4$  V;  $f = 1$  kHz; unless otherwise specified

### Bridge tied load application (BTL); see Fig. 3

Output power at $R_L = 4$ $\Omega$ (with bootstrap) $V_P = 14,4$ V; $d_{tot} = 0,5\%$	$P_O$	> typ.	15,5 W 16 W
$V_P = 14,4$ V; $d_{tot} = 10\%$	$P_O$	> typ.	20 W 21 W
$V_P = 13,2$ V; $d_{tot} = 0,5\%$	$P_O$	typ.	14 W
$V_P = 13,2$ V; $d_{tot} = 10\%$	$P_O$	typ.	18 W
Open loop voltage gain	$G_O$	typ.	75 dB
Closed loop voltage gain (note 2)	$G_C$	typ.	40 ( $\pm$ 0,5) dB
Frequency response at $-3$ dB (note 3)	B		20 Hz to min. 20 kHz
Input impedance (note 4)	$ Z_i $	>	1 M $\Omega$
Noise input voltage (r.m.s. value) at $f = 20$ Hz to 20 kHz $R_S = 0$ $\Omega$	$V_{n(rms)}$	typ.	0,2 mV
$R_S = 10$ k $\Omega$	$V_{n(rms)}$	typ. <	0,35 mV 0,8 mV
$R_S = 10$ k $\Omega$ ; according to IEC 179 curve A	$V_n$	typ.	0,25 mV
Supply voltage ripple rejection (note 5) $f = 100$ Hz	RR	> typ.	42 dB 50 dB
D.C. output offset voltage between the outputs	$ \Delta V_{5-g} $	<	50 mV
Loudspeaker protection (all conditions)		typ.	2 mV
maximum d.c. voltage (across the load)	$ \Delta V_{5-g} $	<	1 V
Power bandwidth; $-1$ dB; $d_{tot} = 0,5\%$	B		30 Hz to 30 kHz

**Stereo application; see Fig. 4**

Output power at $d_{\text{tot}} = 10\%$ ; with bootstrap (note 6)			
$V_P = 14,4 \text{ V}; R_L = 4 \Omega$	$P_o$	>	6 W
		typ.	6,5 W
$V_P = 14,4 \text{ V}; R_L = 2 \Omega$	$P_o$	>	10 W
		typ.	11 W
$V_P = 13,2 \text{ V}; R_L = 4 \Omega$	$P_o$	typ.	6 W
$V_P = 13,2 \text{ V}; R_L = 2 \Omega$	$P_o$	typ.	10 W
Output power at $d_{\text{tot}} = 0,5\%$ ; with bootstrap (note 6)			
$V_P = 14,4 \text{ V}; R_L = 4 \Omega$	$P_o$	typ.	5 W
$V_P = 14,4 \text{ V}; R_L = 2 \Omega$	$P_o$	typ.	8 W
$V_P = 13,2 \text{ V}; R_L = 4 \Omega$	$P_o$	typ.	4,5 W
$V_P = 13,2 \text{ V}; R_L = 2 \Omega$	$P_o$	typ.	7,5 W
Output power at $d_{\text{tot}} = 10\%$ ; without bootstrap			
$V_P = 14,4 \text{ V}; R_L = 4 \Omega$ (notes 6, 8 and 9)	$P_o$	typ.	5,5 W
Frequency response at $-3 \text{ dB}$ (note 3)	B		40 Hz to min. 20 kHz
Supply voltage ripple rejection (note 5)	RR	typ.	50 dB
Channel separation; $R_S = 10 \text{ k}\Omega; f = 1 \text{ kHz}$	$\alpha$	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	$G_c$	typ.	40 dB
Noise output voltage (r.m.s. value) at $f = 20 \text{ Hz}$ to $20 \text{ kHz}$			
$R_S = 0 \Omega$	$V_n(\text{rms})$	typ.	0,15 mV
$R_S = 10 \text{ k}\Omega$	$V_n(\text{rms})$	typ.	0,25 mV
$R_S = 10 \text{ k}\Omega$ ; according to IEC curve A	$V_n$	typ.	0,2 mV

**Notes**

1. The internal circuit impedance at pin 11 is  $> 5 \text{ k}\Omega$  if  $V_{11} > V_{10}$ .
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 k $\Omega$ .
5. Supply voltage ripple rejection measured with a source impedance of 0  $\Omega$  (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 k $\Omega$  between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100  $\mu\text{F}$  capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

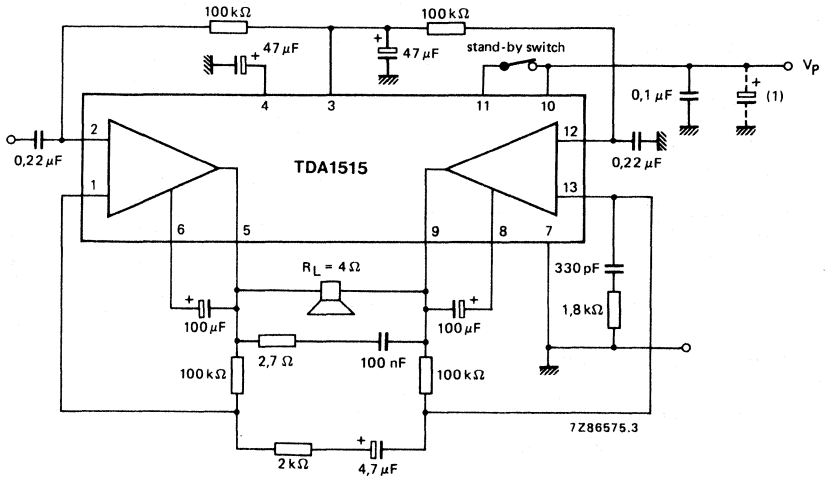


Fig. 3 Test/application circuit bridge tied load (BTL).

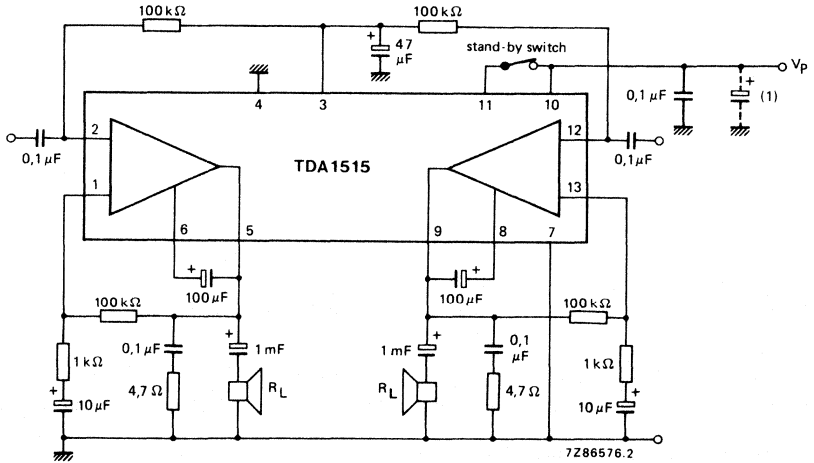


Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.

## 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1520 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.

Special features are:

- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected

### QUICK REFERENCE DATA

Supply voltage range	$V_P$	15 to 40 V
Total quiescent current at $V_P = 33$ V	$I_{tot}$	typ. 54 mA
Output power at $d_{tot} = 0,5\%$ sine-wave power	$P_O$	typ. 22 W
$V_P = 33$ V; $R_L = 4 \Omega$	$P_O$	> 16 W
$V_P = 33$ V; $R_L = 4 \Omega$	$P_O$	typ. 11 W
$V_P = 33$ V; $R_L = 8 \Omega$	$P_O$	typ. 11 W
Closed-loop voltage gain (externally determined)	$G_C$	typ. 30 dB
Input resistance (externally determined by $R_{g,1}$ )	$R_i$	typ. 20 k $\Omega$
Signal-to-noise ratio at $P_O = 50$ mW	S/N	typ. 75 dB
Supply voltage ripple rejection at $f = 100$ Hz	RR	typ. 60 dB

### PACKAGE OUTLINE

TDA1520 : 9-lead SIL; plastic power (SOT-131A).

TDA1520Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

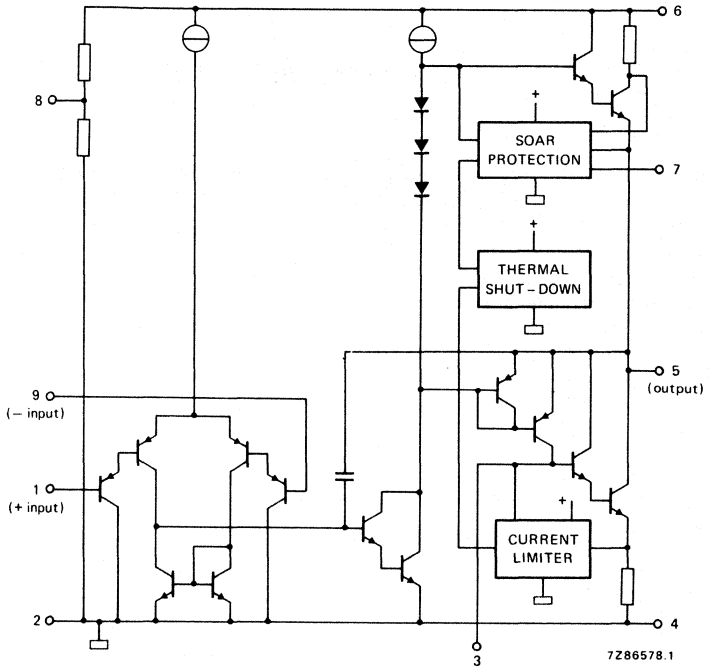


Fig. 1 Simplified internal circuit diagram.

**PINNING**

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (Vp)
7. Internally connected
8. Ripple rejection
9. Inverting input (feedback)



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p$	max.	44 V
Repetitive peak output current	$I_{ORM}$	max.	4 A
Non-repetitive peak output current	$I_{OSM}$	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	$T_{stg}$	-55 to +150 °C	
Operating ambient temperature	$T_{amb}$	-25 to +150 °C	
A.C. short-circuit duration of load during full-load sine-wave drive	$t_{sc}$	max.	1 hour ←
$R_L = 0; V_p = 28 V$ with $R_i = 4 \Omega$ and $f > 20 Hz$			

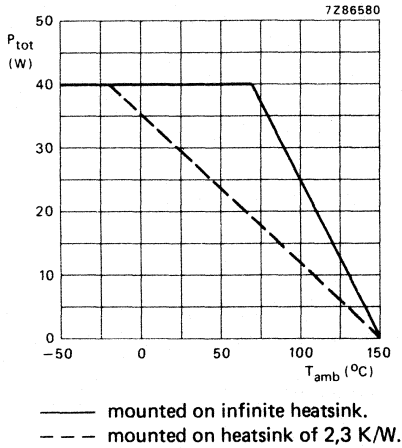


Fig. 2 Power derating curves.

**THERMAL RESISTANCE**

From junction to mounting base  $R_{th j-mb} \leq 2 K/W$



# TDA1520

## TDA1520Q

### D.C. CHARACTERISTICS

Supply voltage range	$V_P$	15 to 40 V
Total quiescent current at $V_P = 33$ V	$I_{tot}$	22 to 105 mA typ. 54 mA

### A.C. CHARACTERISTICS

$V_P = 33$  V;  $R_L = 4 \Omega$ ;  $f = 1$  kHz;  $T_{amb} = 25$  °C; measured in test circuit of Fig. 3; unless otherwise specified

#### Output power

sine-wave power at  $d_{tot} = 0,5\%$

$R_L = 4 \Omega$

$P_O$  typ. 22 W

$R_L = 4 \Omega$

$P_O >$  16 W

$R_L = 8 \Omega$

$P_O$  typ. 11 W

Power bandwidth;  $-3$  dB;  $d_{tot} = 0,5\%$

B 20 Hz to 20 kHz

#### Voltage gain

open-loop

$G_O$  typ. 74 dB

closed-loop

$G_C$  typ. 30 dB

Input resistance (pin 1)

$R_i >$  1 M $\Omega$

Input resistance of test circuit (Fig. 3)

$R_i$  typ. 20 k $\Omega$

Input sensitivity

for  $P_O = 50$  mW

$V_i$  typ. 16 mV

for  $P_O = 16$  W

$V_i$  typ. 260 mV

Signal-to-noise ratio

at  $P_O = 50$  mW;  $R_S = 2$  k $\Omega$ ;

$f = 20$  Hz to 20 kHz; unweighted

S/N typ. 75 dB

weighted; measured according to

IEC 179 (A-curve)

S/N typ. 80 dB

Supply voltage ripple rejection at  $f = 100$  Hz

RR typ. 65 dB

Total harmonic distortion at  $P_O = 16$  W

$d_{tot}$  typ. 0,01 %

Output resistance (pin 5)

$R_o$  typ. 0,01  $\Omega$

$R_o <$  0,1  $\Omega$







## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1520A  
TDA1520AQ

# 20 W HI-FI AUDIO POWER AMPLIFIER

## GENERAL DESCRIPTION

The TDA1520A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.

### Features

- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected
- Very low internal thermal resistance
- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Complete SOAR protection

### QUICK REFERENCE DATA

Supply voltage range	$V_p$	15 to 50 V
Total quiescent current at $V_p = 33$ V	$I_{tot}$	typ. 70 mA
Output power at $d_{tot} = 0,5\%$ sine-wave power		
$V_p = 33$ V; $R_L = 4 \Omega$	$P_o$	typ. 22 W
$V_p = 33$ V; $R_L = 4 \Omega$	$P_o$	> 20 W
$V_p = 42$ V; $R_L = 8 \Omega$	$P_o$	typ. 20 W
Closed-loop voltage gain (externally determined)	$G_c$	typ. 30 dB
Input resistance (externally determined by $R_{g.1}$ )	$R_i$	typ. 20 k $\Omega$
Signal-to-noise ratio at $P_o = 50$ mW	S/N	typ. 76 dB
Supply voltage ripple rejection at $f = 100$ Hz	RR	typ. 60 dB

### PACKAGE OUTLINE

TDA1520A : 9-lead SIL; plastic power (SOT-131A).

TDA1520AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

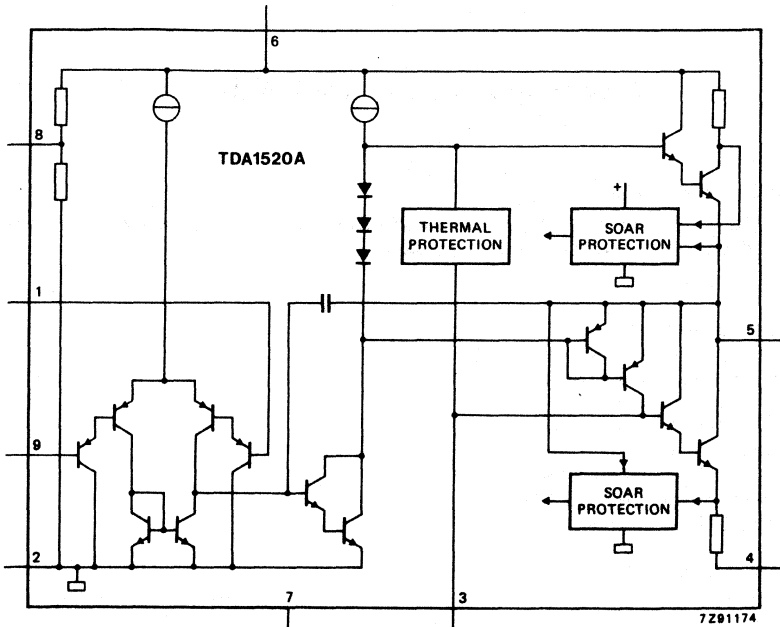


Fig. 1 Simplified internal circuit diagram.

**PINNING**

- 1. Non-inverting input
- 2. Input ground (substrate)
- 3. Compensation
- 4. Negative supply (ground)
- 5. Output
- 6. Positive supply ( $V_p$ )
- 7. Not connected
- 8. Ripple rejection
- 9. Inverting input (feedback)



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p$	max.	50 V
Repetitive peak output current	$I_{ORM}$	max.	4 A
Non-repetitive peak output current	$I_{OSM}$	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	$T_{stg}$	-55 to + 150 °C	
Operating ambient temperature	$T_{amb}$	-25 to + 150 °C	
Duration of a.c. short-circuit of load ( $R_L = 0 \Omega$ ) during full-load sine-wave drive at: $V_S = \pm 20$ V (symmetrical) and $R_{supply} = 0 \Omega$ ; or $V_S = 35$ V (asymmetrical) and $R_{supply} \geq 4 \Omega$	$t_{sc}$	max.	100 hours

DEVELOPMENT SAMPLE DATA

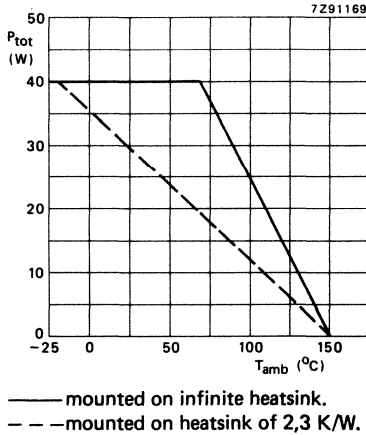


Fig. 2 Power derating curves.

**THERMAL RESISTANCE**

From junction to mounting base

$R_{th\ j-mb} \leq 2\ K/W$



**D.C. CHARACTERISTICS**

Supply voltage range	$V_P$	15 to 50 V
Total quiescent current at $V_P = 33$ V	$I_{tot}$	typ. 70 mA $\leq$ 105 mA
Minimum guaranteed output current (peak value)	$I_{ORM}$	$\geq$ 3,2 A

**A.C. CHARACTERISTICS**

$V_P = 33$  V;  $R_L = 4 \Omega$ ;  $f = 1$  kHz;  $T_{amb} = 25$  °C; measured in test circuit of Fig. 3; unless otherwise specified

**Output power**

sine-wave power at  $d_{tot} = 0,5\%$

$R_L = 4 \Omega$   
 $R_L = 4 \Omega$   
 $R_L = 8 \Omega; V_P = 42$  V

(Fig. 4)

$P_O$	typ.	22 W
$P_O$	$>$	20 W
$P_O$	typ.	20 W

Power bandwidth at  $d_{tot} = 0,5\%$  from  $P_O = 50$  mW to 10 W

B	20 Hz to	20 kHz
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**Voltage gain**

open-loop

closed-loop

$G_O$	typ.	74 dB
$G_C$	typ.	30 dB

Internal resistance of pin 1 (at  $R_{1-g} = \infty$ )

$R_i$	$>$	1 M $\Omega$
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Input resistance of test circuit at pin 1 (Fig. 3)

$R_i$	typ.	20 k $\Omega$
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**Input sensitivity**

for  $P_O = 16$  W

$V_i$	typ.	260 mV
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**Signal-to-noise ratio**

at  $P_O = 50$  mW;  $R_{source} = 2$  k $\Omega$

$f = 20$  Hz to 20 kHz; unweighted

weighted; measured according to

IEC 179 (A-curve)

S/N	typ.	76 dB
-----	------	-------

S/N	typ.	80 dB
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Ripple rejection at  $f = 100$  Hz;  $R_S = 0 \Omega$

RR	typ.	60 dB
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Total harmonic distortion at  $P_O = 16$  W

$d_{tot}$	typ.	0,01 %
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Output resistance (pin 5)

$R_O$	typ.	0,01 $\Omega$
-------	------	---------------

Input offset voltage

$V_{5-8}$	typ.	1 mV
	$<$	100 mV

Transient intermodulation distortion

at  $P_O = 10$  W

$d_{TIM}$	typ.	0,01 %
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Intermodulation distortion at  $P_O = 10$  W

$d_{IM}$	typ.	0,01 %
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Slew rate

SR	typ.	9 V/ $\mu$ s
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APPLICATION INFORMATION

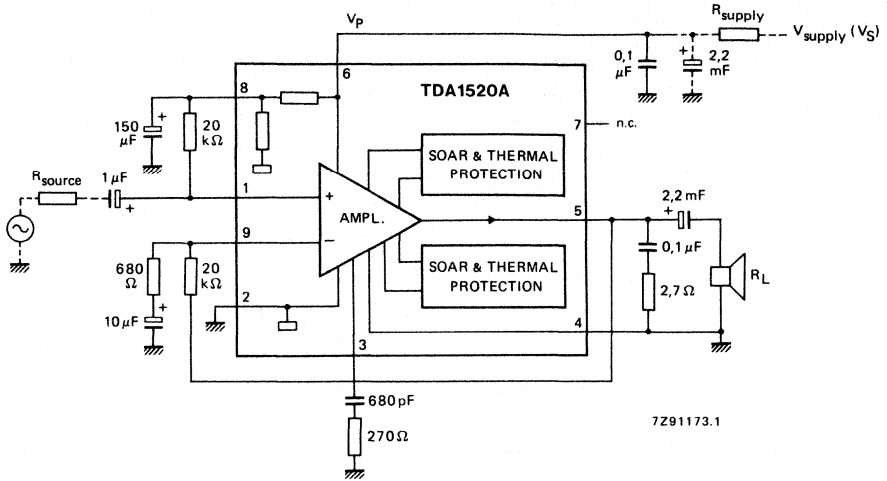


Fig. 3 Test and application circuit.

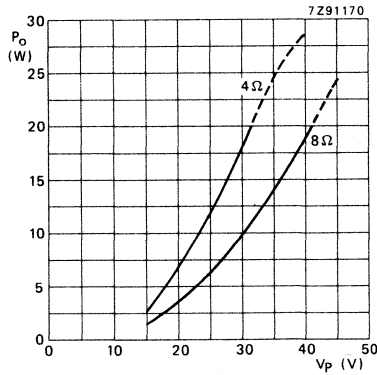


Fig. 4 Output power ( $P_o$ ) versus supply voltage ( $V_p$ ) at  $f = 1\text{ kHz}$ ,  $d_{tot} = 0,5\%$ ,  $G_v = 30\text{ dB}$ .

DEVELOPMENT I SAMPLE DATA



APPLICATION INFORMATION (continued)

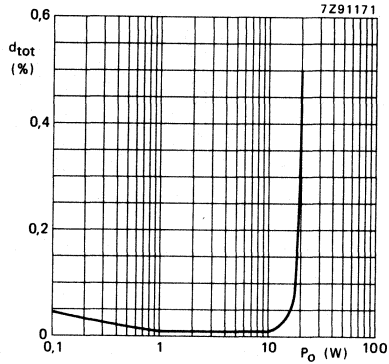


Fig. 5 Total harmonic distortion ( $d_{tot}$ ) versus output power ( $P_o$ ) at  $V_p = 33$  V,  $R_L = 4 \Omega$ ,  $f = 1$  kHz.

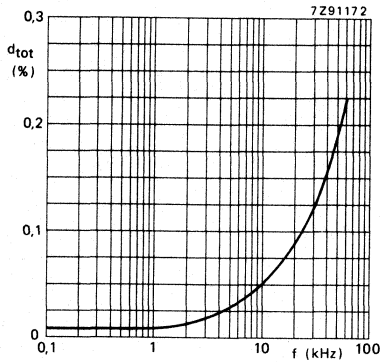


Fig. 6 Total harmonic distortion ( $d_{tot}$ ) versus operating frequency ( $f$ ) at  $V_p = 33$  V,  $R_L = 4 \Omega$ ,  $P_o = 10$  W (constant).

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1522

# STEREO CASSETTE HEAD PREAMPLIFIER AND EQUALIZER

## GENERAL DESCRIPTION

The TDA1522 is a playback amplifier for car radio/cassette players.

### Features

- Two independent amplifiers with open loop gain of typ. 90 dB
- Internal d.c. feedback via a 140 k $\Omega$  resistor from output to feedback point
- A.C. characteristics that can be determined externally by an RC network
- Electronic on/off switching with transient suppression for switch on
- Head input at d.c. ground that eliminates the input coupling capacitor
- Minimal external component requirement
- Stability down to a gain of 30 dB
- Low input noise
- Low distortion
- D.C. input current < 2  $\mu$ A
- Wide supply voltage range

## QUICK REFERENCE DATA

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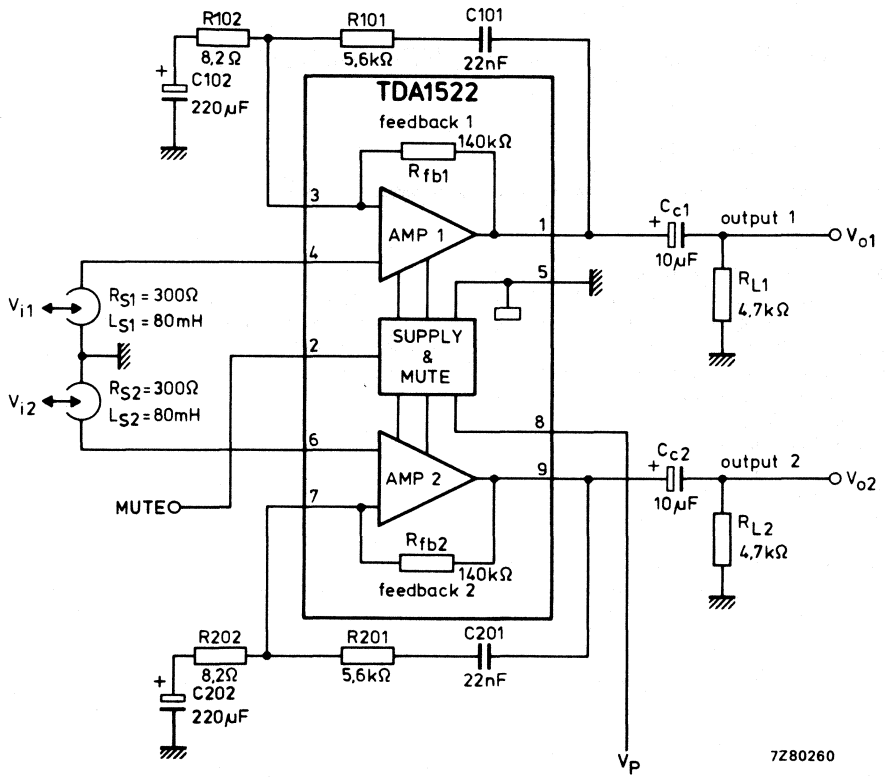
Supply voltage range (pin 8)	V <sub>p</sub>	7,5 to 23 V
Supply current (pin 8)	I <sub>p</sub>	typ. 5 mA
Operating ambient temperature range	T <sub>amb</sub>	-30 to +85 °C
Total harmonic distortion	THD	typ. 0,05 %
Channel separation at R <sub>S</sub> = 10 k $\Omega$ ; L <sub>S</sub> = 0	$\alpha$	min. 45 dB

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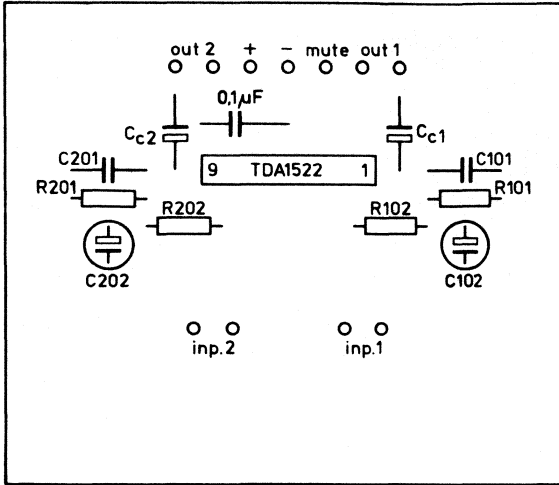
## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).



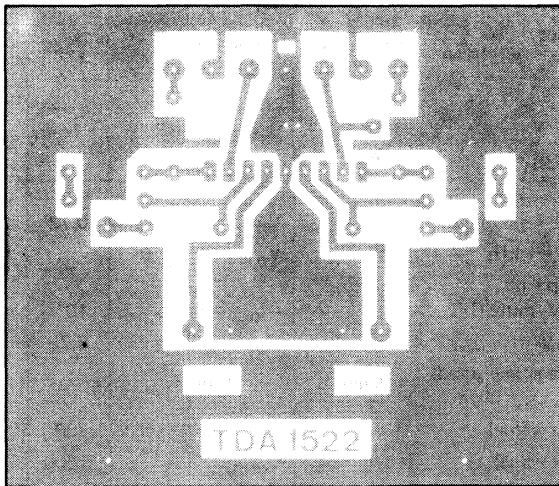
7Z80260

Fig. 1 Block diagram with external components; also used as test circuit.



7280266

Fig. 2 Printed-circuit board component side, showing component layout for circuit of Figure 1.



7280265

Fig. 3 Printed-circuit board, showing track side. Dimensions 75 mm x 65 mm.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	$V_p$	7,5 to 23 V
Power dissipation	$P_{tot}$	max. 800 mW
Feedback current (pins 3 and 7)	$I_{fb}$	max. 10 mA
Storage temperature range	$T_{stg}$	-55 to +150 °C
Operating ambient temperature range	$T_{amb}$	-30 to +85 °C

## Note

All pins except 3 and 7 (feedback) can be connected to  $V_p$  (pin 8) or ground, (pin 5).

## CHARACTERISTICS

 $V_p = 8,5 \text{ V}$ ;  $T_{amb} = 25 \text{ °C}$ ; test circuit Fig. 1 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 8)</b>					
Supply voltage range	$V_p$	7,5	—	23	V
Supply current	$I_p$	—	5	—	mA
<b>Inputs (pin 4 or 6)</b>					
Noise input voltage (unweighted; r.m.s. value) at $f = 20 \text{ Hz}$ to $20 \text{ kHz}^*$	$V_{n(rms)}$	—	1,6	—	$\mu\text{V}$
Noise input voltage at $R_S = 0$ ; $f = 1 \text{ kHz}^*$ , $**$	$V_n$	—	5	—	$n\text{V}\sqrt{\text{Hz}}$
Noise input current at $f = 1 \text{ kHz}^*$ , $\blacktriangle$	$I_n$	—	1,2	—	$\text{pA}\sqrt{\text{Hz}}$
D.C. input current at pins 4 and 6	$-I_4; -I_6$	—	—	2	$\mu\text{A}$
<b>Outputs (pin 1 or 9)</b>					
Output voltage at $V_i = 0,3 \text{ mV}$ ; $f = 315 \text{ Hz}$	$V_o$	—	0,72	—	V
at THD= 1%; $f = 1 \text{ kHz}$	$V_o$	1,0	—	—	V
Output source current at $V_{2.5} \geq 7,5 \text{ V}$ ; mute OFF	$-I_o$	5	10	—	mA
D.C. output voltage	$V_o$	—	3,7	—	V
Noise output voltage (weighted) at $R_S = 300 \Omega$ ; $L_S = 80 \text{ mH}$ as DIN A (r.m.s. value)	$V_{n(rms)}$	—	700	—	$\mu\text{V}$
as CCITT (peak value)	$V_{n(m)}$	—	1200	—	$\mu\text{V}$
as CCIR (peak value)	$V_{n(m)}$	—	1600	—	$\mu\text{V}$
Noise output voltage (unweighted) at $R_S = 300 \Omega$ ; $L_S = 80 \text{ mH}$ as DIN 45405 (peak value)	$V_{n(m)}$	—	1800	—	$\mu\text{V}$

\* Measured in Fig. 4. \*\* See also Fig. 6.  $\blacktriangle$  See also Fig. 7.

parameter	symbol	min.	typ.	max.	unit
<b>Mute on/off characteristics (pin 2)*</b>					
Mute ON voltage at mute switch closed	$V_m$	0	—	1	V
Mute ON current at mute switch closed or $V_{2.5} = 0$ V	$I_m$	—	2,7	—	$\mu$ A
Mute OFF voltage at mute switch open	$V_m$	7,5	—	$V_p$	V
<b>Impedance</b>					
Input impedance** at $f = 1$ kHz	$ Z_i $	200	—	—	$k\Omega$
Output impedance** at $f = 1$ kHz	$ Z_o $	—	—	1	$k\Omega$
<b>General</b>					
Internal feedback resistor**	$R_{fb}$	100	140	180	$k\Omega$
Open-loop voltage gain** at $f = 315$ Hz	$G_v$	—	90	—	dB
Channel separation at $R_S = 10$ $k\Omega$ ; $L_S = 0$ ; (note 1)	$\alpha$	45	—	—	dB
Power supply ripple rejection at $V_{P(rms)} = 0,1$ V; $f = 100$ Hz (note 2)	RR	90	95	—	dB
Total harmonic distortion at $f = 1$ kHz; $V_o = 0,72$ V (note 3)	THD	—	0,05	—	%

**Notes**

1. Frequency range 300 Hz to 20 kHz.
2. Referred to the input.
3. Measured selective.



\* See also Fig. 5.

\*\* Applies to each amplifier.

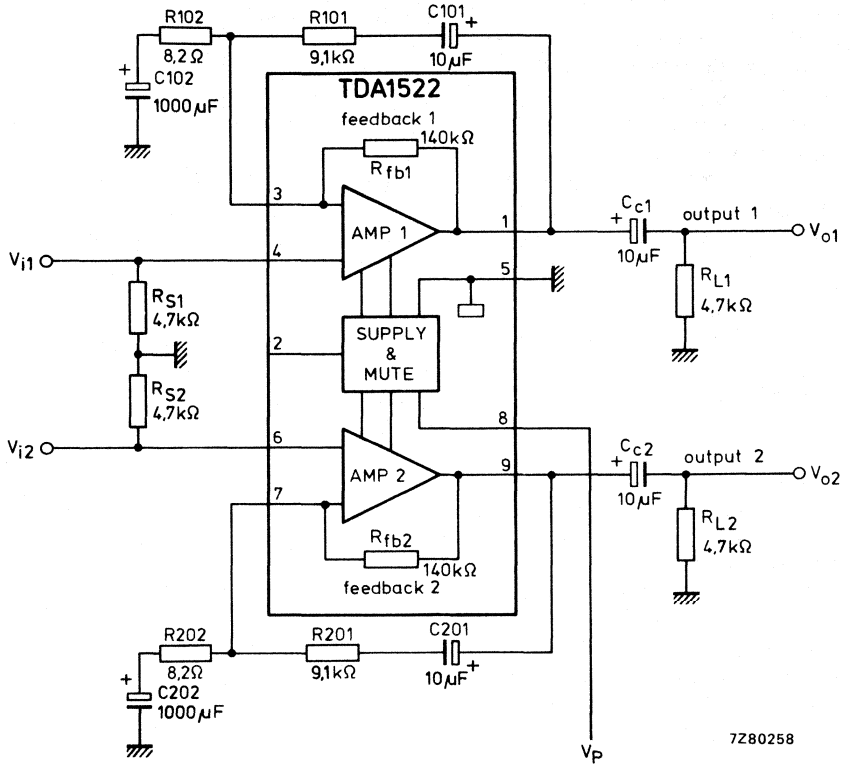


Fig. 4 Test circuit for noise measurement.

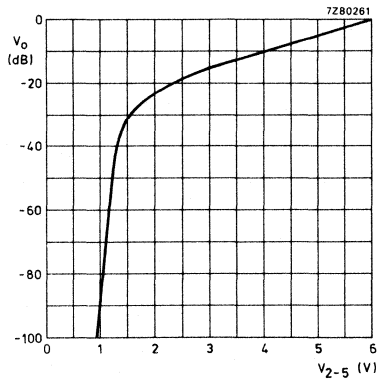


Fig. 5 Muting depth as a function of control voltage at pin 2.



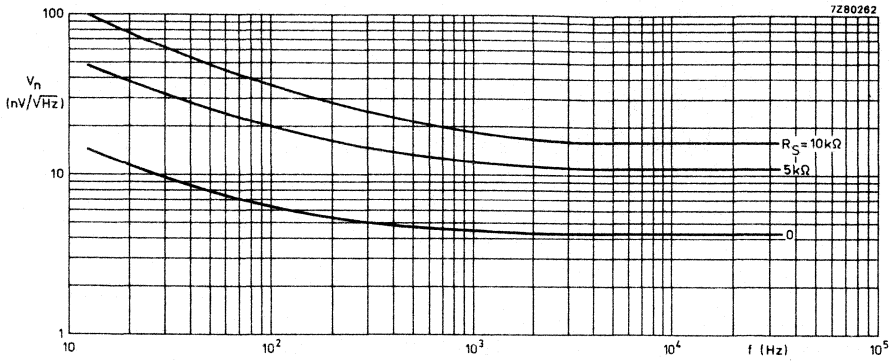


Fig. 6 Noise input voltage as a function of frequency.

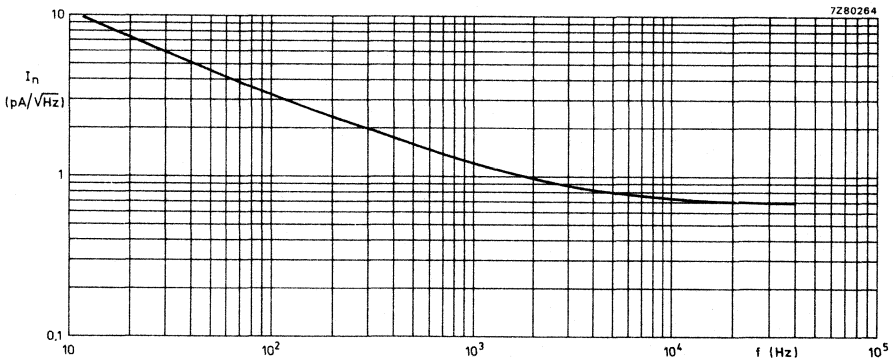


Fig. 7 Noise input current as a function of frequency.

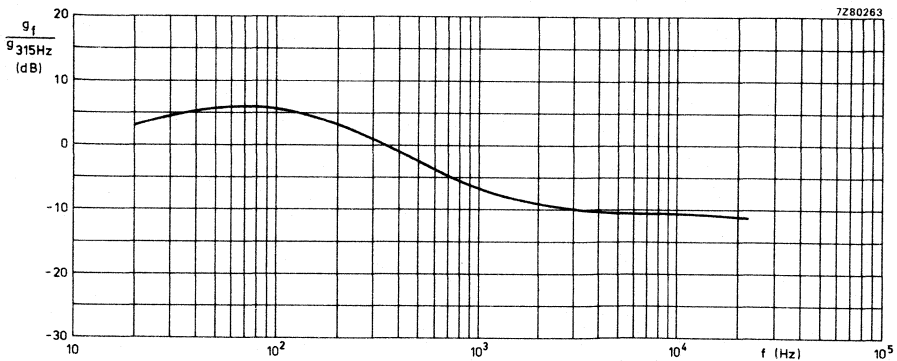


Fig. 8 Frequency response curve for the circuit in Figure 1.

APPLICATION INFORMATION

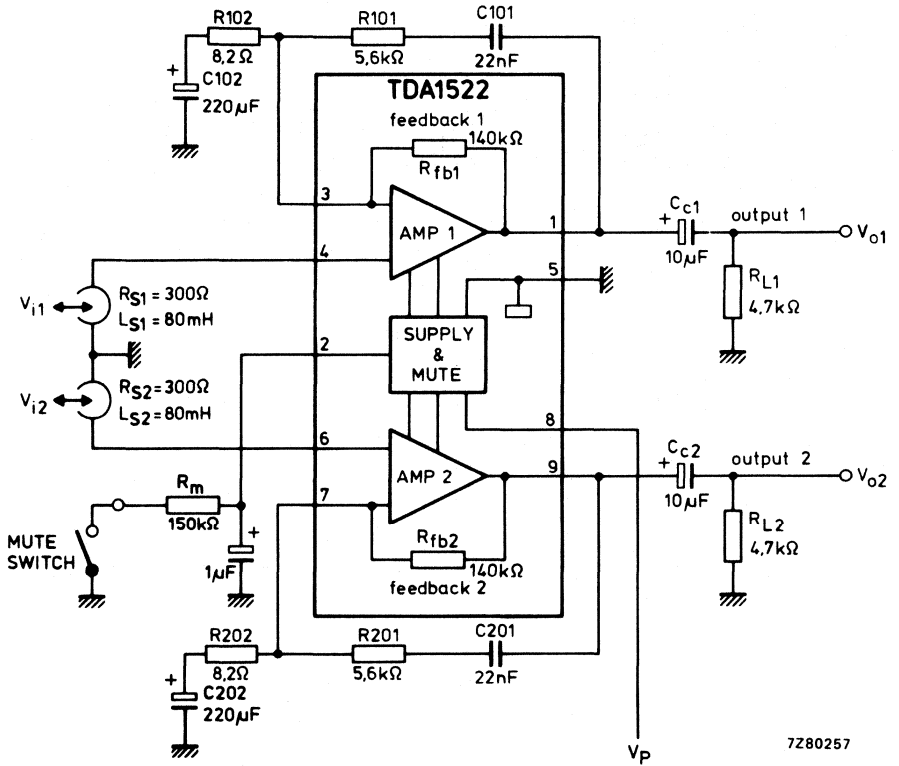
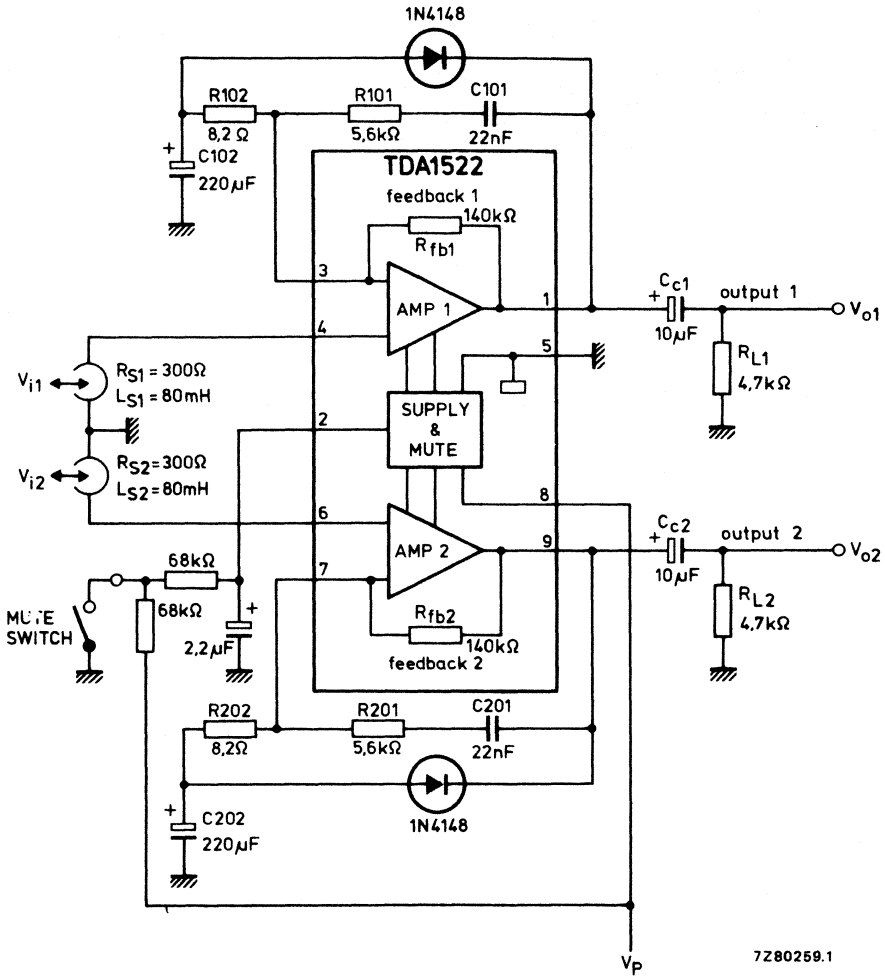


Fig. 9 Simple mute application.



7Z80259.1

Fig. 10 Application for pop-free muting.



Successor type is TDA1524A

## STEREO-TONE/VOLUME CONTROL CIRCUIT

### GENERAL DESCRIPTION

The TDA1524 is a monolithic integrated circuit designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

### Features

- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

### QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3-18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	$G_V$		-80 to + 21,5 dB
Bass control range at 40 Hz	$\Delta G_V$	typ.	± 15 dB
Treble control range at 16 kHz	$\Delta G_V$	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at $f = 20$ Hz to 20 kHz; $V_P = 12$ V; for max. voltage gain for voltage gain $G_V = -40$ dB	$V_{no(rms)}$	typ.	310 $\mu$ V
	$V_{no(rms)}$	typ.	100 $\mu$ V
Channel separation at $G_V = -20$ to + 21,5 dB	$\alpha_{cs}$	typ.	60 dB
Tracking between channels at $G_V = -20$ to + 26 dB	$\Delta G_V$	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3-18}$		7,5 to 16,5 V
Operating ambient temperature range	$T_{amb}$		-30 to + 80 °C

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1524A

# STEREO-TONE/VOLUME CONTROL CIRCUIT

## GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

### Features

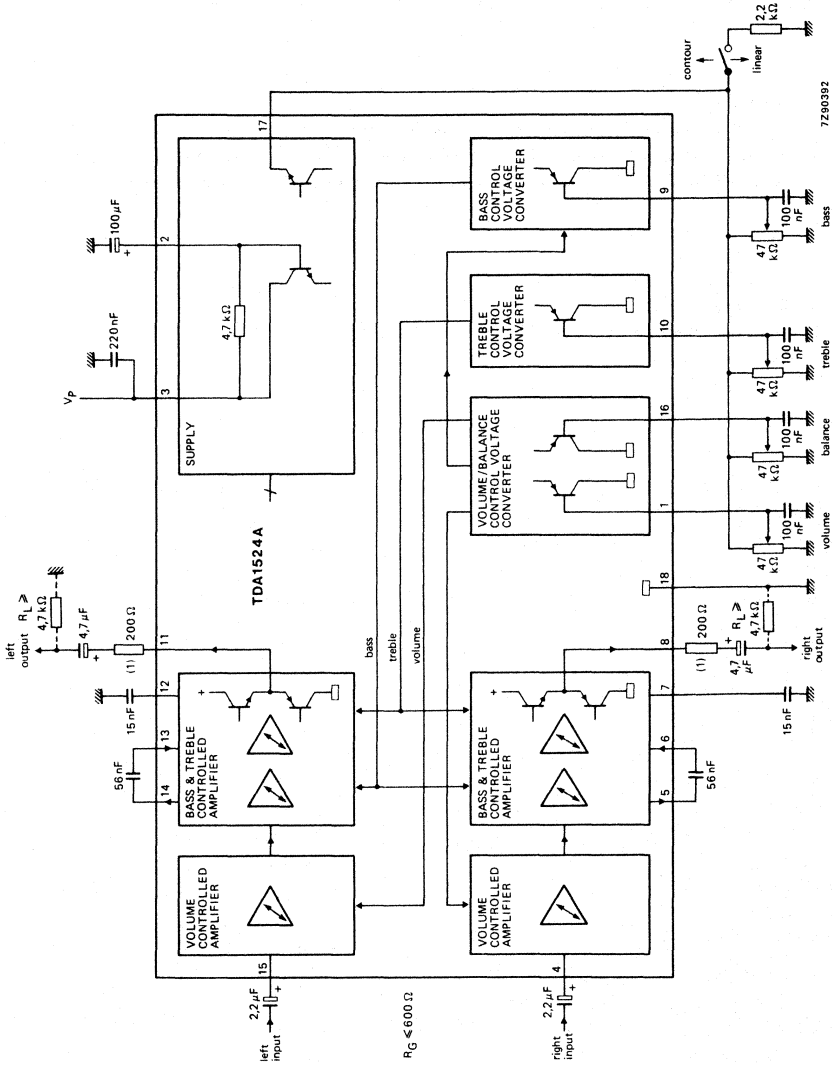
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

## QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3-18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	$G_V$		-80 to + 21,5 dB
Bass control range at 40 Hz	$\Delta G_V$	typ.	$\pm 15$ dB
Treble control range at 16 kHz	$\Delta G_V$	typ.	$\pm 15$ dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at $f = 20$ Hz to 20 kHz; $V_P = 12$ V; for max. voltage gain for voltage gain $G_V = -40$ dB	$V_{no(rms)}$ $V_{no(rms)}$	typ.	310 $\mu$ V 100 $\mu$ V
Channel separation at $G_V = -20$ to + 21,5 dB	$\alpha_{cs}$	typ.	60 dB
Tracking between channels at $G_V = -20$ to + 26 dB	$\Delta G_V$	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
<hr/>			
Supply voltage range (pin 3)	$V_P = V_{3-18}$		7,5 to 16,5 V
Operating ambient temperature range	$T_{amb}$		-30 to + 80 $^{\circ}$ C

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.



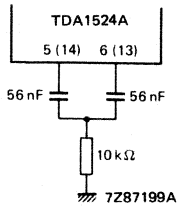


Fig. 2 Double-pole low-pass filter for improved bass-boost.

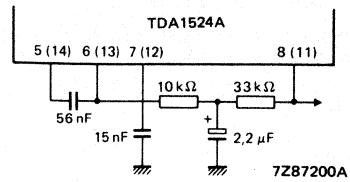


Fig. 3 D.C. feedback with filter network for improved signal handling.

### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_p = V_{3-18}$	max.	20 V
Total power dissipation	$P_{tot}$	max.	1200 mW
Storage temperature range	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature range	$T_{amb}$		-30 to + 80 °C



**D.C. CHARACTERISTICS**

$V_P = V_{3-18} = 12 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; measured in Fig. 1;  $R_G \leq 600 \text{ } \Omega$ ;  $R_L \geq 4,7 \text{ k}\Omega$ ;  $C_L \leq 200 \text{ pF}$ ;  
unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 3)</b>					
Supply voltage	$V_P = V_{3-18}$	7,5	—	16,5	V
Supply current					
at $V_P = 8,5 \text{ V}$	$I_P = I_3$	19	27	35	mA
at $V_P = 12 \text{ V}$	$I_P = I_3$	25	35	45	mA
at $V_P = 15 \text{ V}$	$I_P = I_3$	30	43	56	mA
<b>D.C. input levels (pins 4 and 15)</b>					
at $V_P = 8,5 \text{ V}$	$V_{4,15-18}$	3,8	4,25	4,7	V
at $V_P = 12 \text{ V}$	$V_{4,15-18}$	5,3	5,9	6,6	V
at $V_P = 15 \text{ V}$	$V_{4,15-18}$	6,5	7,3	8,2	V
<b>D.C. output levels (pins 8 and 11)</b> under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8,5 \text{ V}$	$V_{8,11-18}$	3,3	4,25	5,2	V
at $V_P = 12 \text{ V}$	$V_{8,11-18}$	4,6	6,0	7,4	V
at $V_P = 15 \text{ V}$	$V_{8,11-18}$	5,7	7,5	9,3	V
<b>Pin 17</b>					
Internal potentiometer supply voltage at $V_P = 8,5 \text{ V}$	$V_{17-18}$	3,5	3,75	4,0	V
Contour on/off switch (control by $I_{17}$ ) contour (switch open )	$-I_{17}$	—	—	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	—	10	mA
Application without internal potentiometer supply voltage at $V_P \geq 10,8 \text{ V}$ (contour cannot be switched off)					
Voltage range forced to pin 17	$V_{17-18}$	4,5	—	$V_P/2 - V_{BE}$	V
<b>D.C. control voltage range for volume, bass, treble and balance</b> (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5 \text{ V}$	$V_{1,9,10,16}$	1,0	—	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	—	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	—	—	5	$\mu\text{A}$

## A.C. CHARACTERISTICS

$V_p = V_{3-18} = 8,5 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position;  $R_G \leq 600 \text{ } \Omega$ ;  $R_L \geq 4,7 \text{ k}\Omega$ ;  $C_L \leq 200 \text{ pF}$ ;  $f = 1 \text{ kHz}$ ; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Control range</b>					
Max. gain of volume (Fig. 5)	$G_V \text{ max}$	20,5	21,5	23	dB
Volume control range; $G_V \text{ max}/G_V \text{ min}$	$\Delta G_V$	90	100	—	dB
Balance control range; $G_V = 0 \text{ dB}$ (Fig. 6)	$\Delta G_V$	—	-40	—	dB
Bass control range at 40 Hz (Fig. 7)	$\Delta G_V$	$\pm 12$	$\pm 15$	—	dB
Treble control range at 16 kHz (Fig. 8)	$\Delta G_V$	$\pm 12$	$\pm 15$	—	dB
Contour characteristics		see Figs 9 and 10			
<b>Signal inputs, outputs</b>					
Input resistance; pins 4 and 15 (note 1) at gain of volume control: $G_V = 20 \text{ dB}$ $G_V = -40 \text{ dB}$	$R_{i4,15}$ $R_{i4,15}$	10 —	— 160	— —	$\text{k}\Omega$ $\text{k}\Omega$
Output resistance (pins 8 and 11)	$R_{o8,11}$	—	—	300	$\Omega$
<b>Signal processing</b>					
Power supply ripple rejection at $V_{P(rms)} \leq 200 \text{ mV}$ ; $f = 100 \text{ Hz}$ ; $G_V = 0 \text{ dB}$	RR	35	50	—	dB
Channel separation (250 Hz to 10 kHz) at $G_V = -20$ to $+21,5 \text{ dB}$	$\alpha_{cs}$	46	60	—	dB
Spread of volume control with constant control voltage $V_{1-18} = 0,5 V_{17-18}$	$\Delta G_V$	—	—	$\pm 3$	dB
Gain tolerance between left and right channel $V_{16-18} = V_{1-18} = 0,5 V_{17-18}$	$\Delta G_{V,L-R}$	—	—	1,5	dB
Tracking between channels for $G_V = 21,5$ to $-26 \text{ dB}$ $f = 250 \text{ Hz}$ to $6,3 \text{ kHz}$ ; balance adjusted at $G_V = 10 \text{ dB}$	$\Delta G_V$	—	—	2,5	dB



## A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
<b>Signal handling with d.c. feedback (Fig. 3)</b>					
<b>Input signal handling</b>					
at $V_p = 8,5$ V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	—	—	V
at $V_p = 8,5$ V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	—	V
at $V_p = 12$ V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	—	—	V
at $V_p = 12$ V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	—	V
at $V_p = 15$ V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	—	—	V
at $V_p = 15$ V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	—	V
<b>Output signal handling (note 2 and note 3)</b>					
at $V_p = 8,5$ V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{O(rms)}$	1,8	2,0	—	V
at $V_p = 8,5$ V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{O(rms)}$	—	2,2	—	V
at $V_p = 12$ V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{O(rms)}$	2,5	3,0	—	V
at $V_p = 15$ V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{O(rms)}$	—	3,5	—	V
<b>Noise performance (<math>V_p = 8,5</math> V)</b>					
<b>Output noise voltage (unweighted; Fig. 15)</b>					
at f = 20 Hz to 20 kHz (r.m.s. value) for maximum voltage gain (note 4) for $G_v = -3$ dB (note 4)	$V_{no(rms)}$	—	260	—	$\mu$ V
	$V_{no(rms)}$	—	70	140	$\mu$ V
<b>Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value) for maximum voltage gain (note 4) for maximum emphasis of bass and treble (contour off; <math>G_v = -40</math> dB)</b>					
	$V_{no(m)}$	—	890	—	$\mu$ V
	$V_{no(m)}$	—	360	—	$\mu$ V
<b>Noise performance (<math>V_p = 12</math> V)</b>					
<b>Output noise voltage (unweighted; Fig. 15)</b>					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5) for maximum voltage gain (note 4) for $G_v = -16$ dB (note 4)	$V_{no(rms)}$	—	310	—	$\mu$ V
	$V_{no(rms)}$	—	100	200	$\mu$ V
<b>Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value) for maximum voltage gain (note 4) for maximum emphasis of bass and treble (contour off; <math>G_v = -40</math> dB)</b>					
	$V_{no(m)}$	—	940	—	$\mu$ V
	$V_{no(m)}$	—	400	—	$\mu$ V

parameter	symbol	min.	typ.	max.	unit
<b>Noise performance (V<sub>P</sub> = 15 V)</b>					
Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5) for maximum voltage gain (note 4) for G <sub>V</sub> = 16 dB (note 4)	V <sub>no(rms)</sub>	—	350	—	μV
	V <sub>no(rms)</sub>	—	110	220	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value) for maximum voltage gain (note 4) for maximum emphasis of bass and treble (contour off; G <sub>V</sub> = -40 dB)	V <sub>no(m)</sub>	—	980	—	μV
	V <sub>no(m)</sub>	—	420	—	μV

**Notes to characteristics**

- Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160 \text{ k}\Omega}{1 + G_V}; G_V \text{ max} = 12.$$

- Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
- In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
- Linear frequency response.
- For peak values add 4,5 dB to r.m.s. values.

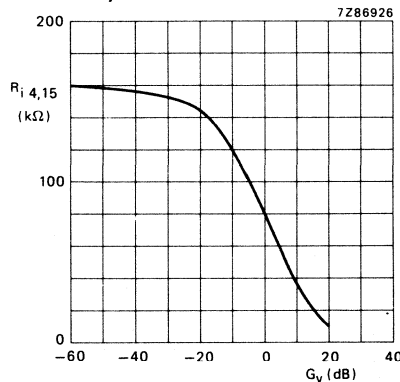


Fig. 4 Input resistance (R<sub>i</sub>) as a function of gain of volume control (G<sub>V</sub>). Measured in Fig. 1.

DEVELOPMENT SAMPLE DATA



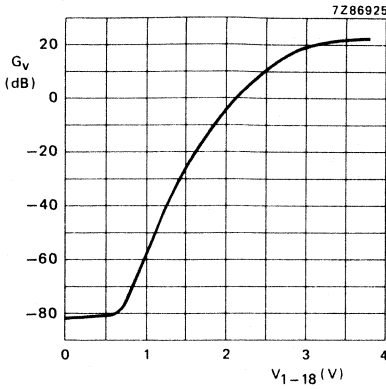


Fig. 5 Volume control curve; voltage gain ( $G_V$ ) as a function of control voltage ( $V_{1-18}$ ). Measured in Fig. 1 (internal potentiometer supply from pin 17 used);  $V_P = 8,5$  V;  $f = 1$  kHz.

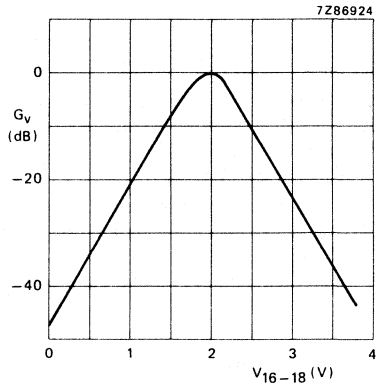


Fig. 6 Balance control curve; voltage gain ( $G_V$ ) as a function of control voltage ( $V_{16-18}$ ). Measured in Fig. 1 (internal potentiometer supply from pin 17 used);  $V_P = 8,5$  V.

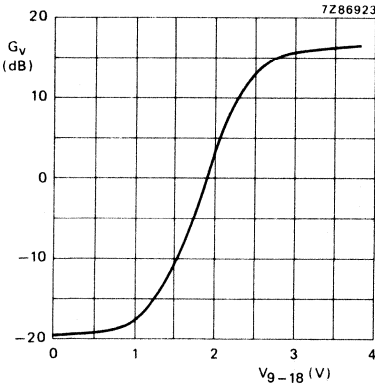


Fig. 7 Bass control curve; voltage gain ( $G_V$ ) as a function of control voltage ( $V_{9-18}$ ). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used);  $V_P = 8,5$  V;  $f = 40$  Hz.

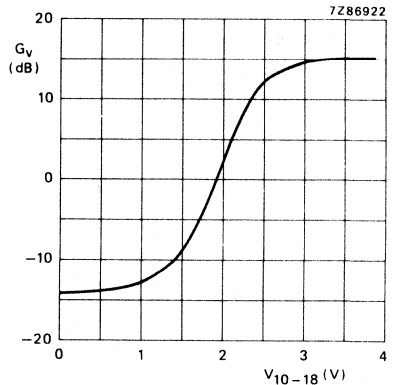


Fig. 8 Treble control curve; voltage gain ( $G_V$ ) as a function of control voltage ( $V_{10-18}$ ). Measured in Fig. 1 (internal potentiometer supply from pin 17 used);  $V_P = 8,5$  V;  $f = 16$  kHz.

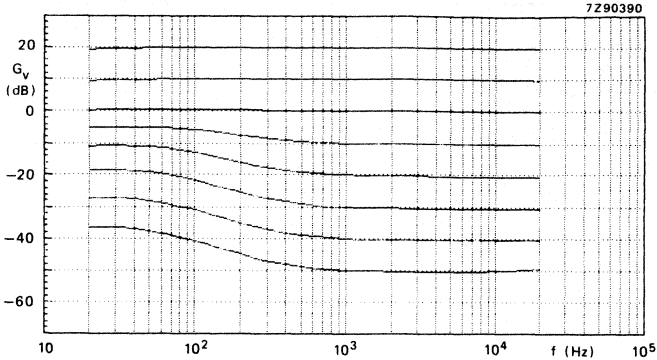


Fig. 9 Contour frequency response curves; voltage gain ( $G_v$ ) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter;  $V_p = 8,5$  V.

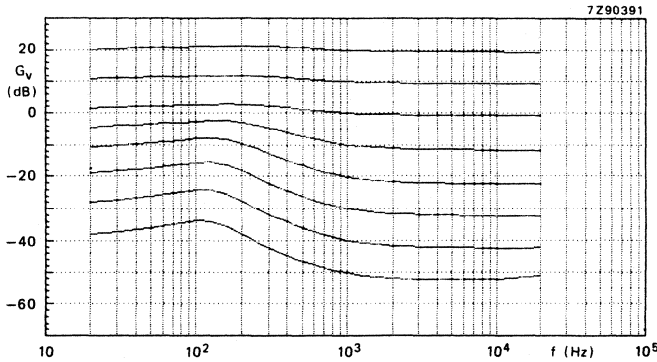


Fig. 10 Contour frequency response curves; voltage gain ( $G_v$ ) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter;  $V_p = 8,5$  V.

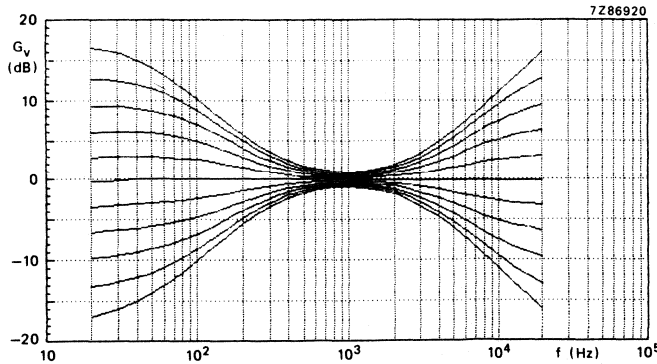


Fig. 11 Tone control frequency response curves; voltage gain ( $G_v$ ) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter;  $V_p = 8,5$  V.



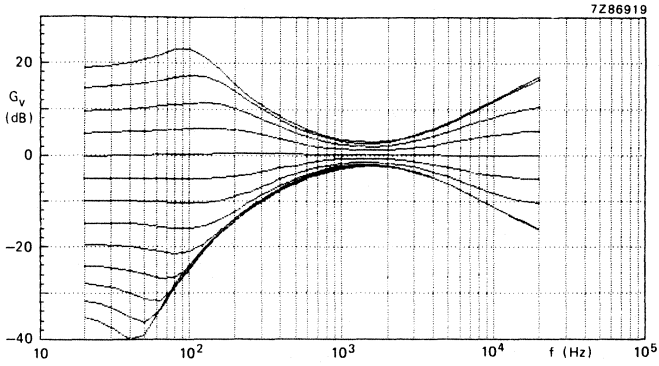


Fig. 12 Tone control frequency response curves; voltage gain ( $G_v$ ) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter;  $V_p = 8,5$  V.

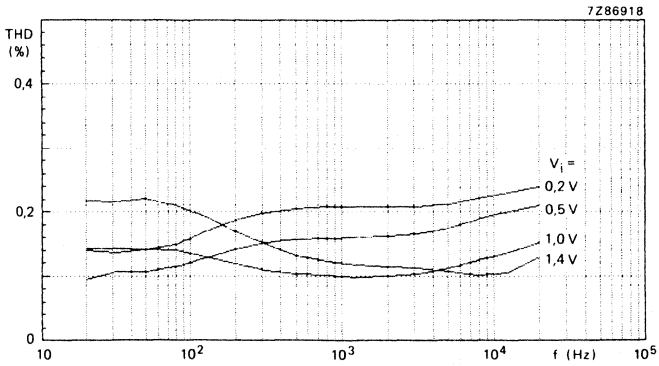


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1;  $V_p = 8,5$  V; volume control voltage gain at  $G_v = 20 \log \frac{V_o}{V_i} = 0$  dB.

$$G_v = 20 \log \frac{V_o}{V_i} = 0 \text{ dB.}$$





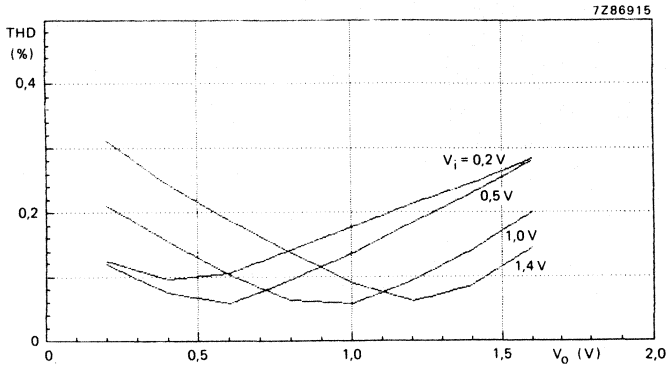
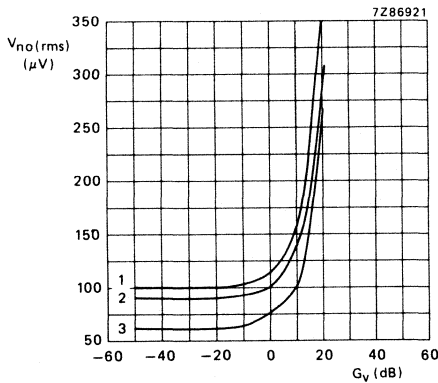


Fig. 14 Total harmonic distortion (THD); as a function of output voltage ( $V_O$ ). Measured in Fig. 1;  $V_P = 8,5$  V;  $f_i = 1$  kHz.



- (1)  $V_P = 15$  V.
- (2)  $V_P = 12$  V.
- (3)  $V_P = 8,5$  V.

Fig. 15 Noise output voltage ( $V_{no}(rms)$ ; unweighted); as a function of voltage gain ( $G_V$ ). Measured in Fig. 1;  $f = 20$  Hz to 20 kHz.



## SIGNAL-SOURCES SWITCH

The TDA1527 is a dual operational amplifier connected as an impedance converter. It incorporates the following features:

- two switchable stereo inputs, with a max. signal handling of 10 V (r.m.s.)
- input protection circuit
- input currents are independent of the switch position
- short-circuit protected outputs

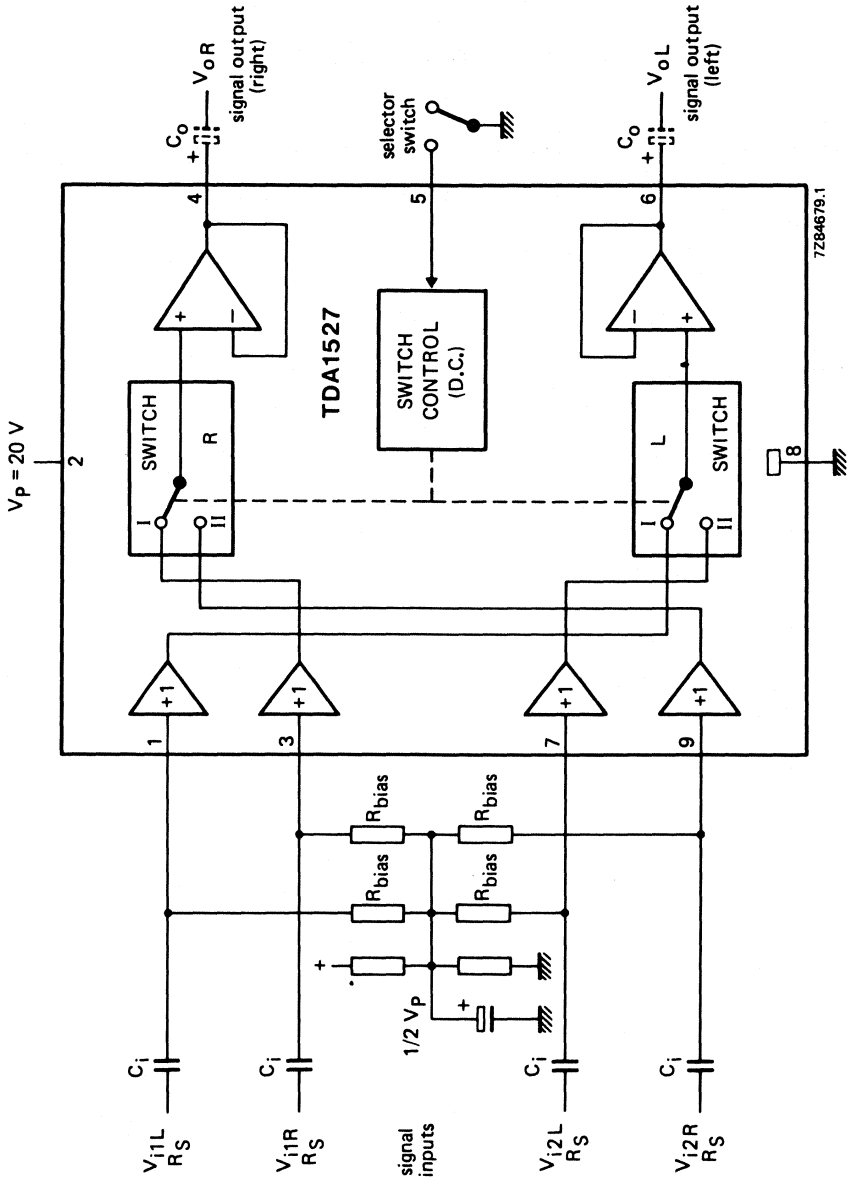
## QUICK REFERENCE DATA

Supply voltage range (pin 2)	$V_P$		4 to 20 V
Operating ambient temperature range	$T_{amb}$		-30 to +80 °C
<hr/>			
$f = 20 \text{ Hz to } 20 \text{ kHz}; R_S = 47 \text{ k}\Omega$			
Supply voltage (pin 2)	$V_P = V_{2-8}$	typ.	20 V
<hr style="border-top: 1px dashed black;"/>			
Supply current (unloaded)	$I_P$	typ.	8 mA
Input voltage range at $V_i = V_o$	$V_i$		1 to $V_P - 1$ V
Voltage gain	$G_V$	typ.	1
Total harmonic distortion	$d_{tot}$	typ.	0,01 %
Channel separation (R/L)	$\alpha$	typ.	74 dB
Crosstalk attenuation between the output and the non-selected input	$\alpha_{I-II}$	typ.	100 dB
Noise output voltage (unweighted; r.m.s. value)	$V_{n(rms)}$	typ.	6 $\mu$ V



## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).



7284679.1

Fig. 1 Block diagram/test circuit.

## PLL MOTOR SPEED CONTROL CIRCUIT FOR HI-FI APPLICATIONS

The TDA1533 is a monolithic integrated circuit intended for PLL motor speed control in several hi-fi applications; e.g. record players, cassette recorders, reel-to-reel, and operates in accordance with the phase-locked-loop (PLL) system.

The circuit incorporates the following functions:

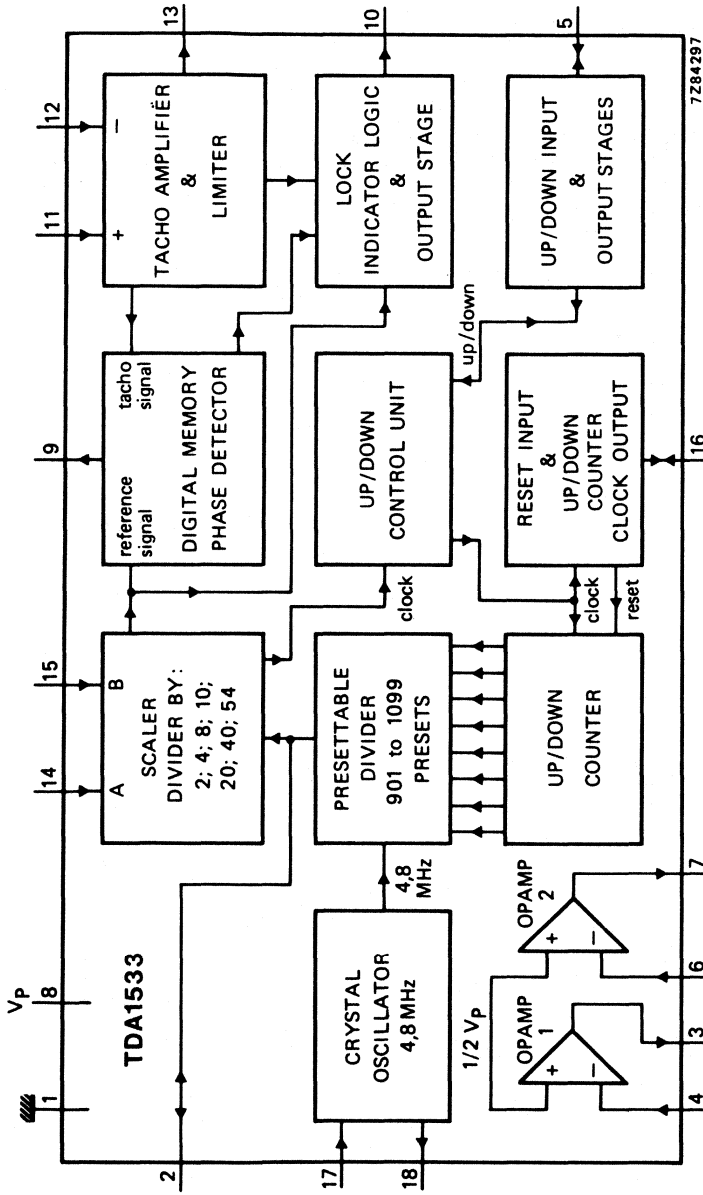
- A quartz reference oscillator
- A synthesizer for adjustment of the phase detector reference frequency
- A programmable scaler for the several applications
- A digital memory phase detector
- A tacho-signal amplifier/limiter
- Two operational amplifiers for the external integration and loop filtering of the phase detector output.

### QUICK REFERENCE DATA

Supply voltage range	$V_p$		9 to 11 V
Supply current	$I_p$	typ.	50 mA
<b>Crystal oscillator</b>			
Frequency	$f$	<	5 MHz
Temperature coefficient	TC	<	$0,1 \cdot 10^{-6} \text{ K}^{-1}$
<b>Tacho input</b>			
Input voltage	$V_I$		-0,3 to + 10 V
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	>	10 mV
<b>Operational amplifiers</b>			
Voltage gain	$G_v$	typ.	10 000
Input bias current	$I_{bias}$	<	100 nA
Input offset voltage	$V_{io}$	<	15 mV
<b>Temperatures</b>			
Storage temperature	$T_{stg}$		-25 to + 125 °C
Operating ambient temperature	$T_{amb}$		0 to + 60 °C

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).



**PINNING**

- 1. Ground
- 2. Test input/output
- 3. Output of opamp 1
- 4. Input of opamp 1
- 5. Up/down input/output
- 6. Input of opamp 2
- 7. Output of opamp 2
- 8. Positive supply (+ 10 V)
- 9. Phase detector output
- 10. Lock indicator output
- 11. + input tachometer limiter
- 12. - input tachometer limiter
- 13. Output tachometer limiter
- 14. A-input scaler control
- 15. B-input scaler control
- 16. Reset input/output
- 17. Crystal oscillator input
- 18. Crystal oscillator output

Fig. 1 Block diagram.

**GENERAL DESCRIPTION** (see also Fig. 1)

The crystal frequency (e.g. 4,8 MHz) is divided by the presettable 901 to 1099 divider. The scaler is used to obtain the reference signal for the digital memory phase detector. The tacho signal is derived from the tacho amplifier/limiter.

The output of the phase detector becomes HIGH on the positive-going edge of the reference signal, and it is floating on the first-coming positive edge of the tacho signal, if the angle between the edges is not more than 360°. The output becomes LOW if the first positive-going edge is the edge of the tacho signal, and it is floating on the first-coming positive edge of the reference signal. This means that the holding range is 720°.

The lock indication output is HIGH, except for the period between the two positive and the two negative-going edges of the tacho and reference signals.

The dividing number of the presettable divider depends on the state of its presets, thus on the position of the up/down counter.

A pull-up to the IC supply voltage of the reset input results into a reset of the up/down counter and dividing by 1000.

The up/down counter can be changed in position by means of the up/down input and the up/down control unit, and therefore the divisors of the presettable divider in a range from 901 to 1099.

The clock of the up/down counter is available at the reset input as a 0,1 V<sub>p</sub> to 0,8 V<sub>p</sub> pulse.

The timing diagram of the up/down counter is given in Fig. 2.

The up/down input and the scaler control inputs are 3-state inputs. The scaler truth table is given below. A HIGH level at the up/down input gives an increase, a LOW level a decrease, of the phase detector reference signal frequency.

The information at the up/down input will be internally forced on the state present, over a period of 250 ms. Together with the up/down clock at the reset pin, this offers the possibility of displaying the number of clock pulses used.

**SCALER TRUTH TABLE**

control inputs		division ratio
A	B	
H	H	note 1
H	L	note 2
F	F	4
F	H	8
F	L	2
H	F	54
L	H	10
L	L	20
L	F	40

H = HIGH state (the more positive voltage)  
 L = LOW state ( the less positive voltage)  
 F = floating (pin open)

**Notes**

1. Test 1; general preset.
2. Test 2; fast clock via test pin (pin 2).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p = V_{8-1}$	max.	12 V
Total power dissipation	$P_{tot}$	max.	1 W
Storage temperature	$T_{stg}$		-25 to + 125 °C
Operating ambient temperature	$T_{amb}$		-20 to + 80 °C

**CHARACTERISTICS**

Supply voltage	$V_p$	typ.	10 V 9 to 11 V
Supply current	$I_p$	typ.	50 mA
Operating ambient temperature	$T_{amb}$		0 to 60 °C

The following characteristics are measured at  $V_p = 10 V$ ;  $T_{amb} = 25 °C$ ; unless otherwise specified

**Crystal oscillator**

Frequency	$f$	typ.	4,8 MHz < 5,0 MHz
Input voltage HIGH	$V_{IH}$		2,6 to 10 V
Input voltage LOW	$V_{IL}$		-2,0 to + 2,0 V
Input resistance	$R_i$	>	50 k $\Omega$
Input capacitance	$C_i$	<	5 pF
Open voltage 1	$V_{o1}$	typ.	2 V
Open voltage 2	$V_{o2}$	typ.	1,3 V
Temperature coefficient	TC	<	0,1 · 10 <sup>-6</sup> K <sup>-1</sup>

**Lock indicator output (open collector)**

Output voltage HIGH	$V_{OH}$	<	12 V
Output voltage LOW at 10 mA	$V_{OL}$	typ.	0,25 V < 0,5 V
Output sink current	$I_o$	typ.	10 mA < 20 mA

**Phase detector output**

Output voltage HIGH at 20 $\mu A$	$V_{OH}$	>	9,5 V typ. 9,7 V
Output voltage LOW at 20 $\mu A$	$V_{OL}$	typ.	0,3 V < 0,5 V
Output current source	$I_o$	>	30 $\mu A$ typ. 44 $\mu A$
sink	$I_o$	>	30 $\mu A$ typ. 44 $\mu A$





**Tacho input**

Input voltage	$V_I$	-0,3 to + 10 V
Input biasing current	$I_{bias}$	typ. 0,5 $\mu A$ < 5,0 $\mu A$
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	> 10 mV
Offset voltage over temperature range	$V_{io}$	typ. 0,1 mV < 2,0 mV
Offset current over temperature range	$I_{io}$	typ. 50 nA < 250 nA

**Tacho output (open collector)**

Output voltage HIGH	$V_{OH}$	< 12 V
Output voltage LOW at 5 mA	$V_{OL}$	< 0,5 V
Output sink current	$I_o$	< 10 mA

**Up/down - input/output**

Input voltage LOW	$V_{IL}$	typ. 0 V -0,4 to + 0,4 V
Output voltage HIGH	$V_{OH}$	3 to 10 V
Open voltage	$V_o$	typ. 0,7 V 0,6 to 0,8 V
Output voltage HIGH at 0,5 mA	$V_{OH}$	> 8,5 V typ. 9,0 V
Output voltage LOW at 5 mA	$V_{OL}$	< 0,5 V
Output sink current	$I_o$	< 10 mA
Output source impedance	$ Z_o $	< 1,5 k $\Omega$

**Scaler inputs**

Input voltage LOW	$V_{IL}$	typ. 0 V -0,4 to + 0,4 V
Input voltage HIGH	$V_{IH}$	4 to 10 V
Open voltage	$V_o$	typ. 0,7 V 0,6 to 0,8 V

**Reset input/output**

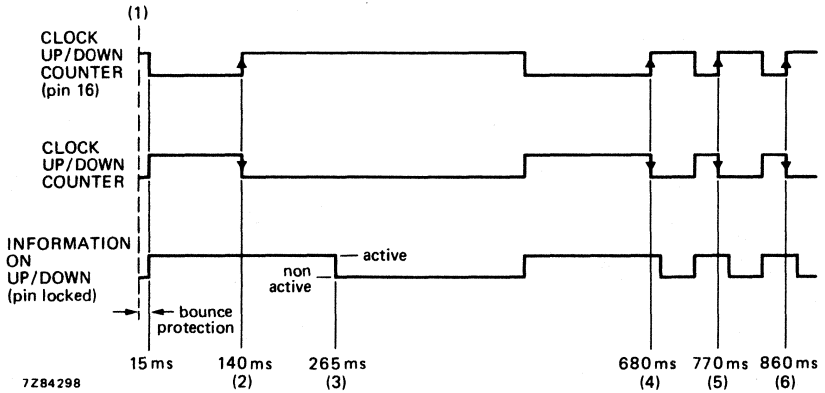
Input voltage HIGH	$V_{IH}$	> 9,5 V typ. 10,0 V
Output voltage LOW	$V_{OL}$	typ. 0,3 V < 0,5 V
Output voltage HIGH	$V_{OH}$	typ. 8 V



**CHARACTERISTICS** (continued)

**Operational amplifiers**

Voltage gain	$G_v$	typ.	10 000
Input bias current	$I_{bias}$	typ.	30 nA
		<	100 nA
Output sink current at $V_o = 1$ V	$I_o$	typ.	0,1 mA
Output source current at $V_o = 9$ V	$I_o$	>	15 mA
		typ.	20 mA
Input offset voltage	$V_{i0}$	<	15 mV
Input offset voltage drift	$\Delta V_{i0}/\Delta T$	<	0,25 mV/K
Bandwidth (3 dB)	B		60 Hz



- (1) Start operation of up/down pin.
- (2) 1st clock pulse.
- (3) From this point on, restart of cycle by second excitation is possible.
- (4) 2nd clock pulse.
- (5) 3rd clock pulse.
- (6) 4th clock pulse.

Fig. 2 Timing diagram of up/down counter.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1540D  
TDA1540P

## 14-BIT DAC WITH 85 dB S/N RATIO

### GENERAL DESCRIPTION

The TDA1540 is a monolithic integrated 14-bit digital to analogue converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85 dB in the audio band.

### QUICK REFERENCE DATA

Supply voltages			
pin 4	V <sub>P1</sub>	typ.	5 V
pin 7	V <sub>N1</sub>	typ.	-5 V
pin 11	V <sub>N2</sub>	typ.	-17 V
Signal-to-noise ratio (full scale sine-wave) at analogue output (pin 22)	S/N	typ.	85 dB
Non-linearity at T <sub>amb</sub> = -20 to +70 °C		typ.	½ LSB
Current settling time	t <sub>cs</sub>	typ.	0,5 µs
Maximum input bit rate at data input (pin 1)	BR <sub>max</sub>	min.	12 Mbit/s
Maximum clock frequency at clock input (pin 28)	f <sub>cl max</sub>	min.	12 MHz
Full scale temperature coefficient at analogue output (pin 22)	TC <sub>FS</sub>	typ.	± 30 · 10 <sup>-6</sup> K <sup>-1</sup>
Operating ambient temperature range	T <sub>amb</sub>		-20 to +70 °C
Total power dissipation	P <sub>tot</sub>	typ.	350 mW



### PACKAGE OUTLINES

TDA1540D: 28-lead DIL; ceramic (cerdip) (SOT-135A).  
TDA1540P: 28-lead DIL; plastic (SOT-117BE).

**FUNCTIONAL DESCRIPTION**

The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current  $4I$  of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an a.c. low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents  $I(\bar{I}_1)$ ,  $I(\bar{I}_2)$  and  $2I(\bar{I}_3)$  (see Fig. 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Fig. 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be  $0V \pm 10mV$ . The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Fig. 4.

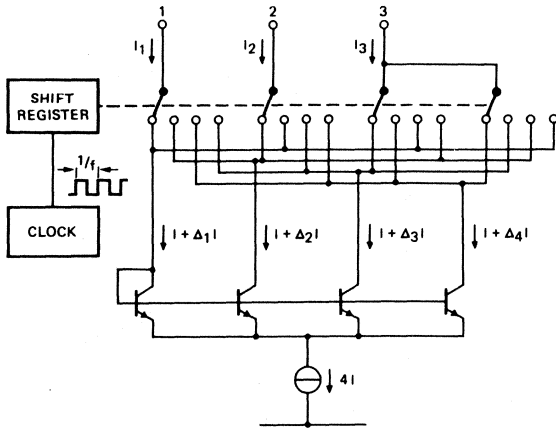


Fig. 1a Circuit diagram of one divider stage.

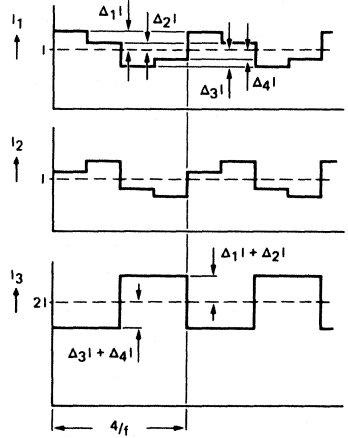


Fig. 1b Waveforms showing output currents  $I_1$ ,  $I_2$  and  $I_3$  of Fig. 1a.

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DEVELOPMENT SAMPLE DATA

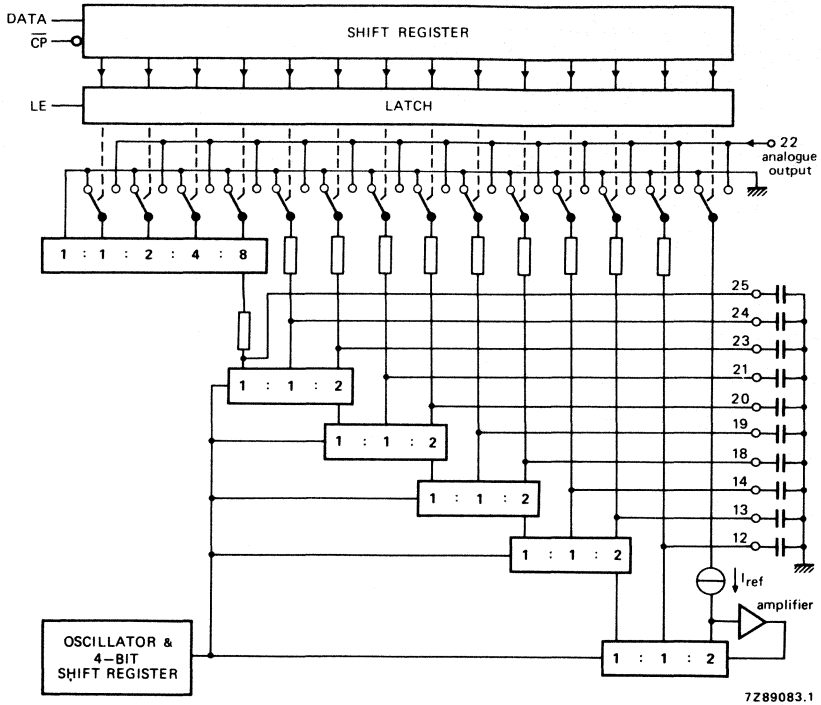


Fig. 2 Functional diagram showing cascading of current division stages.

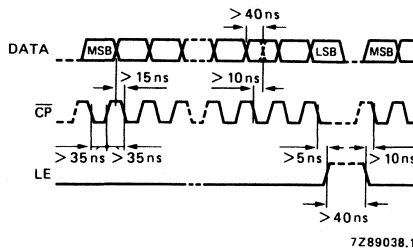


Fig. 3 Format of input signals.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages

with respect to GND (pin 6)

at pin 4

$V_{P1}$  max. 12 V

at pin 7

$V_{N1}$  max. -12 V

at pin 11

$V_{N2}$  max. -20 V

at pin 4 with respect to pin 11

$V_{P1}-V_{N2}$  max. 32 V

at pin 7 with respect to pin 11

$V_{N1}-V_{N2}$  -1 to +20 V

Total power dissipation

$P_{tot}$  max. 600 mW

Storage temperature range

$T_{stg}$  -55 to +125 °C

Operating ambient temperature range

$T_{amb}$  -25 to +80 °C

**CHARACTERISTICS** (see application circuit Fig. 4)

$T_{amb} = 25\text{ °C}$ ; at typical supply voltages; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply voltages</b>					
with respect to GND (pin 6)					
at pin 4	$V_{P1}$	3	5	7	V
at pin 7	$V_{N1}$	-4,7	-5	-7	V
at pin 11	$V_{N2}$	-16,5	-17	-18	V
<b>Supply currents</b>					
at pin 4*	$I_{P1}$	-	12	14	mA
at pin 7	$I_{N1}$	-	-20	-24	mA
at pin 11	$I_{N2}$	-	-11	-13	mA
<b>Power dissipation</b>					
Total power dissipation	$P_{tot}$	-	350	410	mW
<b>Temperature</b>					
Operating ambient temperature range	$T_{amb}$	-20	-	+70	°C

\* When the output current is  $\frac{1}{2}I_{FS}$  ( $\frac{1}{2}$  full scale output current).

parameter	symbol	min.	typ.	max.	unit
<b>Data input DATA (pin 1)</b>					
Input voltage HIGH	$V_{IH}$	2,0	—	7,0	V
Input voltage LOW	$V_{IL}$	0	—	0,8	V
Input current HIGH at $V_{IH}$	$I_{IH}$	—	—	50	$\mu$ A
Input current LOW at $V_{IL}$	$-I_{IL}$	—	—	0,2	mA
Maximum input bit rate	$BR_{max}$	12	—	—	Mbits/s
<b>Latch enable input LE (pin 2)</b>					
<b>Clock input <math>\overline{CP}</math> (pin 28)</b>					
Input voltage HIGH	$V_{IH}$	2,0	—	7,0	V
Input voltage LOW	$V_{IL}$	0	—	0,8	V
Input current HIGH at $V_{IH}$	$I_{IH}$	—	—	50	$\mu$ A
Input current LOW at $V_{IL}$	$-I_{IL}$	—	—	0,2	mA
Maximum clock frequency	$f_{CPmax}$	12	—	—	MHz
<b>Oscillator (pins 8 and 9)</b>					
Oscillator frequency at $C_{g,g} = 820$ pF	$f_{osc}$	100	160	200	kHz
<b>Analogue output <math>I_{out}</math> (pin 22)</b>					
Output voltage compliance	$V_{OC}$	-10	—	+10	mV
Full scale current	$I_{FS}$	3,8	4,0	4,2	mA
Zero scale current	$\pm I_{ZS}$	—	—	100	nA
Full scale temperature coefficient $T_{amb} = -20$ to $+70$ °C	$TC_{FS}$	—	$\pm 30 \times 10^{-6}$	—	K <sup>-1</sup>
Settling time to $\pm \frac{1}{2}$ LSB all bits on or off	$t_{cs}$	—	0,5	—	$\mu$ s
Signal-to-noise ratio*	S/N	80	85	—	dB

\* Signal-to-noise ratio within 20 Hz and 20 kHz of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

TDA1540D  
TDA1540P

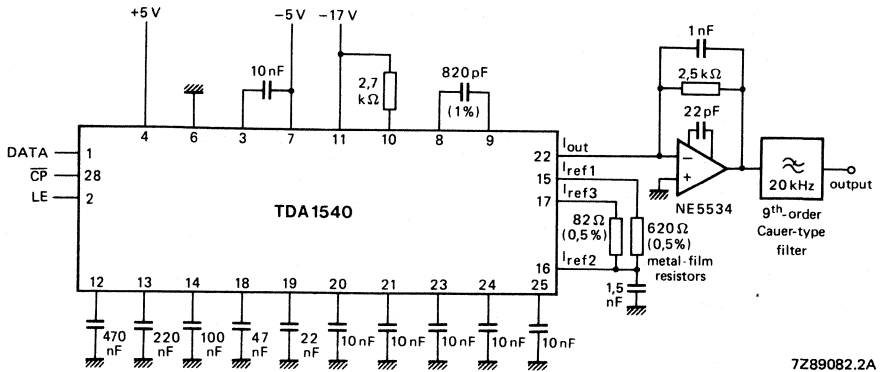


Fig. 4 Application circuit.

PINNING

- |    |                   |  |
|----|-------------------|--|
| 1  | DATA              | data input                                   |
| 2  | LE                | latch enable input                           |
| 3  | V <sub>ref1</sub> | voltage reference                            |
| 4  | V <sub>P1</sub>   | positive supply                              |
| 5  | i.c.*             | frequency compensation                       |
| 6  | GND               | on-chip operational amplifier ground         |
| 7  | V <sub>N1</sub>   | negative supply                              |
| 8  | OSC1              | } oscillator capacitor                       |
| 9  | OSC2              |  |
| 10 | V <sub>ref2</sub> | voltage reference                            |
| 11 | V <sub>N2</sub>   | negative supply                              |
| 12 | C1                | } decoupling binary weighted current sources |
| 13 | C2                |  |
| 14 | C3                |  |
| 15 | I <sub>ref1</sub> | } current reference sources                  |
| 16 | I <sub>ref2</sub> |  |
| 17 | I <sub>ref3</sub> |  |
| 18 | C4                | } decoupling binary weighted current sources |
| 19 | C5                |  |
| 20 | C6                |  |
| 21 | C7                |  |
| 22 | I <sub>out</sub>  | analogue output                              |
| 23 | C8                | decoupling binary weighted current sources   |
| 24 | C9                |  |
| 25 | C10               |  |
| 26 | i.c.*             | voltage reference                            |
| 27 | i.c.*             | voltage reference                            |
| 28 | CP                | clock pulse input                            |

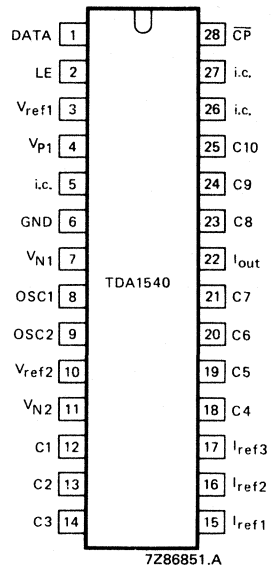


Fig. 5 Pinning diagram.

\* i.c.: internally connected.



## MOTOR SPEED REGULATOR

The TDA1559 is a 3 pins speed regulator circuit for d.c. motors. It is especially intended for low-voltage motors in battery operated cassette recorder systems and record players. The IC features a high multiplication coefficient ( $k = 21,5$ ) and a low drop-out voltage ( $0,5\text{ V}$ ). It also contains a current limiter and thermal shut-down.

## QUICK REFERENCE DATA

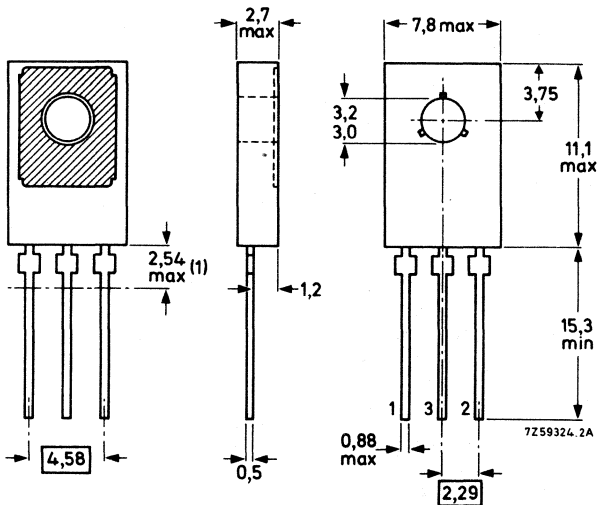
Supply voltage	$V_p$	max.	16 V
Internal reference voltage	$V_{ref}$	typ.	1,26 V
Drop-out voltage	$V_{2-3}$	typ.	0,5 V
Limited output current	$I_2\text{ lim}$	typ.	0,7 A
Multiplication coefficient	$k$	typ.	21,5
Thermal limitation	$T_j\text{ lim}$	typ.	145 °C
Operating ambient temperature range	$T_{amb}$		-25 to +70 °C

## PACKAGE OUTLINE

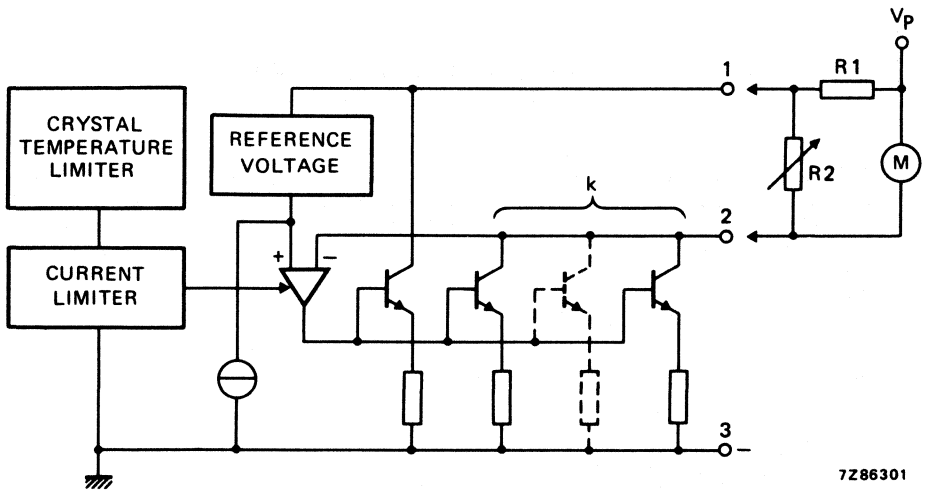
Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.



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Fig. 2 Functional diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p = V_{1-3}$ max.	16 V
Output current	$I_2$ max.	1,2 A
Storage temperature	$T_{stg}$	-25 to +125 °C
Junction temperature (limited by thermal limitation)	$T_j$ max.	130 °C
Operating ambient temperature range	$T_{amb}$	-25 to +70 °C

**THERMAL RESISTANCE**

From junction to case	$R_{thj-c}$ =	10 K/W
From junction to ambient	$R_{thj-a}$ =	100 K/W

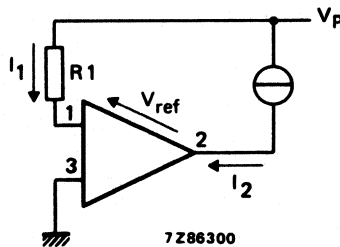


Fig. 3 Test circuit.

## CHARACTERISTICS

$V_p = 9\text{ V}$ ;  $I_2 = 70\text{ mA}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ;  $R_1 = 0$ ; heatsink with  $R_{\text{th}} = 100\text{ K/W}$  and after thermal stabilization; unless otherwise specified; see test circuit Fig. 3.

	symbol	min.	typ.	max.	unit	conditions
Internal reference voltage	$V_{\text{ref}} = V_{1.2}$	1,20	1,26	1,32	V	$V_p = 2,1\text{ V}$
Drop-out voltage	$V_{2.3}$	—	0,5	0,7	V	$I_2 = 400\text{ mA}$
	$V_{2.3}$	—	0,85	1,1	V	
Quiescent current	$I_q$	0,8	1,3	1,8	mA	
Limiting output current	$I_2\text{ lim}$	0,45	0,7	1	A	
Multiplication coefficient*	$k = \frac{\Delta I_2}{\Delta I_1}$	19,3	21,5	24,3		$\Delta I_2 = \pm 10\text{ mA}$
Thermal limitation	$T_j\text{ lim}$	130	—	160	$^\circ\text{C}$	$V_{\text{ref}} = 1,2\text{ V}$
Line regulation variation						
$V_{\text{ref}}$ versus $V_p$	$\frac{\Delta V_{\text{ref}}}{\Delta V_p}$	0	0,9	2,0	mV/V	$V_p = 2,1\text{ to }15\text{ V}$
		0	0,07	0,16	%/V	
k-spread versus $V_p$	$\frac{\Delta k}{\Delta V_p}$	-0,3	+0,2	+1	%/V	$\Delta I_2 = \pm 10\text{ mA}$ $V_p = 2,1\text{ to }15\text{ V}$
$I_q$ versus $V_p$	$\frac{\Delta I_q}{\Delta V_p}$	—	11	—	$\mu\text{A/V}$	$I_2 = 0$ $V_p = 2,1\text{ to }15\text{ V}$
		—	0,95	—	%/V	
Load regulation variation						
$V_{\text{ref}}$ versus $I_2$	$\frac{\Delta V_{\text{ref}}}{\Delta I_2}$	-0,4	0	+0,4	V/A	$I_2 = 50\text{ to }100\text{ mA}$
		-0,03	0	+0,03	%/mA	
k-spread versus $I_2$	$\frac{\Delta k}{\Delta I_2}$	-0,05	0	+0,05	%/mA	$I_2 = 50\text{ to }100\text{ mA}$ $\Delta I_2 = \pm 10\text{ mA}$
Temperature coefficient variation						
$V_{\text{ref}}$ versus $T_{\text{amb}}$	$\frac{\Delta V_{\text{ref}}}{\Delta T_{\text{amb}}}$	-0,2	0,1	+0,4	mV/K	$T_{\text{amb}} = -5\text{ to }+55\text{ }^\circ\text{C}$
		-0,02	0,01	+0,04	%/K	
k-spread versus $T_{\text{amb}}$	$\frac{\Delta k}{\Delta T_{\text{amb}}}$	-0,03	0	+0,03	%/K	$T_{\text{amb}} = -5\text{ to }+55\text{ }^\circ\text{C}$ $\Delta I_2 = \pm 10\text{ mA}$
$I_q$ versus $T_{\text{amb}}$	$\frac{\Delta I_q}{\Delta T_{\text{amb}}}$	—	-1,1	—	$\mu\text{A/K}$	$T_{\text{amb}} = -5\text{ to }+55\text{ }^\circ\text{C}$ $I_2 = 0$
		—	-0,08	—	%/K	

\* There are 4 ranges of k-factors, indicated by either '1', '2', '3', or '4' on the package. Ordering a specific range is not possible.

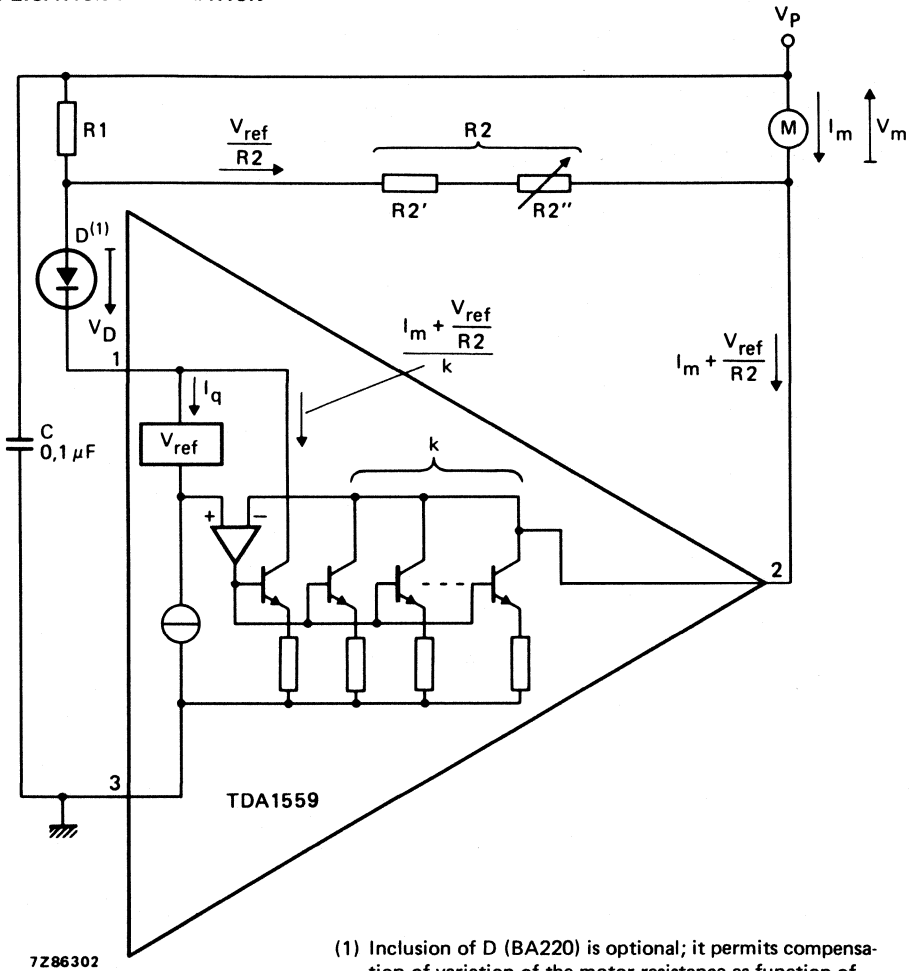
1 = 19,3 to 20,5

2 = 20,3 to 21,5

3 = 21,3 to 22,7

4 = 22,5 to 24,3

APPLICATION INFORMATION



(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 4 Example of using the TDA1559 in a d.c. motor speed regulation circuit.

Notes to Fig. 4

$$R2 = R2' + R2''$$

$$E_n = n \times C \times \phi \quad \text{where: } n = \text{speed in revolutions per minute}$$

C = motor constant

$\phi$  = magnetic flux

$E_n$  = electromotive force (e.m.f.)

T = motor torque

$R_m$  = motor resistance

$$I_m = T \times \frac{2\pi}{60} = \frac{1}{C \cdot \phi}$$

$E_n$  can be expressed as:

$$E_n = I_m \left( \frac{R1}{k} - R_m \right) + V_{ref} \left\{ 1 + \frac{R1}{R2} \left( 1 + \frac{1}{k} \right) \right\} + R2 \times I_q$$

For optimal regulation ( $dn/dT = 0$ ),  $\left( \frac{R1}{k} - R_m \right)$  should be zero.

However, if  $R1 = k \times R_m$ , the regulator will be oscillating, so for stability always  $R1 < k \times R_m$ .

$R2$  is determined by:

$$R2 = \frac{V_{ref} \times R1 \times \left( 1 + \frac{1}{k} \right)}{E_n - (R1 \times I_q) - V_{ref} - I_m \left( \frac{R1}{k} - R_m \right)}$$

Example:

$$E_n = E_{2000} = 3,58 \text{ V} \pm 11,6\%$$

$$R_m = 13 \Omega \pm 10\%$$

$$n = 2000 \text{ rev/min}$$

$$T = 1 \text{ mNm}$$

$$R1 = 220 \Omega$$

$$R2' = 82 \Omega$$

$$R2'' = 220 \Omega$$

When a diode ( $D = \text{BA220}$ ) is connected in series with pin 1, then the expressions for  $R2$  and  $E_n$  are:

$$R2 = \frac{(V_{ref} + V_D) \times R1 \times \left( 1 + \frac{1}{k} \right)}{E_n - (R1 \times I_q) - (V_{ref} + V_D) - I_m \left( \frac{R1}{k} - R_m \right)}$$

$$E_n = I_m \left( \frac{R1}{k} - R_m \right) + (V_{ref} + V_D) \left\{ 1 + \frac{R1}{R2} \left( 1 + \frac{1}{k} \right) \right\} + R2 \times I_q$$

Example:

$$E_n = E_{2000} = 3,58 \text{ V} \pm 11,6\%$$

$$R_m = 13 \Omega \pm 10\%$$

$$n = 2000 \text{ rev/min}$$

$$T = 1 \text{ mNm}$$

$$R1 = 220 \Omega$$

$$R2' = 160 \Omega$$

$$R2'' = 470 \Omega$$

$$D = \text{BA220}$$



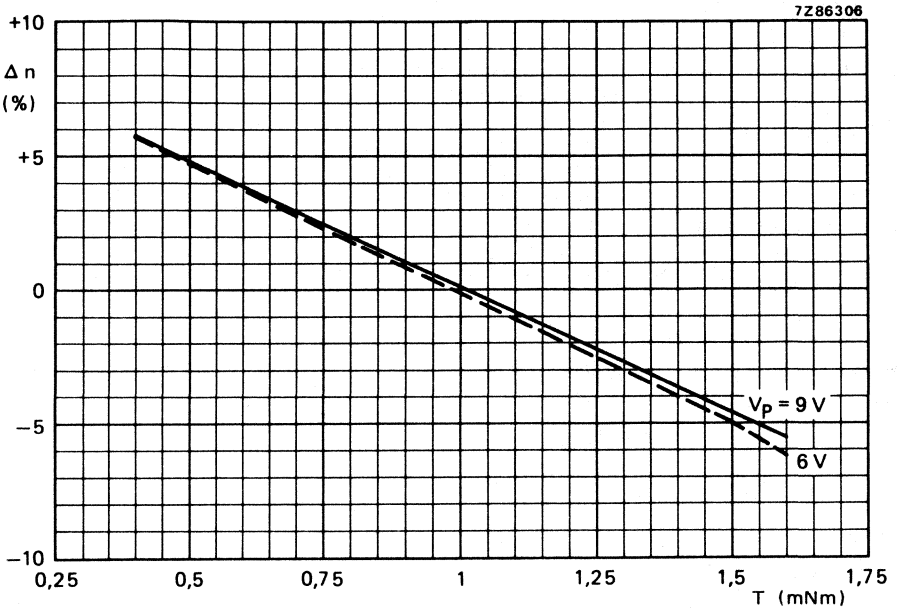


Fig. 5 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

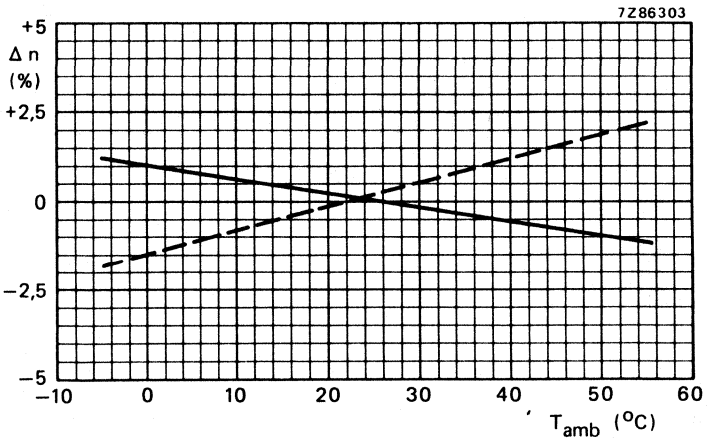


Fig. 6 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at  $T = 1\text{ mNm}$  nominal and  $V_p = 9\text{ V}$ .

—: with diode (D = BA220; see Fig. 4).  
 - - -: without diode.

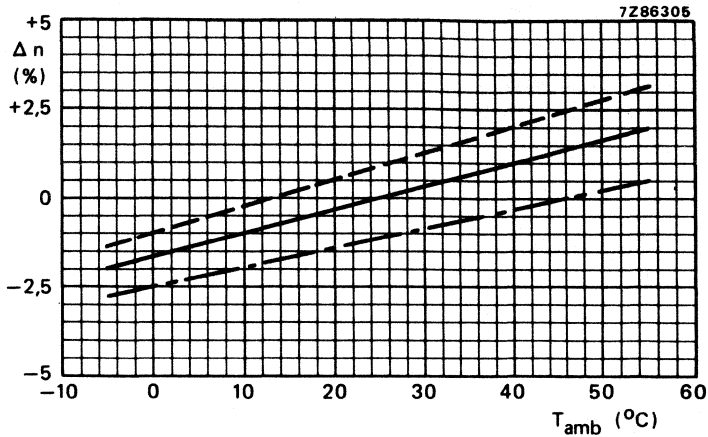


Fig. 7a V<sub>p</sub> = 6 V.

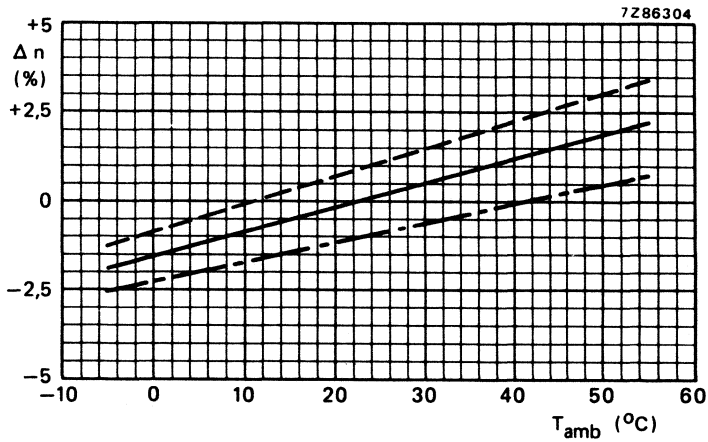


Fig. 7b V<sub>p</sub> = 9 V.

Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (D = BA220; see Fig. 4).

- : T = 0,9 mNm
- : T = 1,0 mNm
- · - · - · : T = 1,1 mNm





## BALANCED MIXER/MODULATOR/DEMODULATOR CIRCUIT

## GENERAL DESCRIPTION

The TDA1571T is a monolithic integrated circuit which, due to the universal design, can be used in various applications such as:

- Mixer
- Modulator
- Chopper
- AM synchronous demodulator
- FM quadrature detector
- Differential amplifier

## QUICK REFERENCE DATA

For application as a mixer in FM tuners;  $f_i = 98 \text{ MHz}$ ;  $f_{osc} = 108,7 \text{ MHz}$

Supply voltage (pins 12 and 13)	$V_p$	typ.	15 V
Total supply current (from $V_S$ )	$I_S$	typ.	6,5 mA
Input admittance			
at pins 2 and 7 for $f = 98 \text{ MHz}$	$Y_{11}$	typ.	$3,8 + j5 \text{ mS}$
at pins 3 and 5 for $f = 108,5 \text{ MHz}$	$Y_{11}$	typ.	$2,3 + j8 \text{ mS}$
Mixer gain	$G_{mix}$	typ.	19,5 dB
Mixer noise figure	$F_{mix}$	typ.	6,5 dB
I.F. suppression	$\alpha_{if}$	typ.	40 dB
Oscillator suppression at the input	$\alpha_{osc}$	typ.	46 dB

---

Supply voltage range (pins 12 and 13)	$V_p$	4 to 25 V
Operating ambient temperature range	$T_{amb}$	-30 to +80 °C

---

## PACKAGE OUTLINE

16-lead mini-pack; plastic (SO-16; SOT-109A).

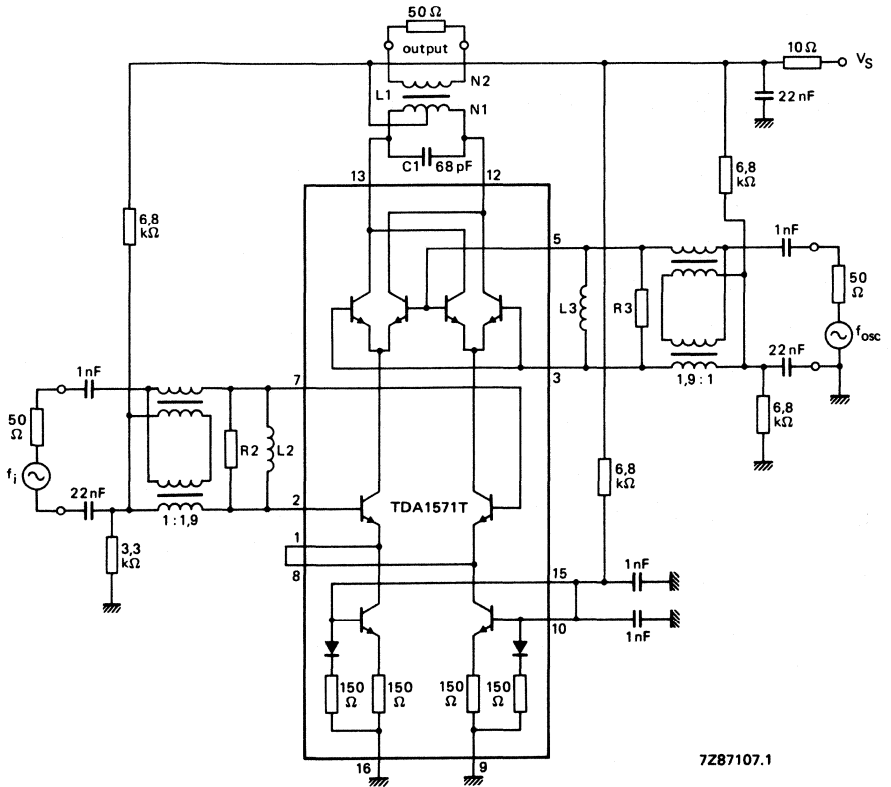


Fig. 1 Application circuit diagram of the TDA1571T used as a FM mixer; also used as test circuit for the characteristics.

Data for coil L1: N1 = 2 x 7 turns CuL (0,18 mm) on coil former  
 N2 = 1 turn CuL (0,18 mm) on coil former  
 $Q_0 = 78$

L2, R2, L3 and R3 are selected for minimum reflection  
 $r < 0,03$ ;  $R2 = R3 = 1 \text{ k}\Omega$

N.B.: Unused pins should be grounded.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages (pins 12 and 13)	$V_P = V_{12-9} = V_{13-16}$	max.	40 V
Voltage at pins 2 and 7	$V_{2-9} = V_{7-16}$	max.	18 V
Voltage at pins 3 and 5	$V_{3-2} = V_{5-7}$	max.	18 V
Voltage at pins 3 and 5	$V_{3-9} = V_{5-16}$	max.	23 V
Voltage at pins 12 and 13	$V_{12-3} = V_{13-5}$	max.	18 V
Voltage between pins 3 and 5	$\pm V_{3-5}$	max.	6 V
Voltage at pins 2 and 7	$-V_{2-1} = -V_{7-8}$	max.	6 V
Current on all pins	$I_n$	max.	10 mA
Total power dissipation	$P_{tot}$	max.	700 mW
Storage temperature range	$T_{stg}$		-55 to +150 °C
Operating ambient temperature range	$T_{amb}$		-30 to +80 °C



**CHARACTERISTICS**

$f_i = 98 \text{ MHz}$ ;  $f_{osc} = 108,7 \text{ MHz}$  with  $R_S = R_L = 50 \Omega$ ; oscillator amplitude  $P_{osc} = -14 \text{ dBm}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; measured in test circuit in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	$V_S$	—	15	—	V
Total supply current	$I_S$	—	6,5	—	mA
D.C. supply current output stage (pins 12 and 13)	$I_P$	—	2	—	mA
Input admittance at pins 2 and 7 for $f = 98 \text{ MHz}$	$y_{11}$	—	$3,8 + j5$	—	mS
at pins 3 and 5 for $f = 108,7 \text{ MHz}$	$y_{11}$	—	$2,3 + j8$	—	mS
Output admittance at pins 12 and 13 for $f = 108,7 \text{ MHz}$	$y_{22}$	—	$0,001 + j0,24$	—	mS
Conversion transconductance of mixer	$ y_{21} $	—	11	—	mS
Mixer gain	$G_{mix}$	—	19,5	—	dB
Mixer noise figure at $R_S' = 200 \Omega$	$F_{mix}$	—	6,5	—	dB
I.F. suppression at an input signal amplitude $P_i = -60 \text{ dBm}$	$\alpha_{if}$	—	40	—	dB
Oscillator suppression at the input	$\alpha_{osc i}$	—	46	—	dB
at the i.f. output	$\alpha_{osc if}$	—	38	—	dB

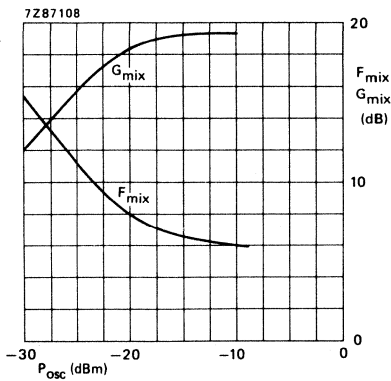


Fig. 2 Mixer gain ( $G_{mix}$ ) and mixer noise figure ( $F_{mix}$ ) at  $R_S' = 200 \Omega$  as a function of the oscillator amplitude ( $P_{osc}$ ).

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1574

# INTEGRATED FM TUNER FOR RADIO RECEIVERS

## GENERAL DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

### Features

- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

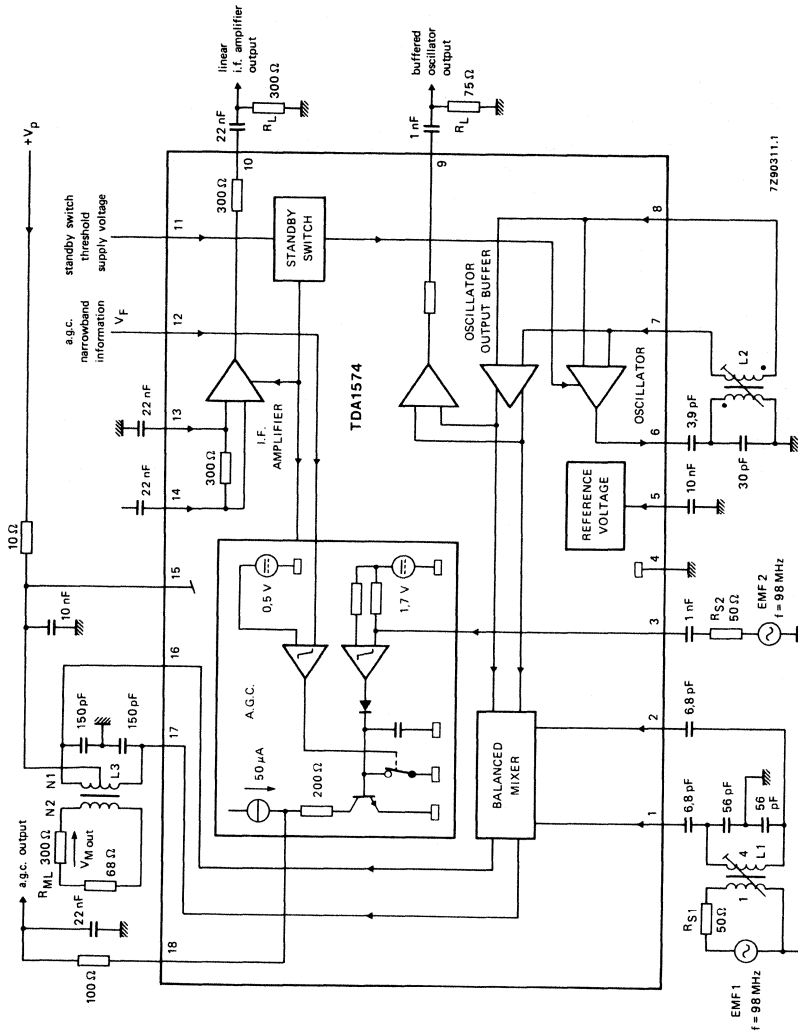
## QUICK REFERENCE DATA

Supply voltage range (pin 15)	V <sub>P</sub>		7 to 16 V
Mixer input bias voltage (pins 1 and 2)	V <sub>1, 2-4</sub>	typ.	1 V
noise figure	NF	typ.	9 dB
Oscillator output voltage (pin 6)	V <sub>6-4</sub>	typ.	2 V
output admittance at pin 6 for f = 108,7 MHz	Y <sub>22</sub>	typ.	1,5 + j2 mS
Oscillator output buffer			
D.C. output voltage (pin 9)	V <sub>9-4</sub>	typ.	6 V
Total harmonic distortion	THD	typ.	-15 dBC
Linear i.f. amplifier output voltage (pin 10)	V <sub>10-4</sub>	typ.	3,5 V
noise figure at R <sub>S</sub> = 300 Ω	NF	typ.	6,5 dB
Keyed a.g.c. output voltage range (pin 18)	V <sub>18-4</sub>		0,5 to V <sub>P</sub> -0,3 V



## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



**Coil data**

- L1: TOKO MC-108, 514HNE-150023S14; L = 0,078  $\mu$ H
- L2: TOKO MC-111, E516HNS-200057; L = 0,08  $\mu$ H
- L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

Fig. 1 Block diagram and test circuit.

**FUNCTIONAL DESCRIPTION****Mixer**

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

**Oscillator**

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

**Linear i.f. amplifier**

The i.f. amplifier is a one stage, differential input, wideband amplifier with an output buffer.

**Keyed a.g.c.**

The a.g.c. processor combines narrow- and wideband information via an r.f. level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load which sets the a.g.c. threshold.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-4}$	max.	18 V
Mixer output voltage (pins 16 and 17)	$V_{16,17-4}$	max.	35 V
Standby switch input voltage (pin 11)	$V_{11-4}$	max.	23 V
Reference voltage (pin 5)	$V_{5-4}$	max.	7 V
Total power dissipation	$P_{tot}$	max.	800 mW
Storage temperature range	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature range	$T_{amb}$		-40 to + 85 °C

**THERMAL RESISTANCE**

From junction to ambient (in free air)	$R_{th\ j-amb}$	=	80 K/W
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**Note**

All pins are short-circuit protected to ground.



## CHARACTERISTICS

$V_P = V_{15-4} = 8,5 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 15)</b>					
Supply voltage	$V_P = V_{15-4}$	7	—	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	$V_{5-4}$	4,0	4,2	4,4	V
<b>Mixer</b>					
<i>D.C. characteristics</i>					
Input bias voltage (pins 1 and 2)	$V_{1,2-4}$	—	1	—	V
Output voltage (pins 16 and 17)	$V_{16,17-4}$	4	—	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	—	4,5	—	mA
<i>A.C. characteristics (<math>f_i = 98 \text{ MHz}</math>)</i>					
Noise figure	NF	—	9	—	dB
Noise figure including transforming network	NF	—	11	—	dB
3rd order intercept point	$EMF_{1IP3}$	—	115	—	dB $\mu$ V
Conversion power gain					
$10 \log \frac{4 (V_{M(\text{out})} 10,7 \text{ MHz})^2}{(EMF_{198 \text{ MHz}})^2} \times \frac{R_{S1}}{R_{ML}}$	$G_p$	—	14	—	dB
Input resistance (pins 1 and 2)	$R_{1,2-4}$	—	12	—	$\Omega$
Output capacitance (pins 16 and 17)	$C_{16,17}$	—	13	—	pF
<b>Oscillator</b>					
<i>D.C. characteristics</i>					
Input voltage (pins 7 and 8)	$V_{7,8-4}$	—	1,3	—	V
Output voltage (pin 6)	$V_{6-4}$	—	2	—	V
<i>A.C. characteristics (<math>f_{\text{osc}} = 108,7 \text{ MHz}</math>)</i>					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 $\mu$ s	$\Delta f$	—	2,2	—	Hz



parameter	symbol	min.	typ.	max.	unit
<b>Linear i.f. amplifier</b>					
<i>D.C. characteristics</i>					
Input bias voltage (pin 13)	V <sub>13-4</sub>	—	1,2	—	V
Output voltage (pin 10)	V <sub>10-4</sub>	—	3,5	—	V
<i>A.C. characteristics (f<sub>i</sub> = 10,7 MHz)</i>					
Input impedance	R <sub>14-13</sub>	240	300	360	Ω
	C <sub>14-13</sub>	—	13	—	pF
Output impedance	R <sub>10-4</sub>	240	300	360	Ω
	C <sub>10-4</sub>	—	3	—	pF
Voltage gain					
$20 \log \sqrt{\frac{V_{10-4}}{V_{14-13}}}$	G <sub>VIF</sub>	27	30	—	dB
T <sub>amb</sub> = -40 to + 85 °C	ΔG <sub>VIF</sub>	—	0	—	dB
1 dB compression point (r.m.s. value)					
at V <sub>p</sub> = 8,5 V	V <sub>10-4rms</sub>	—	900	—	mV
at V <sub>p</sub> = 7,5 V	V <sub>10-4rms</sub>	—	500	—	mV
Noise figure					
at R <sub>S</sub> = 300 Ω	NF	—	6,5	—	dB
<b>Keyed a.g.c.</b>					
<i>D.C. characteristics</i>					
Output voltage range (pin 18)	V <sub>18-4</sub>	0,5	—	V <sub>p</sub> -0,3	V
<i>A.G.C. output current</i>					
at I <sub>3</sub> = φ or					
V <sub>12-4</sub> = 450 mV; V <sub>18-4</sub> = V <sub>p</sub> /2	-I <sub>18</sub>	25	50	100	μA
at V <sub>3-4</sub> = 2 V and					
V <sub>12-4</sub> = 1 V; V <sub>18-4</sub> = V <sub>15-4</sub>	I <sub>18</sub>	2	—	5	mA



## CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
<b>Narrowband threshold</b>					
at $V_{3-4} = 2 \text{ V}$ ; $V_{12-4} = 550 \text{ mV}$	$V_{18-4}$	—	—	1	V
at $V_{3-4} = 2 \text{ V}$ ; $V_{12-4} = 450 \text{ mV}$	$V_{18-4}$	$V_{p-0,3}$	—	—	V
<i>A.C. characteristics</i> ( $f_i = 98 \text{ MHz}$ )					
<b>Input impedance</b>					
	$R_{3-4}$	—	4	—	$k\Omega$
	$C_{3-4}$	—	3	—	pF
<b>Wideband threshold (r.m.s. value)</b> (see figures 2, 3, 4 and 5)					
at $V_{12-4} = 0,7 \text{ V}$ ; $V_{18-4} = V_p/2$ ; $I_{18} = 0$	$EMF2_{rms}$	—	19	—	mV
<b>Oscillator output buffer (pin 9)</b>					
D.C. output voltage	$V_{9-4}$	—	6,0	—	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$	$V_{9-4rms}$	—	110	—	mV
at $R_L = 75 \Omega$	$V_{9-4rms}$	25	—	—	mV
D.C. output impedance	$R_{9-15}$	—	2,5	—	$k\Omega$
<b>Signal purity</b>					
Total harmonic distortion	THD	—	-15	—	dBc
Spurious frequencies					
at $EMF1 = 1 \text{ V}$ ; $R_{S1} = 50 \Omega$	$f_S$	—	-35	—	dBc
<b>Electronic standby switch (pin 11)</b>					
Oscillator; linear i.f. amplifier; a.g.c.					
at $T_{amb} = -40 \text{ to } +85 \text{ }^\circ\text{C}$					
<b>Input switching voltage</b>					
for threshold ON; $V_{18-4} = \geq V_p - 3 \text{ V}$	$V_{11-4}$	0	—	2,3	V
for threshold OFF; $V_{18-4} = \leq 0,5 \text{ V}$	$V_{11-4}$	3,3	—	23	V
<b>Input current</b>					
at ON condition; $V_{11-4} = 0 \text{ V}$	$-I_{11}$	—	—	150	$\mu\text{A}$
at OFF condition; $V_{11-4} = 23 \text{ V}$	$I_{11}$	—	—	10	$\mu\text{A}$
<b>Input voltage</b>					
at $I_{11} = \phi$	$V_{11-4}$	—	—	4,4	V

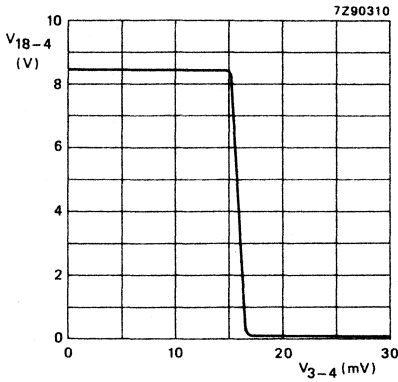


Fig. 2 Keyed a.g.c. output voltage  $V_{18-4}$  as a function of r.m.s. input voltage  $V_{3-4}$ . Measured in test circuit Fig. 1 at  $V_{12-4} = 0,7$  V;  $I_{18} = \phi$ .

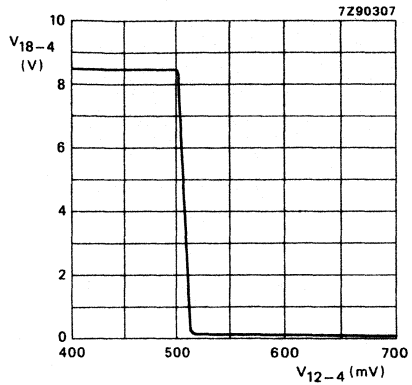


Fig. 3 Keyed a.g.c. output voltage  $V_{18-4}$  as a function of input voltage  $V_{12-4}$ . Measured in test circuit Fig. 1 at  $V_{3-4} = 2$  V;  $I_{18} = \phi$ .

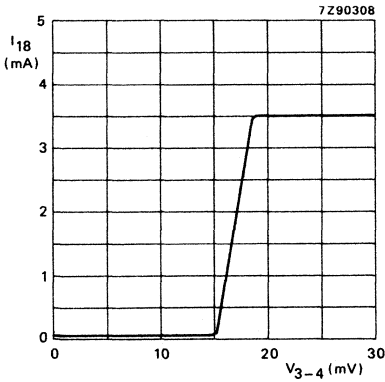


Fig. 4 Keyed a.g.c. output current  $I_{18}$  as a function of r.m.s. input voltage  $V_{3-4}$ . Measured in test circuit Fig. 1 at  $V_{12-4} = 0,7$  V;  $V_{18-4} = 8,5$  V.

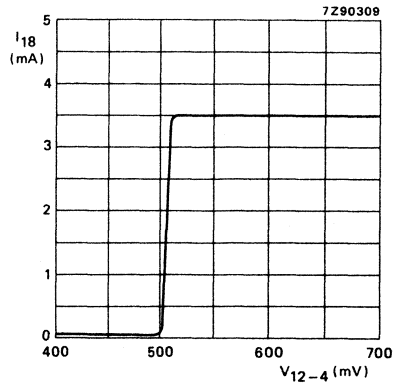
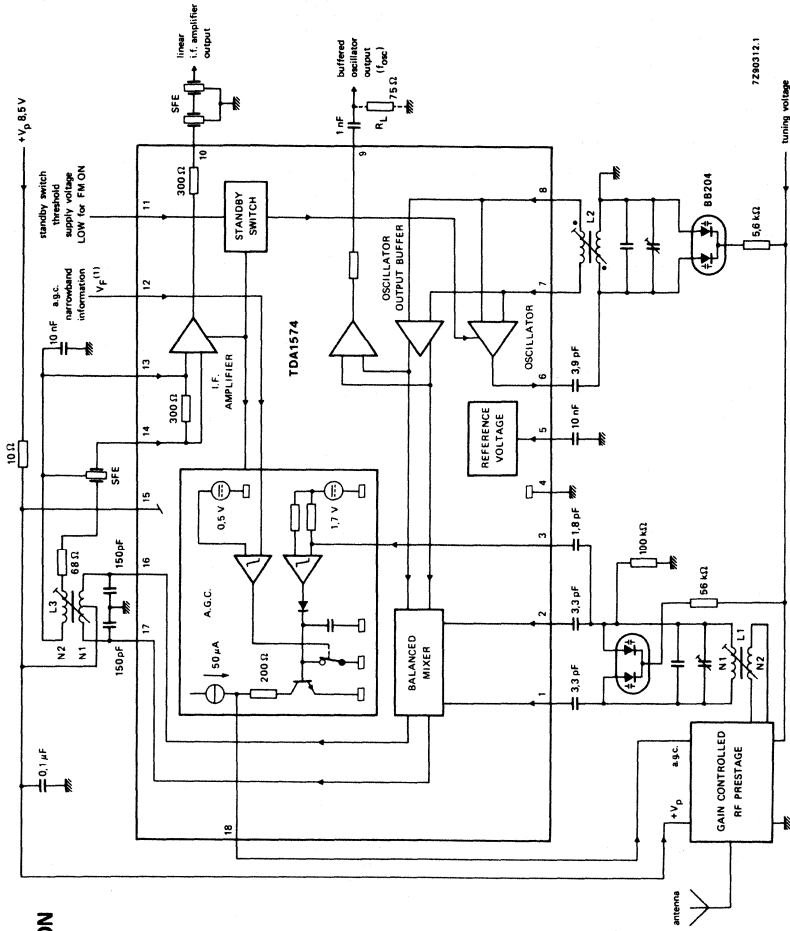


Fig. 5 Keyed a.g.c. output current  $I_{18}$  as a function of input voltage  $V_{12-4}$ . Measured in test circuit Fig. 1 at  $V_{3-4} = 2$  V;  $V_{18-4} = 8,5$  V.



APPLICATION INFORMATION



Coil data:

- L1: TOKO MC-108, N1 = 5.5 turns, N2 = 1 turn
- L2: } see Fig. 1
- L3: }

(1) Field strength indication of main i.f. amplifier.

Fig. 6 TDA1574 application diagram.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1576

## FM/IF AMPLIFIER CIRCUIT

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

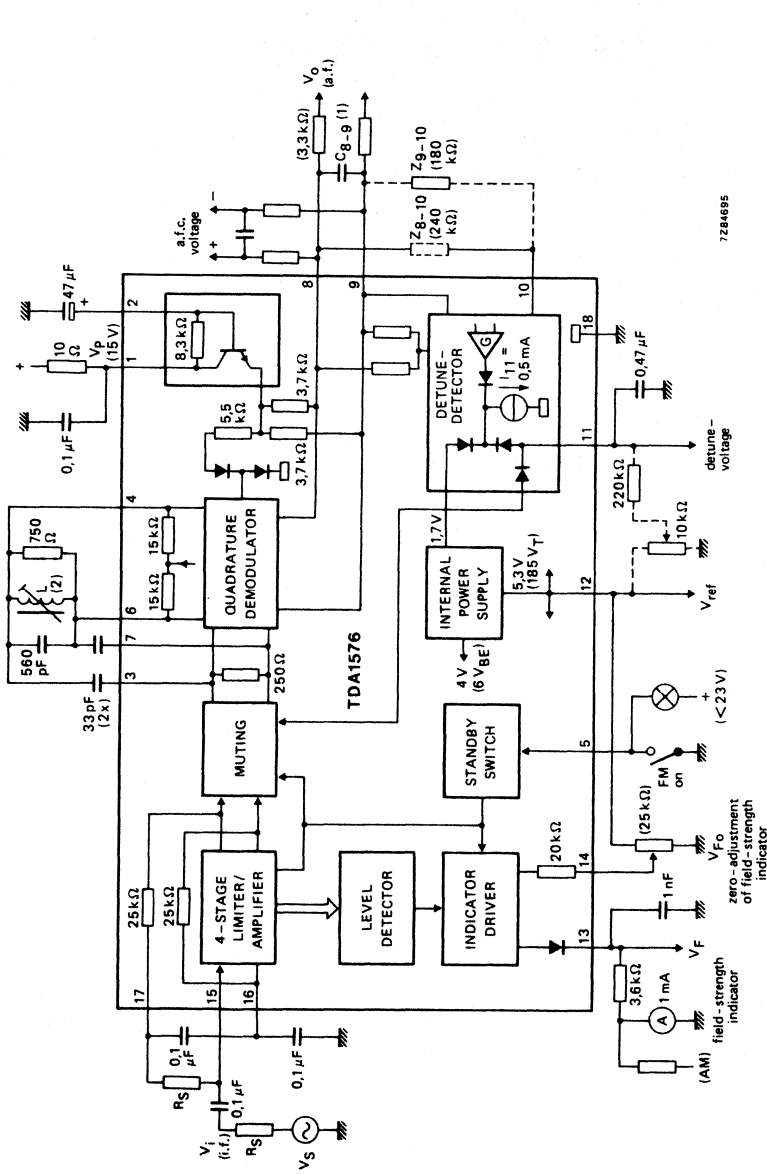
### QUICK REFERENCE DATA

$f_o = 10,7 \text{ MHz}$ ;  $\Delta f = \pm 22,5 \text{ kHz}$ ;  $f_m = 400 \text{ Hz}$ ;  $Q_L = 20$ ; de-emphasis  $\tau = 50 \mu\text{s}$

Supply voltages (pin 1)	$V_p$		8,5	15	V
Supply current	$I_p$	typ.	16	18	mA
Sensitivity at -3 dB before limiting	$V_i$	typ.	22		$\mu\text{V}$
I.F. sensitivity for					
$S + N/N = 26 \text{ dB}$	$V_i$	typ.	8		$\mu\text{V}$
$S + N/N = 46 \text{ dB}$	$V_i$	typ.	35		$\mu\text{V}$
A.F. output voltage	$V_o$	typ.	67	135	mV
Total distortion					
single tuned circuit	$d_{tot}$	typ.	0,1		%
two tuned circuits	$d_{tot}$	typ.	0,02		%
Signal plus noise-to-noise ratio; $V_i > 1 \text{ mV}$	$S + N/N$	typ.	76	80	dB
A.M. rejection	$\alpha$	typ.	50		dB
A.F.C. offset drift	$\pm \Delta f$	typ.	3	6	kHz
		<	6		kHz
Field-strength indication range	$\Delta V_i$	typ.	90		dB
Permissible indicator (load) current	$I_L$	<	2		mA
-----					
Supply voltage range (pin 1)	$V_p$		7,5 to 20		V
Ambient temperature range	$T_{amb}$		-30 to +80		$^{\circ}\text{C}$

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



(1) For de-emphasis  $\tau = 50 \mu\text{s}$ ;  $C_{8-9} = 6.8 \text{ nF}$ .  
 For stereo operation:  $C_{8-9} = 56 \text{ pF}$ .  
 (2)  $L = 0.38 \mu\text{H}$ ;  $Q_L = 70$ ;  $Q_L = 20$ ; adjusted to minimum 2nd harmonic distortion ( $d_2$ );  
 at  $V_i = 1 \text{ mV}$ ; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-18}$	max.	23 V
Voltages at pin 2	$V_{2-18}$	max.	$V_P$ V
	$-V_{2-18}$	max.	0 V
at pin 5	$V_{5-18}$	max.	23 V
	$-V_{5-18}$	max.	0 V
at pin 12	$V_{12-18}$	max.	7 V
	$-V_{12-18}$	max.	0 V
at pin 13	$V_{13-18}$	max.	6 V
	$-V_{13-18}$	max.	0 V
at pin 14	$V_{14-18}$	max.	23 V
	$-V_{14-18}$	max.	0 V
Total power dissipation	$P_{tot}$	max.	800 mW
Storage temperature range	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature range	$T_{amb}$		-30 to + 80 °C

**THERMAL RESISTANCE**

From crystal to ambient	$R_{th\ cr-a}$	=	80 K/W
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DEVELOPMENT SAMPLE DATA



## CHARACTERISTICS

$f_o = 10,7$  MHz;  $\Delta f = \pm 22,5$  kHz;  $f_m = 400$  Hz;  $R_S = 60 \Omega$ ; de-emphasis  $\tau = 50 \mu s$  ( $C_{g.9} = 6,8$  nF);  $T_{amb} = 25$  °C; measured in Fig. 1, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic ( $d_2$ ) distortion:  $V_i = 1$  mV;  $\Delta f = \pm 75$  kHz.

Supply voltage range (pin 1)

		$V_P$	
		$V_P = 8,5$ V	7,5 to 20 V $V_P = 15$ V
Supply current; without load ( $I_{12} = I_{13} = 0$ )	$I_P$	typ. 16 10 to 23	18 mA 12 to 25 mA
<b>I.F. amplifier/detector</b>			
Sensitivity at $-3$ dB before limiting	$V_i$	typ. < <	22 30 $\mu V$
I.F. sensitivity for			
S + N/N = 26 dB	$V_i$	typ.	8 $\mu V$
S + N/N = 46 dB	$V_i$	typ.	35 $\mu V$
I.F. output voltage (peak-to-peak value)			
$V_i = 1$ mV; $Z_{3.18} = Z_{7.18} = 1$ M $\Omega$ in parallel with 10 pF			
	$V_{3-7(p-p)}$	typ.	680 mV
I.F. output resistance	$R_{3-7}$	typ.	250 $\Omega$
Detector input impedance			
	$R_{4-6}$	typ.	30 k $\Omega$
	$C_{4-6}$	typ.	1 pF
Output resistance	$R_8; R_9$	typ.	3,7 k $\Omega$
D.C. output voltage			
	$V_{8-18} = V_{9-18}$	typ.	5,5 9,8 V
A.F. output voltage; $Q_L = 20$	$V_o$	typ. 67 60 to 75	135 mV 120 to 150 mV
Total distortion			
single tuned circuit; $Q_L = 20$	$d_{tot}$	typ.	0,1 %
two tuned circuits	$d_{tot}$	typ.	0,02 %
Signal plus noise-to-noise ratio			
B = 250 Hz to 15 kHz; $V_i > 1$ mV			
	S + N/N	typ.	76 80 dB
A.M. rejection; $V_i = 10$ mV			
f.m.: $f_m = 70$ Hz; $\Delta f = \pm 22,5$ kHz			
a.m.: $f_m = 1$ kHz; $m = 0,3$			
	$\alpha$	typ.	54 dB*
I.F. input voltage range; $\alpha > 40$ dB			
	$V_i$		0,5 to 500 mV
Hum suppression at $f = 100$ Hz			
$V_P = V_{1.18} = 100$ mV r.m.s.;			
$C_{2-18} = 47 \mu F$			
	$\alpha_{100}$	> typ.	43 48 dB
A.F.C. tuning slope at $Q_L = 20$			
	$\frac{\Delta V_{8-9}}{\Delta f_o}$	typ.	8,5 17 mV/kHz
A.F.C. offset voltages; $Q_L = 20$			
at $V_i = 1$ mV			
	$\pm \Delta V_{8-9}$	<	100 200 mV
at $V_i = 30 \mu V$ to 500 mV			
(reference at 1 mV and muting)			
	$\pm \Delta V_{8-9}$	typ. <	25 50 100 mV

\* Simultaneously measured.



**Field-strength indication**

Indicator sensitivity;  $I_{14} = 0$   
 Field-strength indicator voltage  
 $R_{13-18} = 3,6 \text{ k}\Omega$ ;  $I_{14} = 0$   
 $V_i = 0$

$V_i = 250 \text{ mV}$

Available output current

Reverse voltage at the output  
 for FM 'off';  $V_{5-18} > 3,5 \text{ V}$

**Detune-detector**

Quiescent input current;  $V_{10-9} = 0$

Output voltage range

Available output current

Voltage gain:  $\Delta V_{11}/\Delta(\pm V_{10-9})$   
 at  $I_{11} = 0,25 \text{ mA}$

Input offset voltage (pin 10)  
 at  $V_{11-18} = 2,5 \text{ V}$

**Reference voltage**

Output voltage;  $-I_{12} = 1 \text{ mA}$

Available output current

**Standby switch**

Required control voltage within  
 the rated ambient temperature and  
 supply voltage ranges

for FM 'on'  
 for FM 'off'

Input switching current for FM 'on'

		$V_P = 8,5 \text{ V}$	$V_P = 15 \text{ V}$	
$V_i$		20 $\mu\text{V}$ to 600 mV		
$V_F = V_{13-18}$	typ.	0		mV
	<	200		mV
$V_F = V_{13-18}$	typ.	3,6		V
		3,2 to 4,1		V
$-I_{13}$	>	2		mA
$V_{13-18}$	>	5		V
$I_{10}$	typ.	20		nA
	<	100		nA
$V_{11-18}$		1,8 to 5,0		V
$I_{11}$	typ.	0,5		mA
		0,35 to 0,65		mA
$G_V$	typ.	—		3,3
$V_{10-9}$	typ.	20		mV
$V_{\text{ref}} = V_{12-18}$	typ.	5,1		5,3 V
$-I_{12}$	typ.	2,5		mA
$V_{5 \text{ on}}$	<	2		V
$V_{5 \text{ off}}$	>	3,5		V
$-I_5$	<	100		$\mu\text{A}$

DEVELOPMENT SAMPLE DATA



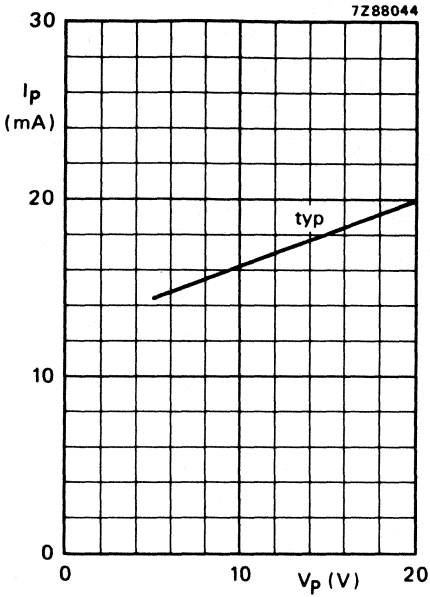


Fig. 2 Supply current consumption; without load.

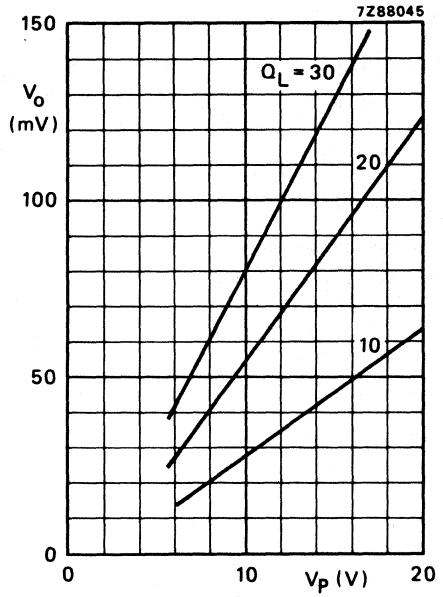


Fig. 3 A.F. output voltage;  $V_i = 1$  mV (i.f.);  $\Delta f = \pm 15$  kHz;  $f_m = 400$  Hz; typical values.

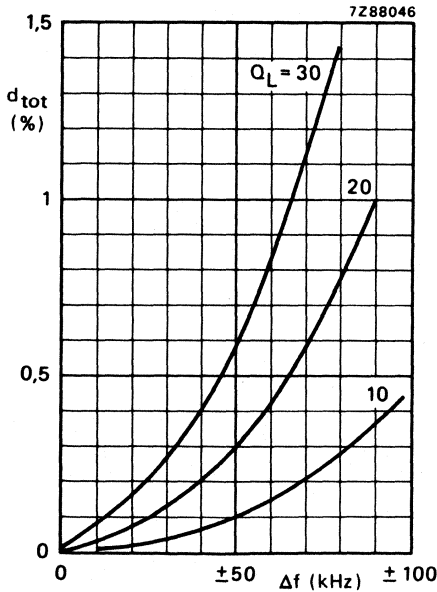


Fig. 4 Total distortion for single tuned circuit;  $V_i = 1$  mV (i.f.);  $f_m = 400$  Hz; adjusted at minimum 2nd harmonic distortion; typical values.

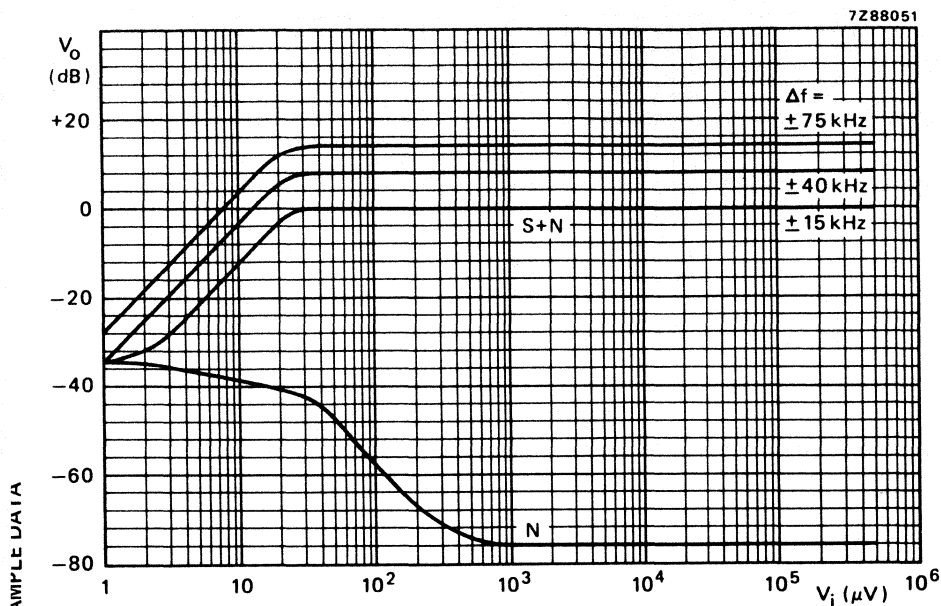


Fig. 5 A.F. output voltage level as a function of i.f. input voltage; S = signal voltage; N = noise voltage;  $V_p = 15 \text{ V}$ ;  $f_m = 400 \text{ Hz}$ ;  $B = 250 \text{ Hz to } 16 \text{ kHz}$ ;  $Q_L = 20$ ;  $C_{g.g} = 6,8 \text{ nF}$ ; typical values.

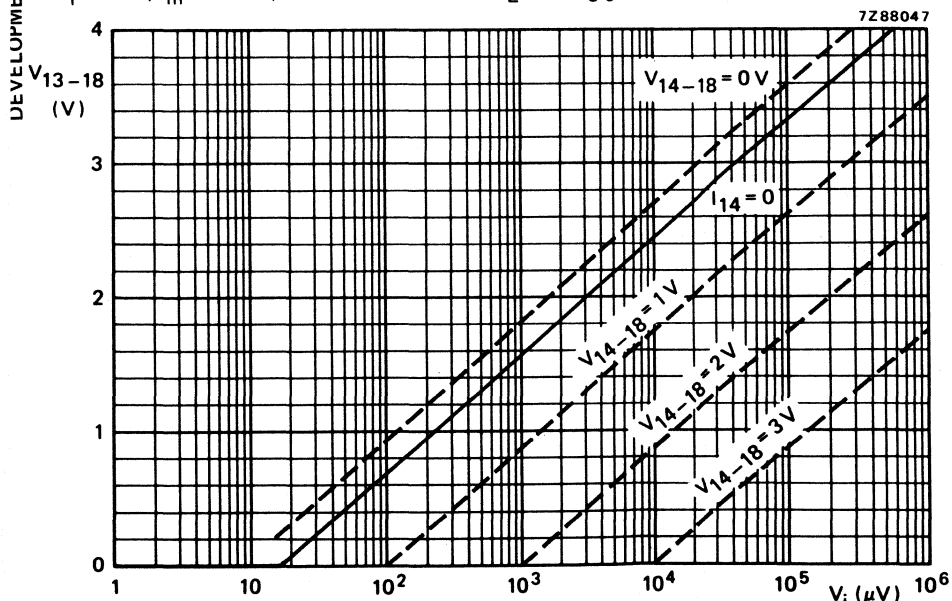


Fig. 6 Voltage at field-strength indicator output (proportional to  $V_{12-18}$ );  $R_{13-18} = 3,6 \text{ k}\Omega$ .

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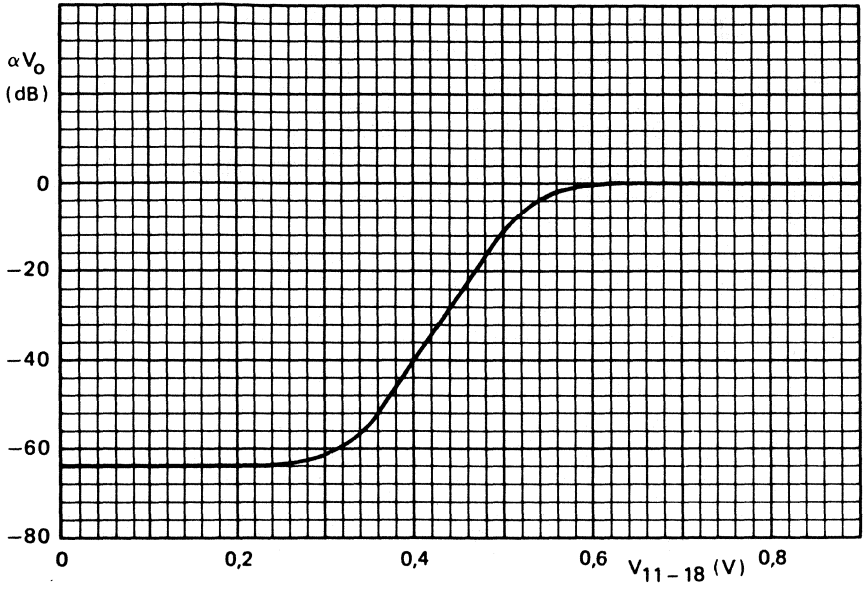


Fig. 7 Attenuation of output voltage ( $\alpha V_O$ ) as a function of the muting control voltage  $V_{11-18}$ .

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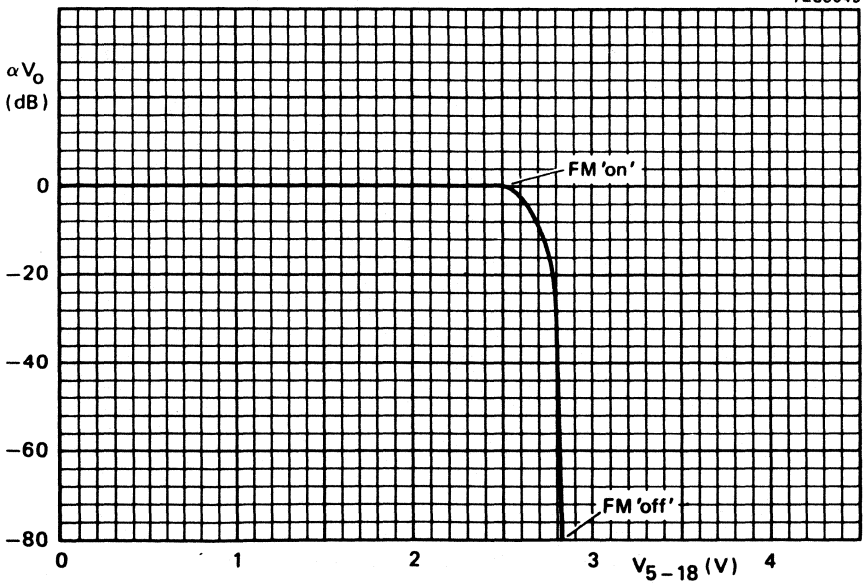
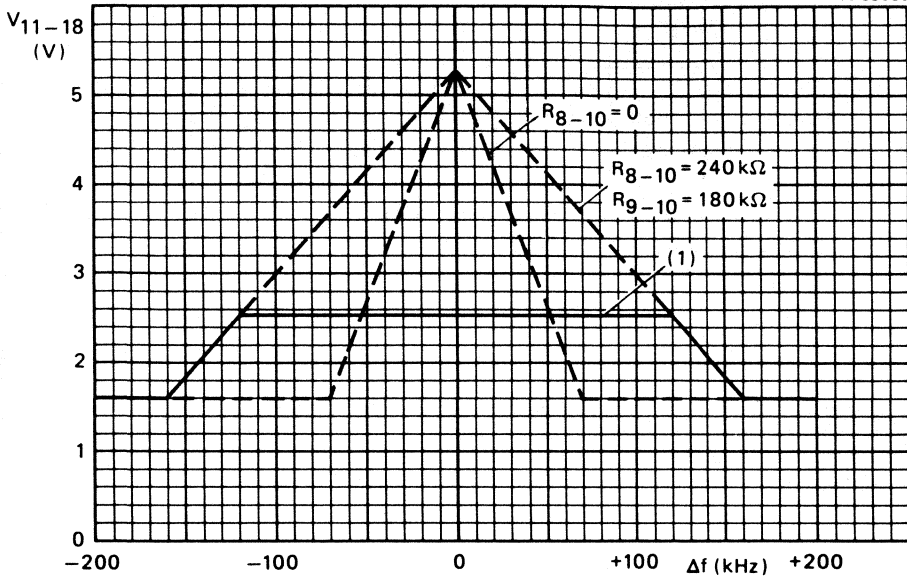


Fig. 8 FM 'on'/'off' stand-by switch; attenuation of output voltage ( $\alpha V_O$ ) as a function of control voltage  $V_{5-18}$ .

7Z88050



(1) Limited by external preset ( $\alpha \cdot V_{12-18}$ ).

Fig. 9 Detune-detector output voltage;  $V_p = 7,5$  to  $20$  V;  $Q_L = 20$ .



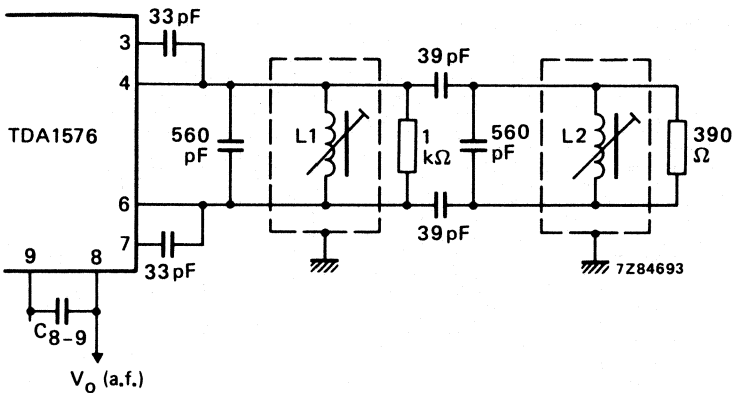


Fig. 10 Example of the TDA1576 when using a demodulator with two tuned circuits. Adjustment of the demodulator circuit is obtained with an i.f. signal which is higher than the 3 dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min.  $d_2$  distortion, and then L2 to min.  $d_2$  distortion. Coil data:  $L_1 = L_2 = 0,38 \mu\text{H}$ ;  $Q_0 = 70$ ; coil former KAN (C).

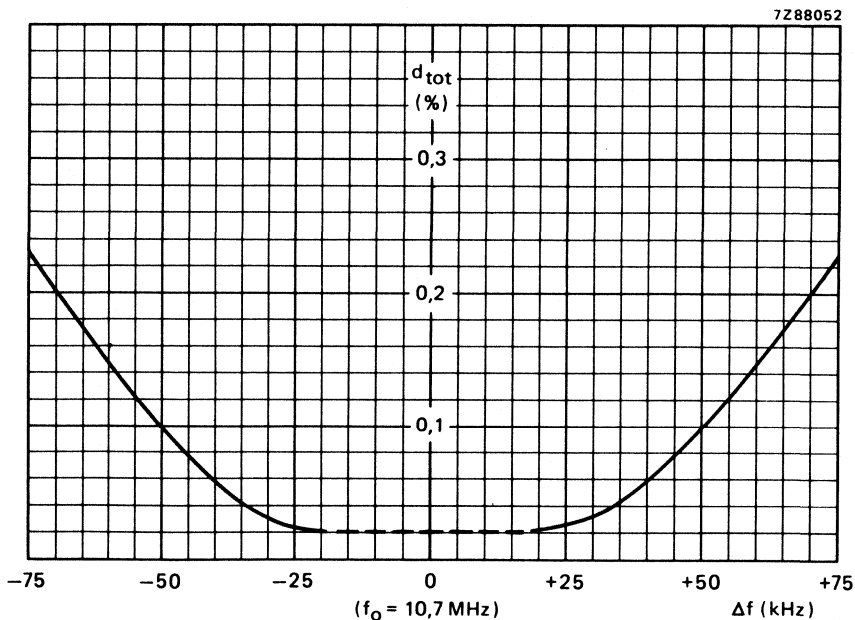
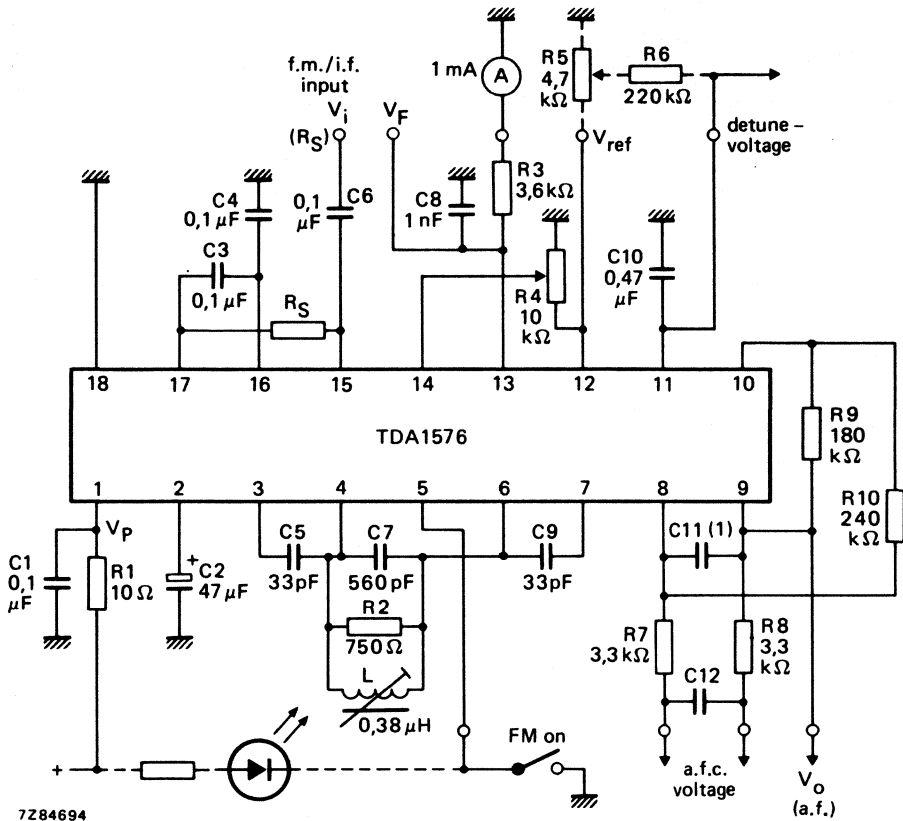


Fig. 11 Total distortion as a function of detuning;  $f_m = 400 \text{ Hz}$ ;  $C_{8-9} = 6,8 \text{ nF}$ ;  $\Delta f = \pm 75 \text{ kHz}$ ;  $V_O = 330 \text{ mV}$  for a frequency deviation  $\Delta f = \pm 75 \text{ kHz}$ .



7284694

(1) For mono:  $C_{11} = 6,8 \text{ nF}$ ; for stereo:  $C_{11} = 56 \text{ pF}$ .

Fig. 12 Application example of using TDA1576.







## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1578A

# TIME MULTIPLEX PLL STEREO DECODER

## GENERAL DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

### Features

- adjustable input and output voltage levels
- automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level
- analogue control of mono/stereo change over
- pilot indicator driver
- analogue muting control
- muting indicator driver
- oscillator with decoupled frequency measurement output
- electronic smoothing of the supply voltage

## QUICK REFERENCE DATA

Measured with a frequency deviation  $\Delta f = \pm 75$  kHz without pilot;  $f_m = 1$  kHz

Supply voltage (pin 8)	$V_P = V_{8-7}$	typ.	8,5	15	V
Supply current (pin 8)	$I_P = I_8$	typ.	21	30	mA
Multiplex input signal (adjustable)	$V_{MUX(p-p)}$	typ.	0,5	1	V
Input resistance (adjustable)	$R_i$	typ.	47		k $\Omega$
A.F. output voltage ( $R = 15$ k $\Omega$ )	$V_o$	typ.	0,75	1,5	V
Output resistance	$R_o$				low-ohmic
Spread in gain	$\Delta G_V$	$\leq$	1		dB
Channel separation	$\alpha$	typ.	50		dB
Total harmonic distortion	THD	$\leq$	0,3	0,1	%
Signal-to-noise ratio	S/N	typ.	90		dB
Carrier and harmonic suppression					
pilot signal; $f = 19$ kHz	$\alpha_{19}$	typ.	32		dB
subcarrier; $f = 38$ kHz	$\alpha_{38}$	typ.	50		dB
$f = 57$ kHz	$\alpha_{57}$	typ.	46		dB
$f = 76$ kHz	$\alpha_{76}$	typ.	60		dB
traffic radio (V.W.F.); $f = 57$ kHz	$\alpha_{57(VWF)}$	typ.	70		dB
SCA (Subsidiary Communications Authorization); $f = 67$ kHz	$\alpha_{67}$	typ.	70		dB
ACI (Adjacent Channel Interference); $f = 114$ kHz	$\alpha_{114}$	typ.	80		dB
intermodulation; $f = 10/13$ kHz	$\alpha_2, \alpha_3$	typ.	70		dB
-----					
Supply voltage range (pin 8)	$V_P = V_{8-7}$		7,5 to 18		V
Operating ambient temperature range	$T_{amb}$		-30 to +80		$^{\circ}C$

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

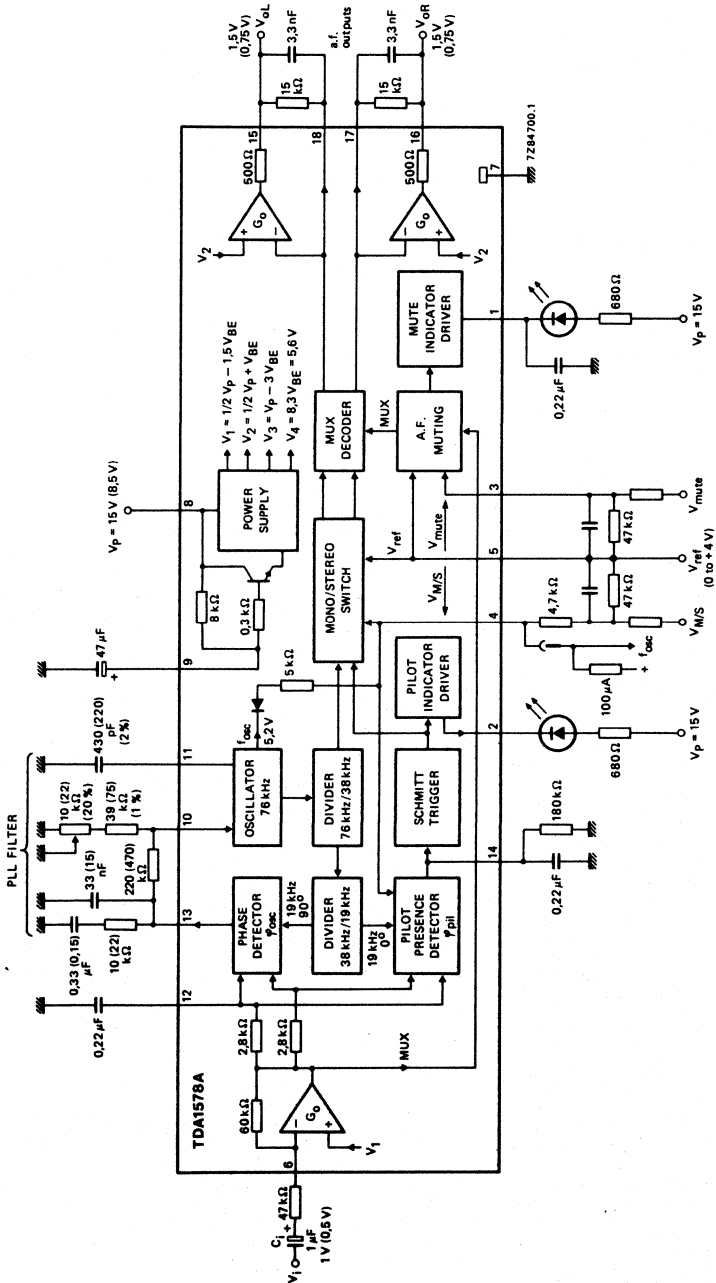


Fig. 1 Block diagram with external components; used as test circuit. Values given in parentheses are for Vp = 8.5 V.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-7}$	max.	20 V
Input voltages (pins 3, 4 and 5)	$V_{3;4;5-7}$		0 to 12 V
Indicator driver output voltage	$V_{1;2-7}$	max.	24 V
Indicator driver output current	$I_1; I_2$	max.	30 mA
Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1,2 W
Storage temperature range	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Operating ambient temperature range	$T_{amb}$		-30 to + 80 $^\circ\text{C}$

**THERMAL RESISTANCE**

From crystal to ambient	$R_{th\ c-a}$	=	80 K/W
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## CHARACTERISTICS (measured in Fig. 1)

Input signal:  $m = 100\%$  ( $\Delta f = \pm 75$  kHz); pilot signal:  $m = 9\%$  ( $\Delta f = \pm 6,75$  kHz);  
 modulation frequency: 1 kHz;  $V_{3,5} = V_{4,5} = 0$  V;  
 de-emphasizing time:  $T = 50$   $\mu$ s; oscillator adjusted to  $f_{osc}$  at a pilot voltage  $V_i = 0$  V;  
 $T_{amb} = 25$  °C; unless otherwise specified

parameter	V <sub>p</sub> (V)	symbol	min.	typ.	max.	unit
Supply voltage range (pin 8)	—	V <sub>p</sub>	7,5	—	18	V
Supply current (except output and indicator) pin 8	8,5	I <sub>p</sub>	—	21	—	mA
	15	I <sub>p</sub>	—	30	40	mA
Nominal multiplex input voltage (peak-to-peak value) R <sub>i</sub> = 47 k $\Omega$	8,5	V <sub>MUX(p-p)</sub>	—	0,5	—	V
	15	V <sub>MUX(p-p)</sub>	—	1,0	—	V
Overdrive reserve of input at THD = 1 % at THD = 0,3 %	8,5		3	6	—	dB
	15		3	6	—	dB
A.F. output voltage (r.m.s. value; mono without pilot) R <sub>15-18</sub> = R <sub>16-17</sub> = 15 k $\Omega$  R <sub>15-18</sub> = R <sub>16-17</sub> = 24 k $\Omega$	8,5	V <sub>o(rms)</sub>	—	0,75	—	V
	15	V <sub>o(rms)</sub>	—	1,5	—	V
	8,5	V <sub>o(rms)</sub>	—	1,2	—	V
	15	V <sub>o(rms)</sub>	—	2,4	—	V
Overdrive reserve of output R <sub>15-18</sub> = R <sub>16-17</sub> = 24 k $\Omega$	*		3	—	—	dB
Spread in output voltage levels	*	$\pm \Delta V_o/V_o$	—	—	1	dB
Difference of output voltage levels	*	$\pm \Delta V_{15-16}/V_o$	—	—	1	dB
Output resistance	*	R <sub>o</sub>	low-ohmic			
Available output current pins 15 and 16	*	$\pm I_o$	—	—	—	mA
Modulation range at output (unloaded)	*	V <sub>15;16-7</sub>	—	1 to V <sub>g.7-1</sub>	—	V
Internal current limiting	*	I <sub>o</sub>	—	15	—	mA
D.C. output voltage R <sub>15-18</sub> = R <sub>16-17</sub> = 24 k $\Omega$	8,5	V <sub>15;16-7</sub>	3,6	4,1	4,6	V
	15	V <sub>15;16-7</sub>	7,0	7,7	8,4	V
D.C. current (pins 17 and 18)	8,5	-I <sub>17;18</sub>	—	33	—	$\mu$ A
	15	-I <sub>17;18</sub>	—	23	—	$\mu$ A

\* V<sub>p</sub> = 8,5 or 15 V.

parameter	V <sub>p</sub> (V)	symbol	min.	typ.	max.	unit
Channel separation at V <sub>4.5</sub> = 0 V	8,5	$\alpha$	32	50	—	dB
	15	$\alpha$	39	50	—	dB
Total harmonic distortion	8,5	THD	—	0,1	0,3	%
	15	THD	—	0,04	0,1	%
Signal-to-noise ratio f = 20 Hz to 16 kHz	8,5	S/N	—	87	—	dB
	15	S/N	—	90	—	dB
Carrier and harmonic suppression at the output						
pilot signal; f = 19 kHz	*	$\alpha_{19}$	—	32	—	dB
subcarrier; f = 38 kHz	*	$\alpha_{38}$	40	50	—	dB
f = 57 kHz	*	$\alpha_{57}$	—	46	—	dB
f = 76 kHz	*	$\alpha_{76}$	—	60	—	dB
intermodulation (note 1)						
f <sub>m</sub> = 10 kHz; spurious signal f <sub>s</sub> = 1 kHz PLL-filter Fig. 1	*	$\alpha_2$	—	50	—	dB
PLL-filter Fig. 2	*	$\alpha_2$	—	70	—	dB
f <sub>m</sub> = 13 kHz; spurious signal f <sub>s</sub> = 1 kHz	*	$\alpha_3$	—	75	—	dB
traffic radio (V.W.F.); f = 57 kHz (note 2)	*	$\alpha_{57(VWF)}$	—	70	—	dB
SCA (Subsidiary Communi- cations Authorization); f = 67 kHz (note 4)	*	$\alpha_{67}$	—	70	—	dB
ACI (Adjacent Channel Interference) (note 3); f = 114 kHz	*	$\alpha_{114}$	—	80	—	dB
f = 190 kHz	*	$\alpha_{190}$	—	52	—	dB
Ripple rejection at the output; f = 100 Hz; V <sub>p(rms)</sub> = 100 mV (pin 8)	*	RR <sub>100</sub>	40	43	—	dB
Voltage on filter capacitor without external load	*	V <sub>9.7</sub>	—	V <sub>p-0,25</sub>	—	V
Source resistance	*	R <sub>9.8</sub>	6	8	10	k $\Omega$

\* V<sub>p</sub> = 8,5 or 15 V.

## CHARACTERISTICS (continued)

parameter	V <sub>p</sub> (V)	symbol	min.	typ.	max.	unit
<b>Mono/stereo control</b>						
Pilot threshold voltages (peak-to-peak values)						
for stereo 'ON'	8,5	V <sub>i(p-p)</sub>	—	21	30	mV
	15	V <sub>i(p-p)</sub>	—	43	61	mV
for mono 'ON'	8,5	V <sub>i(p-p)</sub>	6	15	—	mV
	15	V <sub>i(p-p)</sub>	12	30	—	mV
Switch hysteresis V <sub>i ON</sub> /V <sub>i OFF</sub>	*	ΔV <sub>i</sub>	—	3	—	dB
Switching time at C <sub>14-7</sub> = 0,22 μF						
for stereo 'ON'	*	t <sub>st ON</sub>	—	15	—	ms
for mono 'ON'	*	t <sub>m ON</sub>	—	27	—	ms
<b>External mono/stereo control</b> (see Fig. 12 and note 5)						
Switching voltage for external mono control						
	8,5	V <sub>14-7</sub>	—	—	0,7	V
	15	V <sub>14-7</sub>	—	—	1,4	V
	*	or: -V <sub>4-5</sub>	315	—	—	mV
Control voltage for channel separation: α = 6 dB						
	8,5	-V <sub>4-5</sub>	—	120	—	mV
	15	-V <sub>4-5</sub>	—	130	—	mV
	*	ΔV <sub>4-5</sub>	—	—	± 20	mV
α = 26 dB	8,5	-V <sub>4-5</sub>	—	70	—	mV
	15	-V <sub>4-5</sub>	—	80	—	mV
Control voltage for mono 'ON'						
	8,5	-V <sub>4-5</sub>	—	240	—	mV
	15	-V <sub>4-5</sub>	—	270	—	mV
for stereo 'ON'	8,5	-V <sub>4-5</sub>	—	220	—	mV
	15	-V <sub>4-5</sub>	—	250	—	mV
Control voltage difference for α = 6 dB; stereo 'ON'						
	8,5	ΔV <sub>4-7</sub>	80	100	120	mV

\* V<sub>p</sub> = 8,5 or 15 V.

parameter	V <sub>p</sub> (V)	symbol	min.	typ.	max.	unit
<b>Muting circuit</b> (see Fig. 13 and note 5)						
Control voltage for an attenuation: $\alpha = 3$ dB	8,5	-V <sub>3-5</sub>	-	140	-	mV
	15	-V <sub>3-5</sub>	-	145	-	mV
	*	$\Delta V_{3-5}$	-	$\pm 20$	-	mV
$\alpha = 26$ dB	8,5	-V <sub>3-5</sub>	-	255	-	mV
	15	-V <sub>3-5</sub>	-	270	-	mV
Attenuation with V <sub>3-5</sub> = 0 V with -V <sub>3-5</sub> = 450 mV	*	$\alpha$	-	-	0,2	dB
	*	$\alpha$	-	80	-	dB
LED driver output current at an attenuation: $\alpha = 3$ dB	*	I <sub>1</sub>	1,2	1,7	2,2	mA
Control voltage for I <sub>1</sub> = 200 $\mu$ A	8,5	-V <sub>3-5</sub>	-	150	-	mV
	15	-V <sub>3-5</sub>	-	160	-	mV
<b>Control inputs</b>						
Recommended voltage range	*	V <sub>3;4;5-7</sub>	0	-	4	V
Input bias current	*	I <sub>3;4;5</sub>	-	10	100	nA
<b>Indicator driver</b>						
Output saturation voltages at I <sub>1</sub> = 20 mA; V <sub>3-5</sub> = 0 V at I <sub>2</sub> = 20 mA	*	V <sub>1-7sat</sub>	-	1,2	1,8	V
	*	V <sub>2-7sat</sub>	-	0,5	1,0	V
Output leakage current at V <sub>1;2-7</sub> = 24 V	*	I <sub>1;2</sub>	-	20	-	$\mu$ A

\* V<sub>p</sub> = 8,5 or 15 V.

## CHARACTERISTICS (continued)

parameter	V <sub>p</sub> (V)	symbol	min.	typ.	max.	unit
<b>VCO</b>						
Oscillator frequency adjustable with R <sub>10-7</sub>	*	f <sub>osc</sub>	—	76	—	kHz
Spread of free-running frequency at nominal external circuitry	*	f <sub>osc</sub>	71	—	82	kHz
Free-running frequency dependency (note 6) with temperature	*	TC	—	1 × 10 <sup>-4</sup>	—	K <sup>-1</sup>
with supply voltage	*	Δf <sub>osc</sub> /ΔV <sub>p</sub>	—	—	400	Hz/V
Capture and holding range for a pilot input voltage V <sub>pil</sub> = 0,5 × V <sub>pil nom</sub>	*	Δf/f	± 2	—	—	%
PLL control slope (total)	*	S <sub>tot</sub>	—	4,5	—	kHz/μs
D.C. voltage at pin 10	*	V <sub>10-7</sub>	—	2,1	—	V
		or:	—	3,2 V <sub>BE</sub>	—	V
Frequency measuring point; internal switching threshold	*	V <sub>4-7</sub>	—	6	—	V
		or:	—	9 V <sub>BE</sub>	—	V
Output voltage (peak-to-peak value) at pin 4; R = 4,7 kΩ	*	V <sub>4-7(p-p)</sub>	—	350	—	mV
Output resistance	*	R <sub>4-7</sub>	—	5	—	kΩ

\* V<sub>p</sub> = 8,5 or 15 V.



**Notes to the characteristics****1. Intermodulation suppression (BFC: Beat-Frequency Components)**

$$\alpha_2 = \frac{V_{O(\text{signal})} \text{ (at 1 kHz)}}{V_{O(\text{spurious})} \text{ (at 1 kHz)}}; f_s = (2 \times 10 \text{ kHz}) - 19 \text{ kHz}$$

$$\alpha_3 = \frac{V_{O(\text{signal})} \text{ (at 1 kHz)}}{V_{O(\text{spurious})} \text{ (at 1 kHz)}}; f_s = (3 \times 13 \text{ kHz}) - 38 \text{ kHz}$$

measured with: 91% mono signal;  $f_m = 10$  or  $13$  kHz; 9% pilot signal.

**2. Traffic radio (V.W.F.) suppression**

$$\alpha_{57(\text{VWF})} = \frac{V_{O(\text{signal})} \text{ (at 1 kHz)}}{V_{O(\text{spurious})} \text{ (at 1 kHz} \pm 23 \text{ kHz)}}$$

measured with: 91% stereo signal;  $f_m = 1$  kHz; 9% pilot signal;  
5% traffic subcarrier ( $f = 57$  Hz,  $f_m = 23$  Hz AM,  $m = 60\%$ ).

**3. ACI (Adjacent Channel Interference)**

$$\alpha_{114} = \frac{V_{O(\text{signal})} \text{ (at 1 kHz)}}{V_{O(\text{spurious})} \text{ (at 4 kHz)}}; f_s = 110 \text{ kHz} - (3 \times 38 \text{ kHz})$$

$$\alpha_{190} = \frac{V_{O(\text{signal})} \text{ (at 1 kHz)}}{V_{O(\text{spurious})} \text{ (at 4 kHz)}}; f_s = 186 \text{ kHz} - (5 \times 38 \text{ kHz})$$

measured with: 90% mono signal;  $f_m = 1$  kHz; 9% pilot signal;  
1% spurious signal ( $f_s = 110$  or  $186$  kHz, unmodulated).

**4. SCA (Subsidiary Communications Authorization)**

$$\alpha_{67} = \frac{V_{O(\text{signal})} \text{ (at 1 kHz)}}{V_{O(\text{spurious})} \text{ (at 9 kHz)}}; f_s = (2 \times 38 \text{ kHz}) - 67 \text{ kHz}$$

measured with: 81% mono signal;  $f_m = 1$  kHz; 9% pilot signal;  
10% SCA-subcarrier ( $f_s = 67$  kHz, unmodulated).

$$5. \text{ Assuming } V_T = \frac{k \times T}{q} = 28,6 \text{ mV at } T_j = 330 \text{ K.}$$

6. The effects of external components are not taken into account.



**APPLICATION NOTES**

1. When mono/stereo control and muting control are not used, pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
  - a. A capacitor at pin 12 ( $C_{12-7}$ ): phasing 19/38 kHz
  - b. RC or LCR filter at the input: frequency response compensation ( $V_G = f(\omega)$ )
  - c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation ( $\alpha_2$ ); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

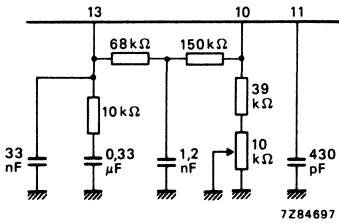


Fig. 2 PLL-filter for  $\alpha_2 = 70$  dB at  $V_p = 15$  V (see also Fig. 1).

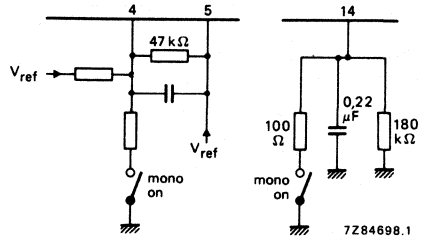


Fig. 3 (a) At pin 4;  $-V_{4.5} > 300$  mV; (b) at pin 14.

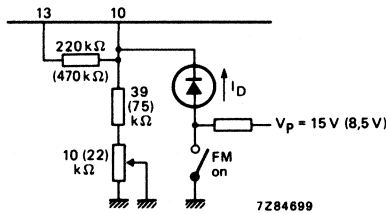


Fig. 4 The oscillator is switched-off when:  $I_D > 100 \mu A$  ( $> 50 \mu A$  for  $V_p = 8,5$  V) and  $I_D < 1$  mA.

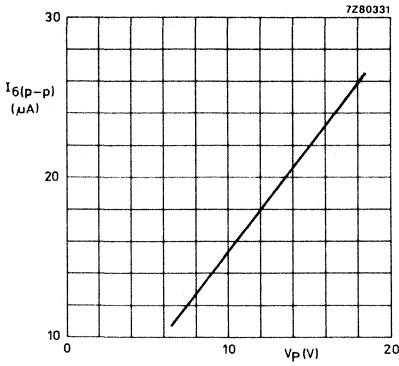


Fig. 5 Signal handling range at the input for  $I_{6nom} (\pm 75 \text{ kHz})$ ;  $V_{9.7} = V_p$ .

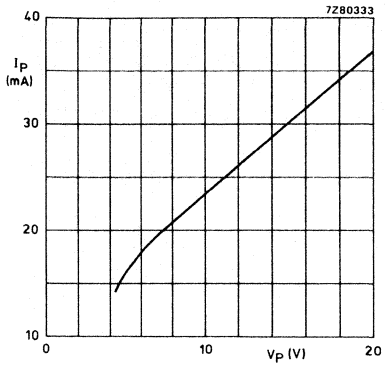


Fig. 6 Supply current consumption at  $V_{9.7} = V_p$ .

DEVELOPMENT SAMPLE DATA

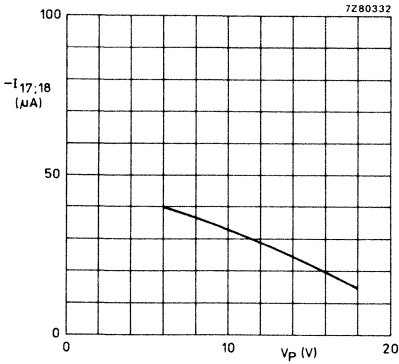


Fig. 7 D.C. current in the feedback loop of the output amplifier.

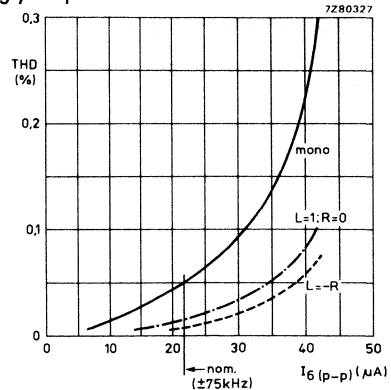


Fig. 8 Total harmonic distortion (THD) as a function of the peak-to-peak input current at pin 6;  $V_p = 15 \text{ V}$ ;  $f_m = 1 \text{ kHz}$ ;  $V_{3.5} = V_{4.5} = 0 \text{ V}$ .

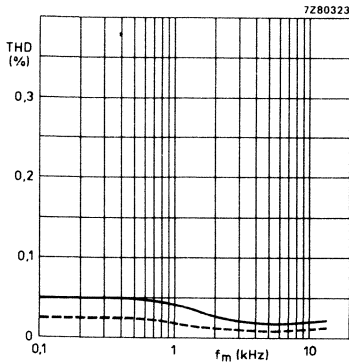


Fig. 9 Total harmonic distortion (THD) as a function of the modulation frequency ( $f_m$ );  $V_p = 15 \text{ V}$ ;  $I_{6(p-p)} = 21,5 \mu\text{A}$ .

— mono  
 - - - stereo;  $L = -R$ ; 91% + 9% pilot signal.



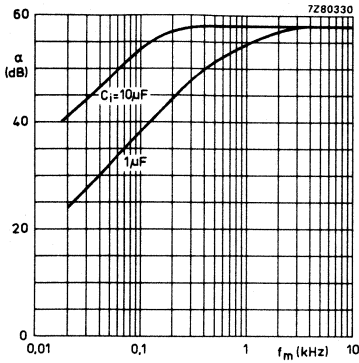


Fig. 10 Channel separation ( $\alpha$ ) as a function of the modulation frequency ( $f_m$ );  $V_P = 15 V$ ;  $R_i = 47 k\Omega$ ;  $V_{4.5} = 0 V$ .

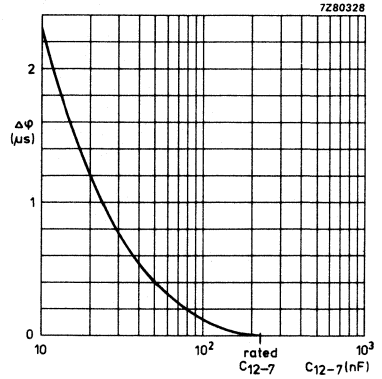


Fig. 11 Phase shift between pilot signal at the input and the internal carrier processing as a function of  $C_{12-7}$ .

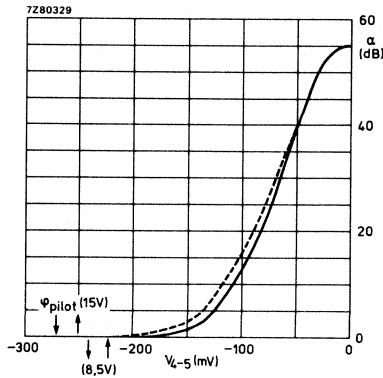


Fig. 12 Mono/stereo control at  $f_m = 1 kHz$ ;  $\alpha$  is the channel separation.  
 —  $V_P = 8,5 V$   
 - - -  $V_P = 15 V$

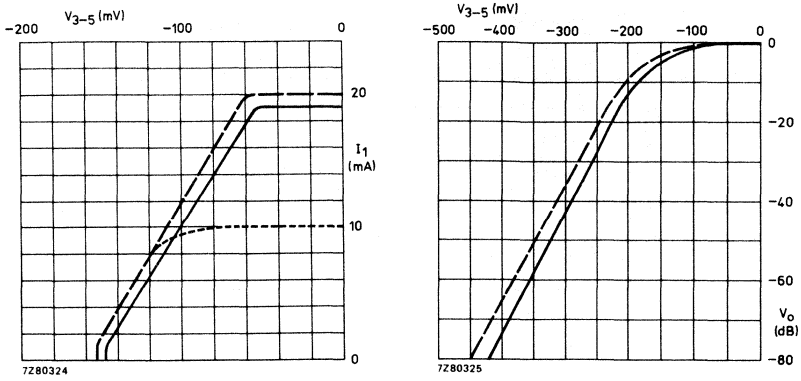


Fig. 13 Muting ( $V_O$ ) and muting indicator current ( $I_1$ ) as a function of  $V_{3-5}$ .

$V_O$  in dB curves; ———  $V_P = 8,5 \text{ V}$   
 - - - -  $V_P = 15 \text{ V}$

$I_1$  in mA curves for  $V_{PL}/R_{bias1}$  (pin 1); - · - · - 22 V/1 k $\Omega$   
 ——— 14 V/680  $\Omega$   
 · · · · · 10 V/680  $\Omega$

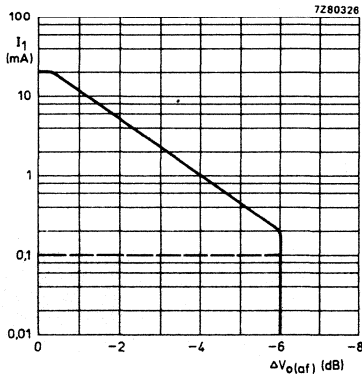


Fig. 14 Muting indicator current;  $V_P = 8,5$  to  $15 \text{ V}$ ;  $V_{PL} = 14 \text{ V}$ .

———  $R_{bias1} = 680 \Omega$   
 - - - -  $R_{bias1} = \text{matched}$

DEVELOPMENT SAMPLE DATA





## AUTOMATIC TUNING CIRCUIT

### GENERAL DESCRIPTION

The TDA1580 is a monolithic integrated circuit for automatic tuning applications in TV and radio receivers.

#### Features

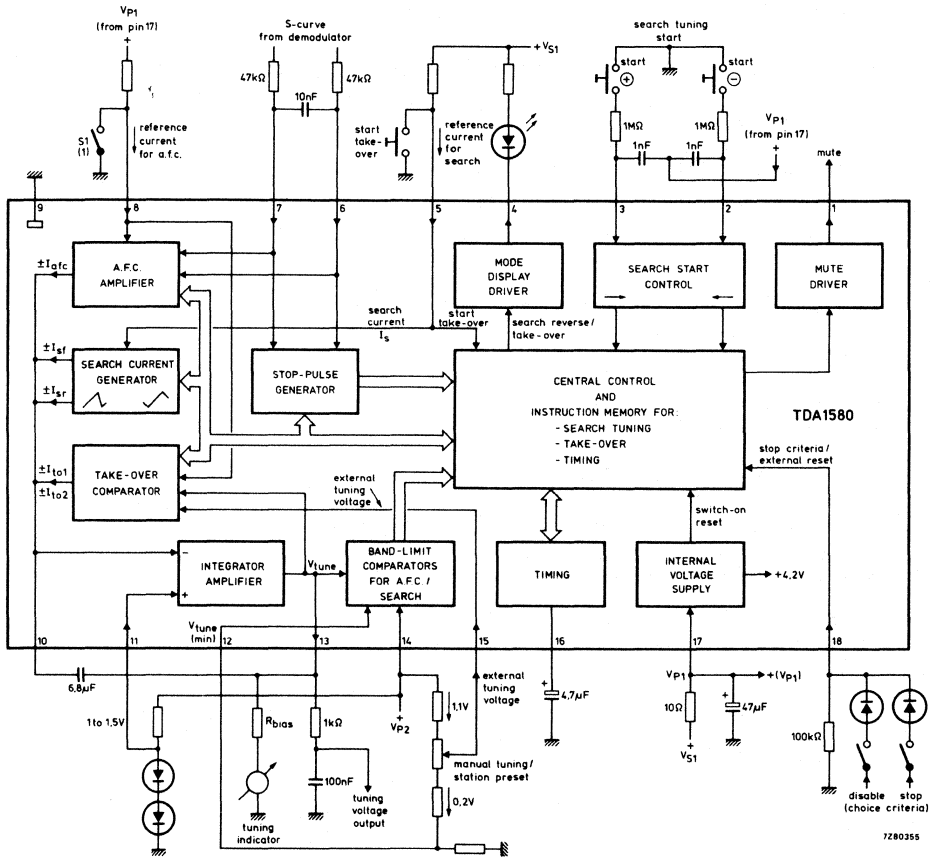
- Bi-directional search; sawtooth characteristic
- Stop-pulse generator (S-curve evaluation)
- Start/stop memory
- Internal control of timing and mute operation
- Take-over circuit for external station-presets
- Search tuning always starts from previous tuning position
- Integrating a.f.c.
- Integrator/amplifier for driving analogue displays
- Comparators for band limits
- Station select input (e.g. field-strength, stereo, traffic news, TV carrier)
- Adjustable a.f.c. and search-tuning characteristic
- Internal switch-on reset (preset station circuit take-over)

### QUICK REFERENCE DATA

Supply voltages			
(pin 17)	$V_{p1}$	typ.	15 V
(pin 14)	$V_{p2}$	typ.	30 V
Supply currents (unloaded)			
(pin 17)	$I_{p1}$	typ.	10 mA
(pin 14)	$I_{p2}$	typ.	1,2 mA
Tuning voltage	$V_{13-9}$		0,5 to $V_{p2}-1$ V
Permissible load current (for display)	$I_{13}$	typ.	1,2 mA
Integrator current for search (adjustable)	$\pm I_{s10}$		20 to 200 $\mu$ A
Integrator input current (a.f.c. off)	$I_{o10}$	typ.	10 nA
Input voltage range for the a.f.c. inputs	$V_{6;7-9}$		2,5 to $V_{p1}-1,4$ V
Supply voltage ranges			
(pin 17)	$V_{p1}$		6 to 24 V
(pin 14)	$V_{p2}$		6 to 33 V
Operating ambient temperature range	$T_{amb}$		-30 to +80 °C

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



(1) S1:

- 1 – A.F.C. OFF (search stand-by mode)
- 2 – Continuous take-over without muting (take-over stand-by mode)

Fig. 1 Block diagram.



## MEMORY CONVERTER FOR 4 PRESETS

### GENERAL DESCRIPTION

The TDA1584 is a monolithic integrated circuit designed as a memory store for preset tuning positions. Together with the TDA1580 it forms a complete tuning system.

The operation of the TDA1584 memory is based on a 4 x 12-bit data format. The information of 4 preset stations is stored in that memory. The circuit also comprises a 12-bit D/A converter, a 12-bit counter acting as a memory for the last tuned position, two comparators, a voltage-controlled analogue switch and a sequential control logic.

The circuit is capable of digitizing and storing an external d.c. voltage as well as converting stored digital information to a d.c. voltage which is available at output  $V_{TO}$  (pin 9).

A built-in adjustable oscillator provides the reference for the correct timing of the internal functions. However, it does not operate continuously.

### Features

- Static 12-bit DAC (Digital-to-Analogue Converter)
- 4 presets with 12-bit code available
- Stand-by mode
- A/D conversion of the search tuning voltage and tuning-potentiometer voltage when in the manual mode
- Storage of search and manual tuned voltages
- Automatic a.f.c. selection during the manual tuning mode
- Automatic clamped tuning voltage during reduced signal strength (without a.f.c.)
- Minimal external circuit components required
- Automatic memory set-up when switched-on for the first time (e.g., not from the stand-by position)

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



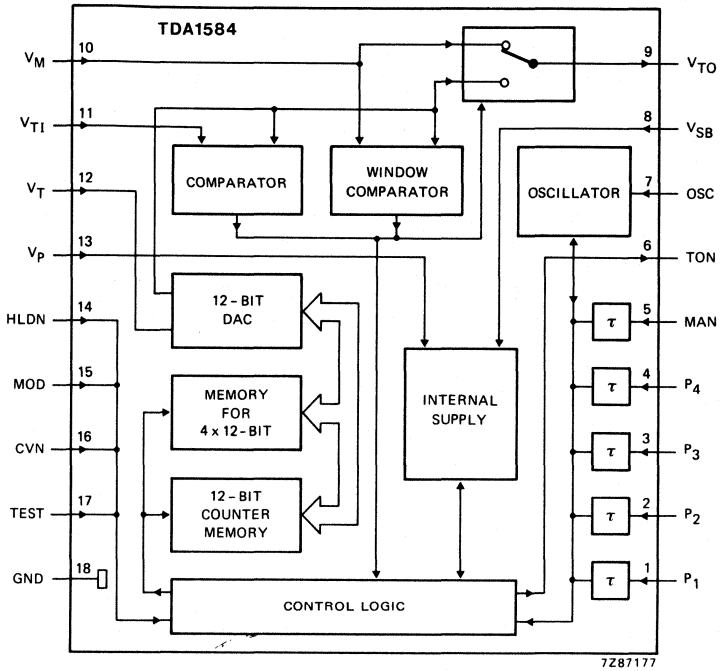


Fig. 1 Block diagram.

**PINNING**

- 1 P<sub>1</sub> preset 1 input
- 2 P<sub>2</sub> preset 2 input
- 3 P<sub>3</sub> preset 3 input
- 4 P<sub>4</sub> preset 4 input
- 5 MAN manual tuning input
- 6 TON take-over output
- 7 OSC oscillator input
- 8 V<sub>SB</sub> stand-by supply
- 9 V<sub>TO</sub> tuning voltage output
- 10 V<sub>M</sub> tuning voltage manual
- 11 V<sub>Tl</sub> tuning voltage input
- 12 V<sub>T</sub> tuning voltage supply
- 13 V<sub>p</sub> main supply
- 14 HLDN hold input
- 15 MOD mode input
- 16 CVN converter input
- 17 TEST test input
- 18 GND ground

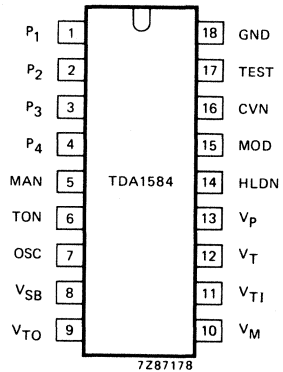


Fig. 2 Pinning diagram.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA1589

## TRAFFIC CONTROL MESSAGES AND WARNING TONE CIRCUIT

The TDA1589 is for evaluation of operating signals and logic control signals of a traffic control (TC) message decoder.

### Features

- mute of non-traffic control stations
- restriction to traffic-control message reception
- LED display driver for MUTE indication
- control output for TC messages minimum volume
- delayed start of warning tone signal on failure of TC transmission. Also to be used to control a start of search tuning
- warning tone generator with automatic level control increasing volume in five steps
- interruption of cassette playback with motor stop during TC messages
- warning tone indicating failure of TC transmission also during cassette playback

### QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_p$	7,5 to 16 V typ. 8,5 V
Supply current	$I_p$	typ. 4,5 mA
Warning tone maximum voltage	$V_{o(p-p)}$	typ. 4,3 V
Output LED driver current (pin 3)	$I_3$	typ. 30 mA
motor stop current (pin 5)	$I_5$	typ. 30 mA
motor stop current (pin 6)	$I_6$	typ. 2 mA
MUTE display current (pin 8)	$I_8$	typ. 2 mA
start warning tone current (pin 13)	$I_{13}$	typ. 2 mA
Saturation voltage at output for minimum volume-on (pin 7)	$V_{7\text{ sat}}$	< 0,1 V

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

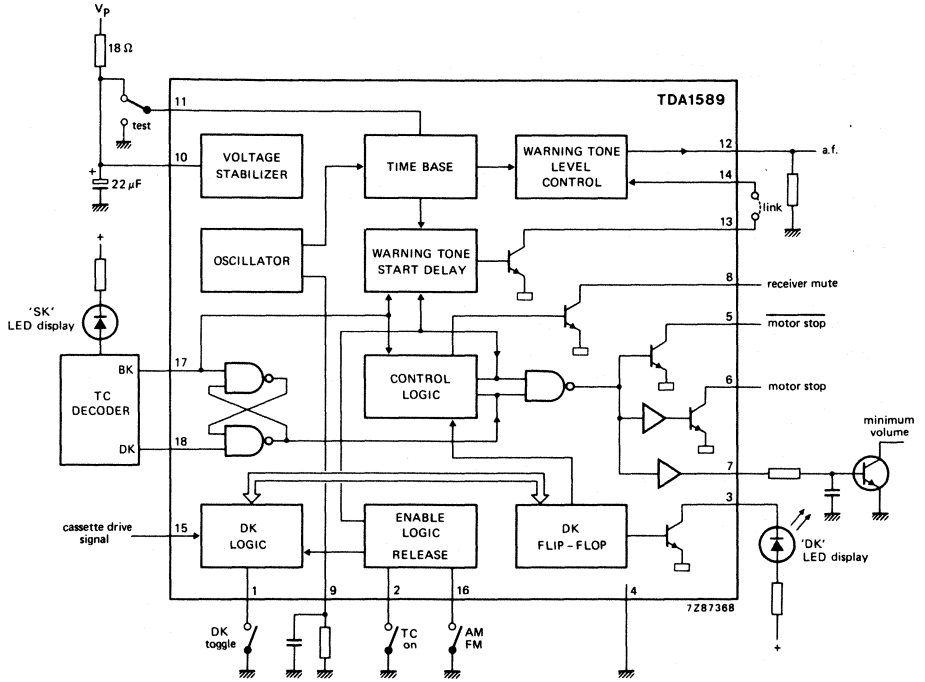


Fig. 1 Block diagram with external components; used as test circuit.

BK = TC area identification code (BereichsKennung)  
 DK = TC message identification code (DurchsageKennung)  
 SK = TC station identification code (SenderKennung)

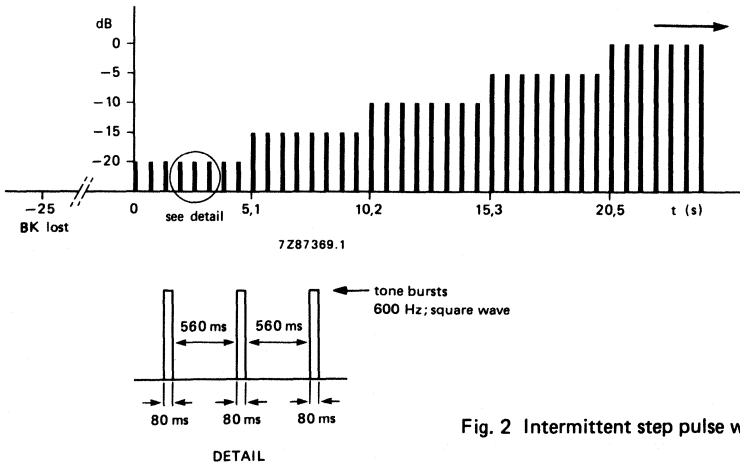


Fig. 2 Intermittent step pulse warning signal.

## FUNCTIONAL DESCRIPTION

The automatic evaluation of traffic control signals is only possible during FM reception. The enable circuit will be active when pin 16 (FM on) is LOW. If traffic control messages are desired, pin 2 (TC on) must be switched to LOW.

### FM radio mode

By operating the DK-toggle switch at pin 1 the DK flip-flop is set. This is displayed by a LED connected to pin 3. In the position "TC off" (pin 2 HIGH) it is not possible to set the DK flip-flop. Non-traffic control stations are muted. If a message is transmitted on the tuned TC station the minimum volume at pin 7 is exposed.

In case of BK-signal failure pin 13 changes to LOW after a delay of about 25 seconds. If pins 13 and 14 are then connected, an intermittent warning signal will be supplied at pin 12. The level increases automatically from  $-20$  dB to 0 dB in 5 steps. (See Fig. 2.)

### Cassette mode

If a TC message is delivered when TC is switched on (pin 16 and pin 2 LOW) and the DK flip-flop is set, the motor of the cassette player is stopped and the receiver automatically cuts in. The minimum volume is also set at the same time.

In case of BK-signal failure, the warning tone will be mixed into the cassette playback.

### Protection

To avoid faulty switching, an internal latch will be set only if both DK (pin 18) and BK (pin 17) are HIGH. The latch will be reset if DK is changed to LOW independent of BK.

Reset of the DK-toggle flip-flop:

- by operating the DK-toggle (pin 1) twice
- by opening the TC-switch (pin 2)
- by switching to AM reception (pin 16)
- by switching off the cassette-player (pin 15)
- by switching power off or on.

### Transmission monitoring

At reception failure of a TC-station BK at pin 17 will become LOW. After about 25 seconds the output (pin 13) will be set LOW to start the warning signal via the jumper between pins 13 and 14. In the meantime the search-tuning can also be started. The warning tone stage gives a graduated signal with a level increasing in five steps from  $-20$  dB to 0 dB in about 20 seconds. The frequency of the warning signal is about 600 Hz; tone period  $\approx 80$  ms; pause  $\approx 560$  ms.

If now another TC-message transmitter has been tuned the input BK (pin 17) becomes HIGH and the warning tone is stopped. Also when switching TC-off (pin 2 HIGH) or switching to AM reception (pin 16 HIGH) the warning tone will stop. The BK-signal has to be stable for more than 1 second to reset the just started 25-second-timer.



mode	inputs pin numbers						outputs pin numbers					
	16	2	15	1	17	18	7	5	6	8	13	3
AM RADIO	H	X	X	X	X	X	H	L	H	H	H	H
FM RADIO TC off	L	H	X	X	X	X	H	H	L	H	H	H
FM-TC on station without TC	L	L	X	X	L	X	H	H	L	L	L*	L
FM-TC on station with BK	L	L	X	H	H	L	H	H	L	H	H	H
FM-TC on station with BK, DK	L	L	X	H	H	H	L	L	H	H	H	H
FM-TC on station with BK DK-toggle operated MUTE	L	L	X		H	L	H	H	L	L	H	
FM-TC on station with BK, DK incoming message	L	L	X	H	H						H	L
FM-TC on station with BK DK-toggle operated twice	L	L	X		H	L	H	H	L		H	
FM-TC on and cassette station with BK, DK cassette switched on	L	L		X	H	H	L	L	H	H	H	H
FM-TC on and cassette station with BK cassette switched on	L	L		X	H	L	H	H	L	H	H	H
FM-TC on and cassette station with BK cassette switched off	L	L		X	H	L	H	H	L		H	
function and state	AM/FM HIGH/LOW	TC on on = LOW	cassette off = H → L	DK toggle active = LOW	BK on = HIGH	DK on = HIGH	min. volume on = LOW	motor stop stop = LOW	motor stop stop = HIGH	MUTE on = LOW	warning time on = LOW	DK display on = LOW

\* After about 25 seconds.

Positive logic:

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

= positive-going transition

= negative-going transition

**Functions of the control inputs**

DK toggle operated  
chatter-proof by internal delay  
of 10 to 20 ms

TC (traffic control) released

Test condition  
clock rate 24 times faster

Start warning signal

Reset of DK flip-flop  
by cassette player

Reset of DK flip-flop  
by tuning AM band

BK input\*

DK input\*

Minimum volume

Motor stop (30 mA)

Motor stop (2 mA)

MUTE (volume off)

Warning tone

DK display

pin 1	active	=	LOW
pin 2	on	=	LOW
pin 11	on	=	to ground
	off	=	to $V_p$ or open
pin 14	on	=	LOW
pin 15	reset	=	HIGH to LOW transition
pin 16	reset	=	HIGH
pin 17	on	=	HIGH
pin 18	on	=	HIGH
pin 7	on	=	LOW
pin 5	stop	=	LOW
pin 6	stop	=	HIGH
pin 8	on	=	LOW
pin 13	on	=	LOW
pin 3	on	=	LOW

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	$V_p$	max.	16 V
Input voltages pins 1, 2, 11, 14, 15, 16, 17 and 18	$V_i$		0 to $V_p$ V
Output voltages pins 3, 5, 6, 8, 13	$V_o$	max.	23 V
Currents inputs 1, 2, 11, 14, 15, 16, 17 and 18	$I_i$	max.	10 mA
outputs 6, 8, 13	$I_o$	max.	10 mA
outputs 3 and 5	$I_o$	max.	50 mA
Storage temperature	$T_{stg}$		-55 to +150 °C
Operating ambient temperature	$T_{amb}$		-30 to +80 °C

\* Open collector output of TC-decoder.

**CHARACTERISTICS**

$V_p$  typ. 8,5 V;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified (see Fig. 1)

Supply voltage range	$V_p$	7,5 to 16 V
Supply current	$I_p$	typ. 4,5 mA < 6 mA

**Control inputs**

Pins 1, 2, 11, 14, 15, 16, 17 and 18

Input voltage HIGH	$V_{IH}$	3,5 V to $V_p$
Input voltage LOW	$V_{IL}$	< 2 V
Input current HIGH $V_i = 16\text{ V}$	$I_{IH}$	< 1 $\mu\text{A}$
Input current LOW $V_i = 0\text{ V}$	$-I_{IL}$	50 to 200 $\mu\text{A}$
Input resistance $V_i = 0\text{ V}$	$R_i$	< 10 k $\Omega$

**Control outputs**

DK-LED display and motor stop  
open collector outputs 3 and 5

Output voltage LOW $I_{OL} = 20\text{ mA}$	$V_{OL}$	typ. 1 V < 1,5 V
Output current LOW	$I_{OL}$	typ. 30 mA
Output voltage HIGH (open collector) $I_{OH} < 10\text{ }\mu\text{A}$	$V_{OH}$	< 23 V

LF-MUTE, motor stop and warning signal start  
pins 8, 6 and 13

Output voltage LOW $I_{OL} = 1\text{ mA}$	$V_{OL}$	< 0,35 V
Output current LOW	$I_{OL}$	= 2 mA
Output voltage HIGH (open collector) $I_{OH} < 1\text{ }\mu\text{A}$	$V_{OH}$	= 16 V

Minimum voltage (pin 7) ( $R_S = 800\text{ }\Omega$ ,  $R_L = \infty$ )

Output voltage LOW (for volume HIGH)	$V_{7.4}$	< 0,1 V
Output voltage HIGH (for volume LOW)	$V_{7.4}$	typ. 5 V

**Warning signal (pin 12)**

$f = 600\text{ Hz}$ ; square-wave pulsed;  $R_S = 300\text{ }\Omega$

Switching time on	$t_{on}$	typ. 80 ms
Switching time off	$t_{of}$	typ. 560 ms
Output voltage during $t_{on}$ at maximum peak ( $R_L = 1\text{ k}\Omega$ )	$V_{12.4}$	typ. 4,3 V
during $T_{off}$	$V_{12.4}$	typ. 0 V



**Automatic level control**

Duration per level	$t_p$	typ.	5 s
Output level swing (in 5 steps)	$\Delta V_{12-4}$		-20 to 0 dB
Output current peak value	-I <sub>12M</sub>	typ.	6 mA

**Oscillator (pin 9)**

Frequency	f	typ.	2400 Hz
Filter resistance	R <sub>0</sub>	typ.	100 kΩ
Filter capacitance	C <sub>0</sub>	typ.	4,7 nF
Oscillator frequency tolerance	$\Delta f/f$		-10 to + 10 %

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## DISPLAY/DRIVER CIRCUIT FOR 11 LEDs

The TDA1594 is a monolithic integrated circuit intended to drive 11 LEDs for analogue signal display. Two display modes are possible: as a pointer (only one LED on) or as a bar (a row of LEDs on).

The circuit contains the following functions:

- A/D converter with S-shaped pre-compensated control curve.
- Current control of LED with separate selectable bias current for the display limits.
- External brightness control; e.g. by an LDR (Light Dependent Resistor).
- External adjustable brightness take-over of the display segments.
- High-ohmic control input; diode protected.
- Internal reference voltage (proportional to  $V_T$ ).

### QUICK REFERENCE DATA

Supply voltage range (pin 12)	$V_P$	7,5 to 23 V
Supply current (pin 12)	$I_P$	typ. 6 mA
Control voltage range	$\pm V_C$	typ. 100 mV
Reference input voltage range	$V_I$	2 to $V_P - 4$ V
Adjustable output current	$I_O$	0 to 25 mA
Output reverse voltage	$V_{OR}$	typ. 25 V
Output saturation voltage	$V_{Osat}$	< 2,5 V
-----		
Ambient temperature range	$T_{amb}$	-30 to +80 °C



### PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

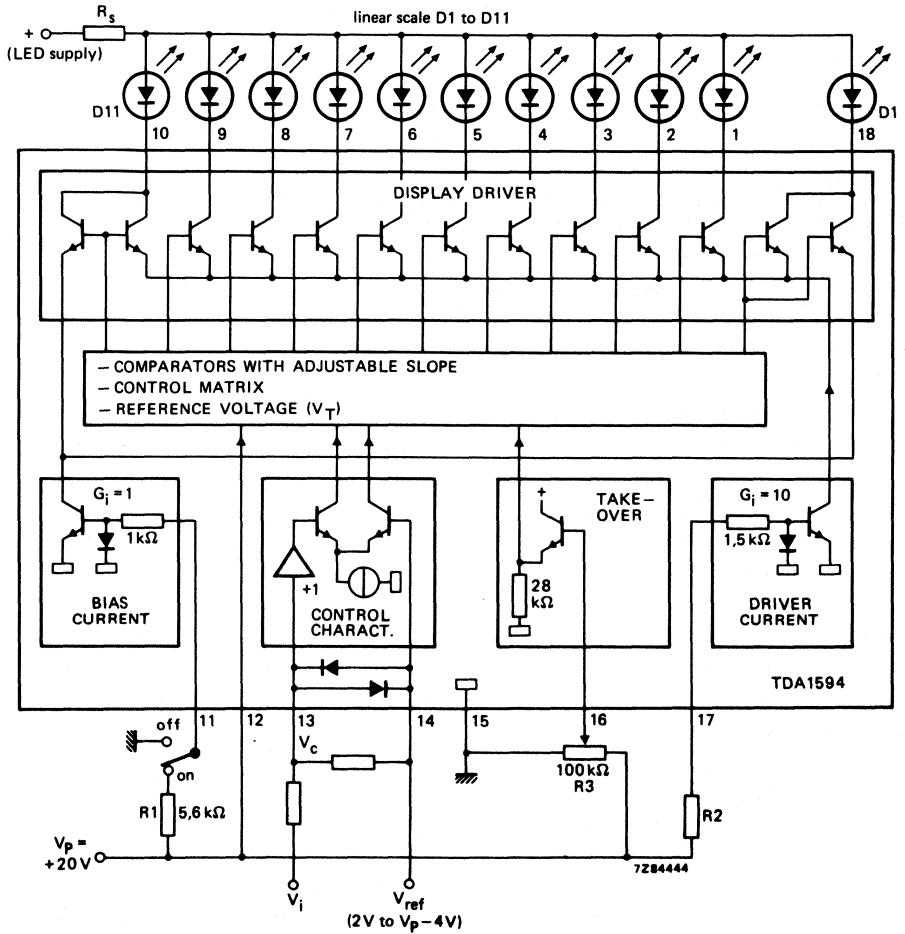


Fig. 1 Block diagram and external components.

## 5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- possibility for increasing the input impedance
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

## QUICK REFERENCE DATA

Supply voltage range	$V_P$	6 to 35 V
Repetitive peak output current	$I_{ORM}$	< 1,5 A
Output power at $d_{tot} = 10\%$		
$V_P = 18\text{ V}; R_L = 8\ \Omega$	$P_O$	typ. 4,5 W
$V_P = 25\text{ V}; R_L = 15\ \Omega$	$P_O$	typ. 5 W
Total harmonic distortion at $P_O < 2\text{ W}; R_L = 8\ \Omega$	$d_{tot}$	typ. 0,3 %
Input impedance	$ Z_i $	typ. 45 k $\Omega$
Total quiescent current at $V_P = 18\text{ V}$	$I_{tot}$	typ. 25 mA
Sensitivity for $P_O = 2,5\text{ W}; R_L = 8\ \Omega$	$V_i$	typ. 55 mV
Operating ambient temperature	$T_{amb}$	-25 to + 150 °C
Storage temperature	$T_{stg}$	-55 to + 150 °C



## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

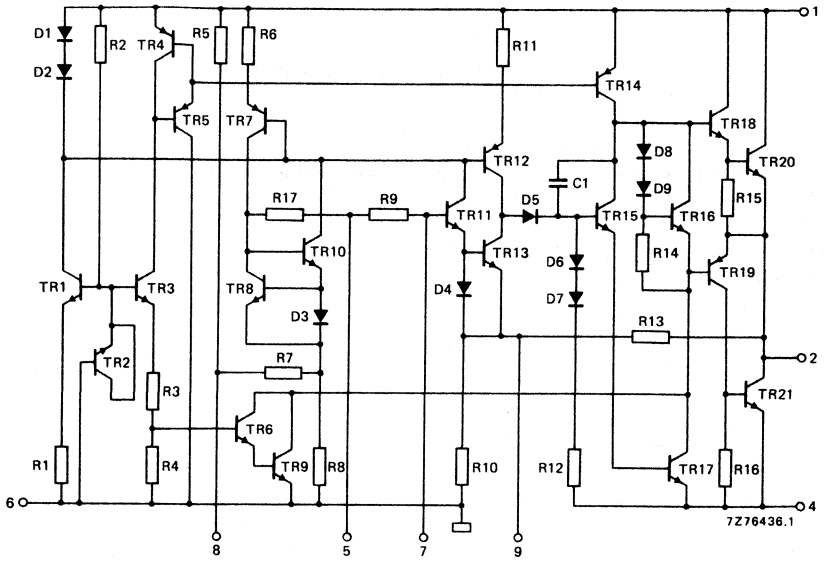


Fig. 1 Circuit diagram; pin 3 not connected.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_p$	max.	35 V
Non-repetitive peak output current	$I_{OSM}$	max.	3 A
Repetitive peak output current	$I_{ORM}$	max.	1,5 A
Total power dissipation			see derating curves Fig. 2
Storage temperature	$T_{stg}$		-55 to + 150 °C
Operating ambient temperature	$T_{amb}$		-25 to + 150 °C

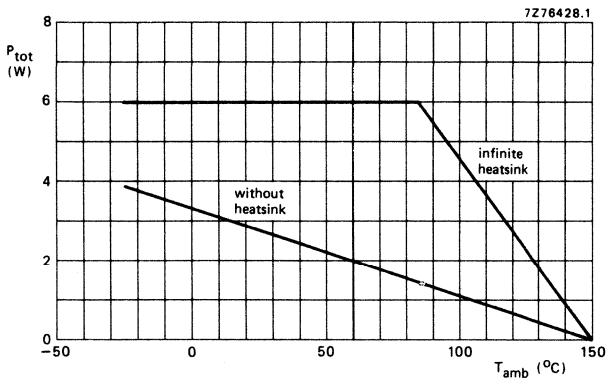


Fig. 2 Power derating curves.

## HEATSINK EXAMPLE

Assume  $V_p = 18$  V;  $R_L = 8 \Omega$ ;  $T_{amb} = 60$  °C maximum;  $T_j = 150$  °C (max. for a 4 W application into an  $8 \Omega$  load, the maximum dissipation is about 2,2 W).

The thermal resistance from junction to ambient can be expressed as:

$$R_{th j-a} = R_{th j-tab} + R_{th tab-h} + R_{th h-a} = \frac{150 - 60}{2,2} = 41 \text{ K/W.}$$

Since  $R_{th j-tab} = 11$  K/W and  $R_{th tab-h} = 1$  K/W,  $R_{th h-a} = 41 - (11 + 1) = 29$  K/W.

## D.C. CHARACTERISTICS

Supply voltage range	$V_p$	6 to 35 V
Repetitive peak output current	$I_{ORM}$	< 1,5 A
Total quiescent current at $V_p = 18$ V	$I_{tot}$	typ. 25 mA

## A.C. CHARACTERISTICS

$T_{amb} = 25$  °C;  $V_p = 18$  V;  $R_L = 8$   $\Omega$ ;  $f = 1$  kHz unless otherwise specified; see also Fig. 3

A.F. output power at  $d_{tot} = 10\%$

$V_p = 18$ V; $R_L = 8$ $\Omega$	$P_o$	> 4 W
	typ.	4,5 W
$V_p = 12$ V; $R_L = 8$ $\Omega$	$P_o$	typ. 1,7 W
$V_p = 8,3$ V; $R_L = 8$ $\Omega$	$P_o$	typ. 0,65 W
$V_p = 20$ V; $R_L = 8$ $\Omega$	$P_o$	typ. 6 W
$V_p = 25$ V; $R_L = 15$ $\Omega$	$P_o$	typ. 5 W

Total harmonic distortion at  $P_o = 2$  W

$d_{tot}$	typ.	0,3 %
	<	1 %

Frequency response

	>	15 kHz
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Input impedance

$ Z_i $	typ.	45 k $\Omega$ *
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Noise output voltage at  $R_S = 5$  k $\Omega$ ; B = 60 Hz to 15 kHz

$V_n$	typ.	0,2 mV
	<	0,5 mV

Sensitivity for  $P_o = 2,5$  W

$V_i$	typ.	55 mV
		44 to 66 mV

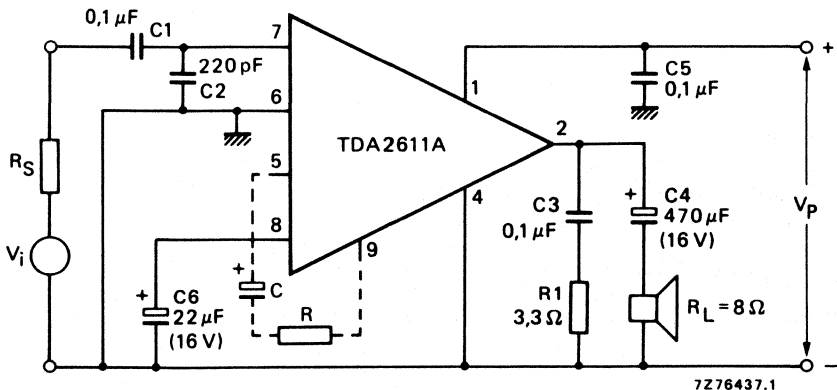


Fig. 3 Test circuit; pin 3 not connected.

\* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).



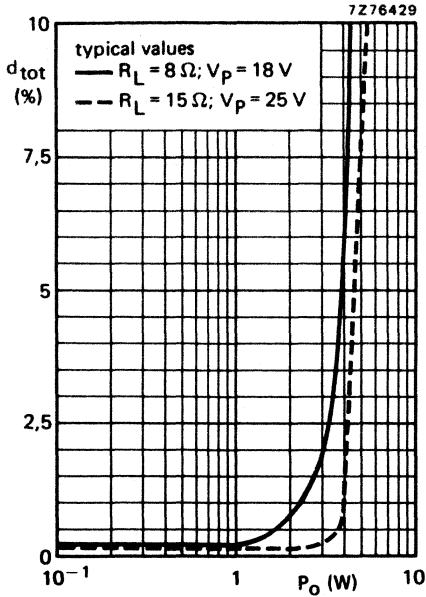


Fig. 4 Total harmonic distortion as a function of output power.

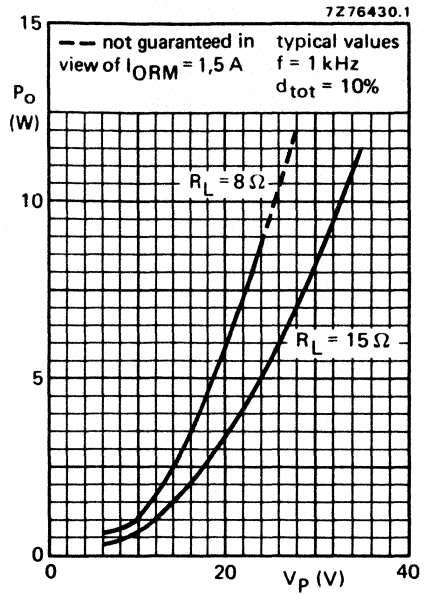


Fig. 5 Output power as a function of supply voltage.

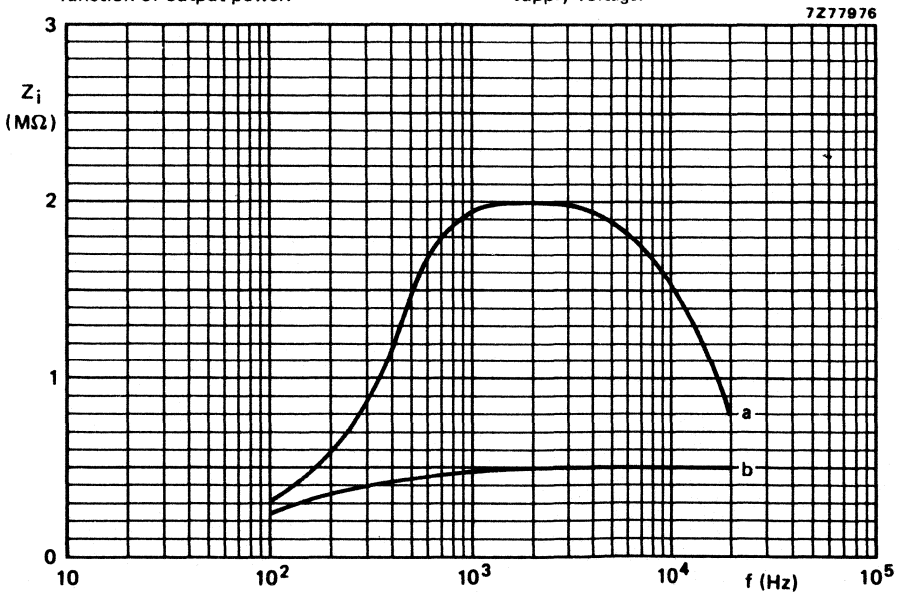


Fig. 6 Input impedance as a function of frequency; curve a for  $C = 1 \mu\text{F}, R = 0 \Omega$ ; curve b for  $C = 1 \mu\text{F}, R = 1 \text{ k}\Omega$ ; circuit of Fig. 3;  $C_2 = 10 \text{ pF}$ ; typical values.

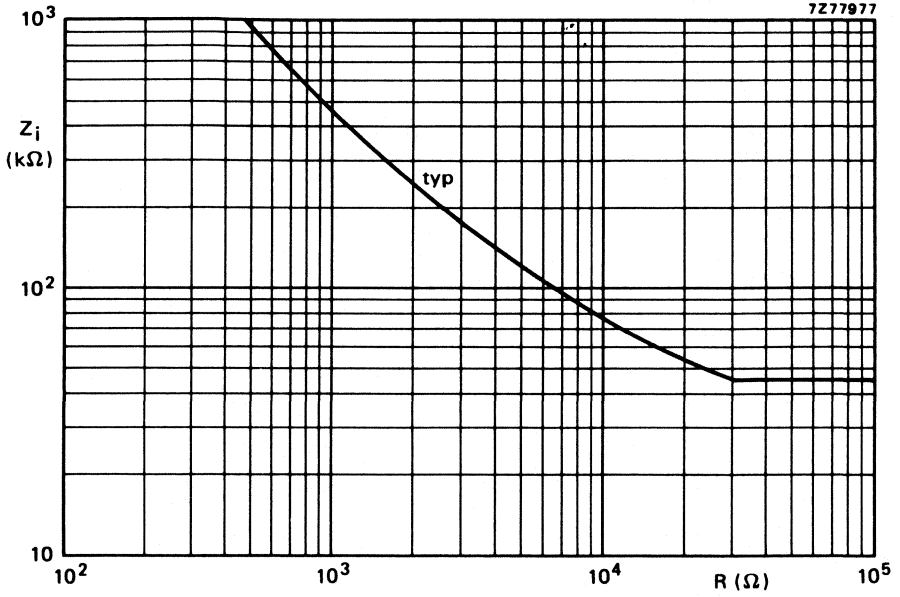


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

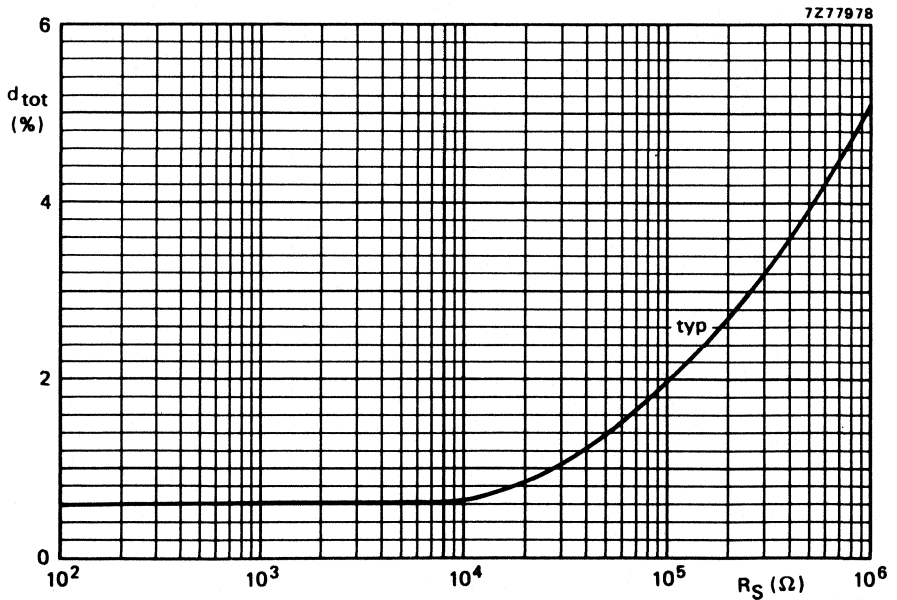


Fig. 8 Total harmonic distortion as a function of R<sub>S</sub> in the circuit of Fig. 3; P<sub>O</sub> = 3,5 W; f = 1 kHz.

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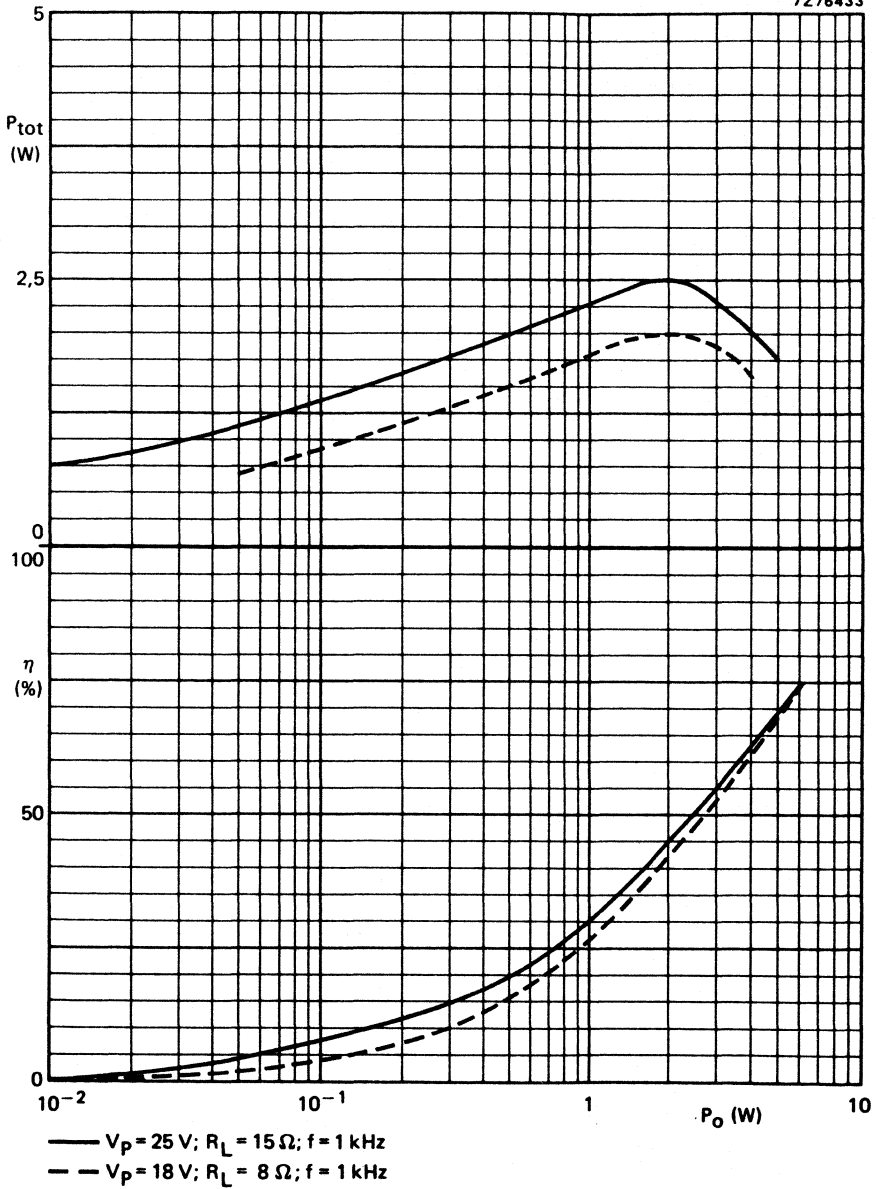


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

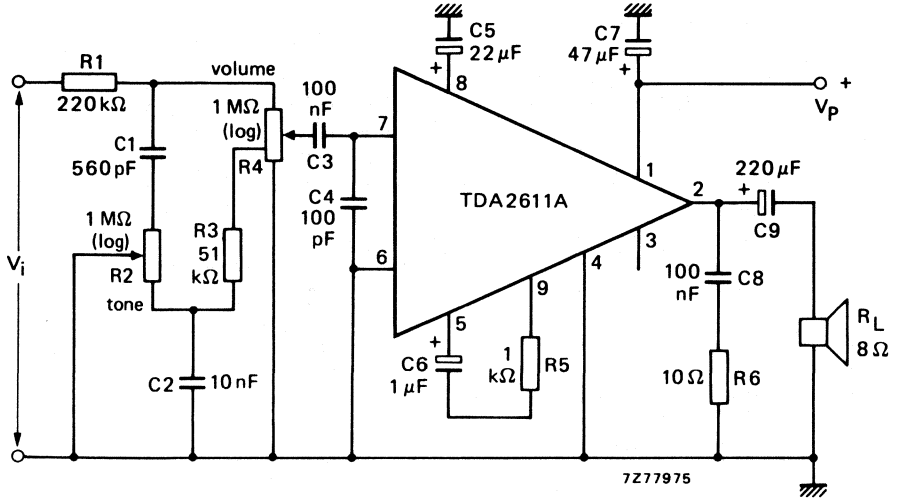


Fig. 10 Ceramic pickup amplifier circuit.

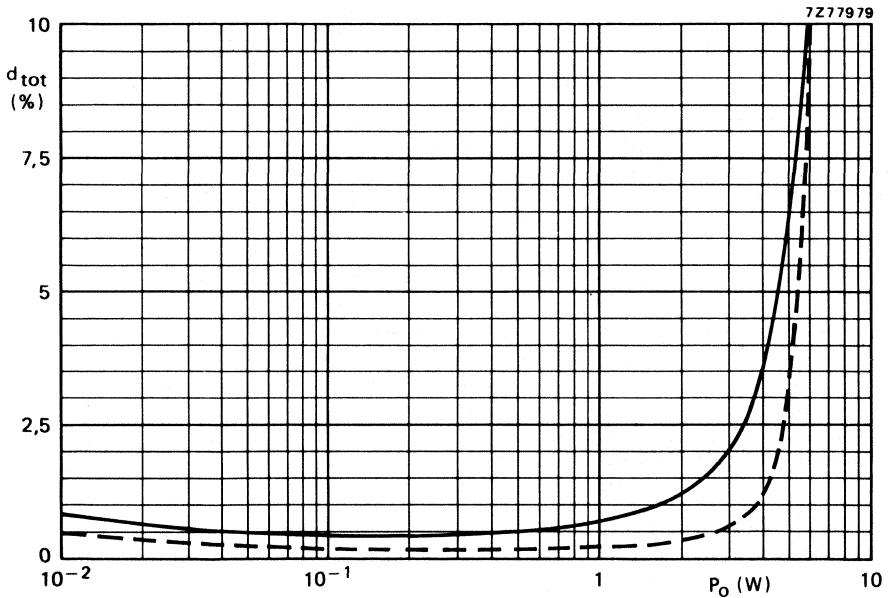


Fig. 11 Total harmonic distortion as a function of output power; — with tone control; - - - without tone control; in circuit of Fig. 10; typical values.

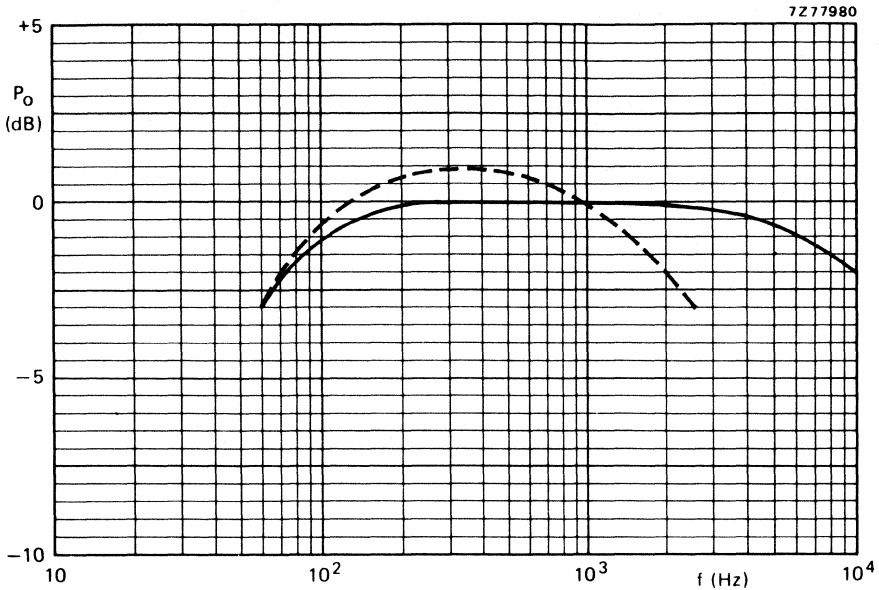


Fig. 12 Frequency characteristics of the circuit of Fig. 10; — tone control max. high; - - - tone control min. high;  $P_o$  relative to 0 dB = 3 W; typical values.

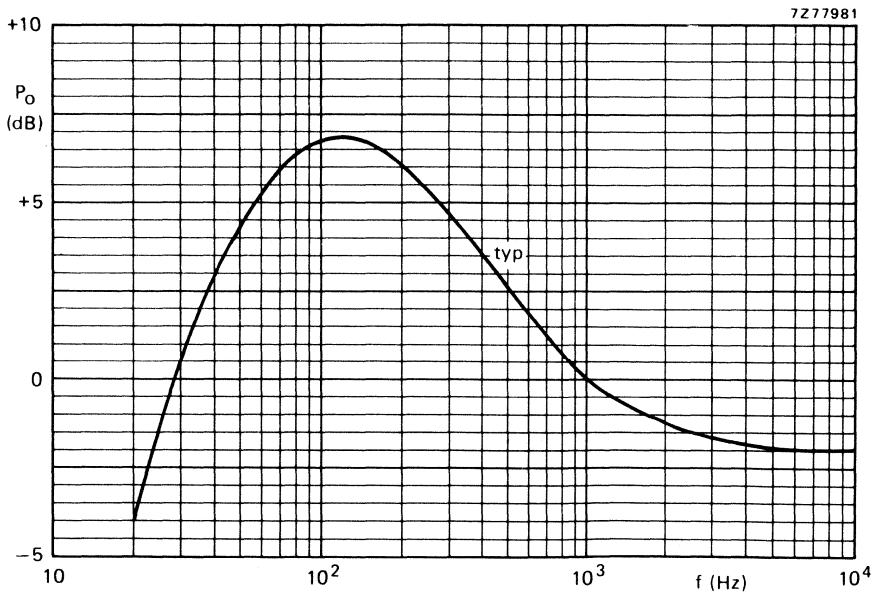
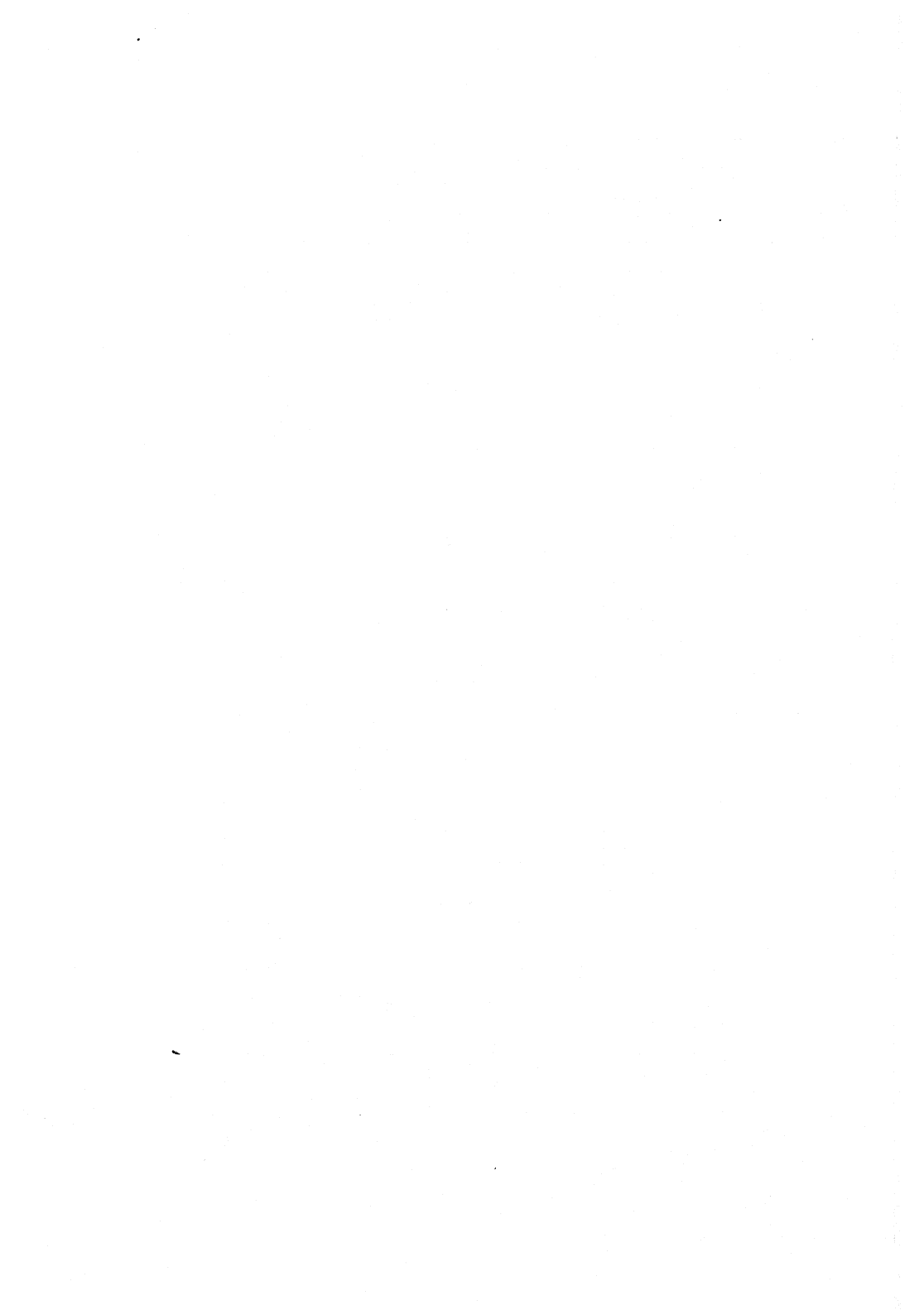


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.





## INTEGRATED AM/FM RADIO RECEIVER CIRCUIT

The TDA5700 is for use in high quality battery or mains-fed a.m. and a.m./f.m. receivers as well as small low-cost a.m. portable receivers. The IC incorporates: a.m. mixer, oscillator, i.f. amplifier, a.g.c. amplifier, a.m. detector and capacitor, f.m./i.f. limiting amplifier and stable base bias for f.m. front-end. The TDA5700 is pin compatible, with the h.f. part of the TBA570A and can be used with conventional coils or ceramic resonators.

The combination of a good sound quality ( $d_{tot}$ ) and quality of reception (a.g.c.) makes the IC well suitable for universal application of one basic printed-circuit board in a wide range of receiver designs.

### QUICK REFERENCE DATA

Applicable supply voltage range of receiver	$V_S$	2,7 to 12 V
Supply voltage range (pin 8)	$V_P$	3,4* to 5,4 V
Ambient temperature	$T_{amb}$	25 °C
Supply voltage (pin 8)	$V_P$	nom. 5,4 V
Total quiescent current	$I_{tot}$	typ. 9 mA
<b>A.M. performance</b> (at pin 2)		
Sensitivity for $V_O = 30$ mV	$V_i$	3,0 to 12 $\mu$ V
for $V_O = 30$ mV; range 1**	$V_i$	5,5 to 12 $\mu$ V
for $V_O = 30$ mV; range 2**	$V_i$	3,0 to 6,5 $\mu$ V
R.F. input voltage for S/N = 26 dB	$V_i$	typ. 16 $\mu$ V < 20 $\mu$ V
for $V_O = 10$ mV	$V_i$	typ. 2,5 $\mu$ V
A.G.C. range; change of r.f. input voltage for 10 dB expansion in audio range		typ. 65 dB
R.F. signal handling $d_{tot} = 10\%$ ; $m = 0,8$	$V_i$	typ. 300 mV
<b>F.M. performance</b> (at pin 2)		
R.F. input voltage 3 dB before limiting	$V_i$	typ. 180 $\mu$ V

\* Minimum supply voltage for guaranteed oscillator operation:  $V_P = 2,5$  V (see Fig. 3).

\*\* There are two ranges of sensitivity measured, and indicated by either '1' or '2' on the package. Ordering a specific range is not possible.

For designs requiring a lower spread of sensitivity, these ranges can be used adapting the application.

### PACKAGE OUTLINES

TDA5700: 16-lead DIL; plastic (SOT-38).

TDA5700Q: 16-lead QIL; plastic (SOT-58).

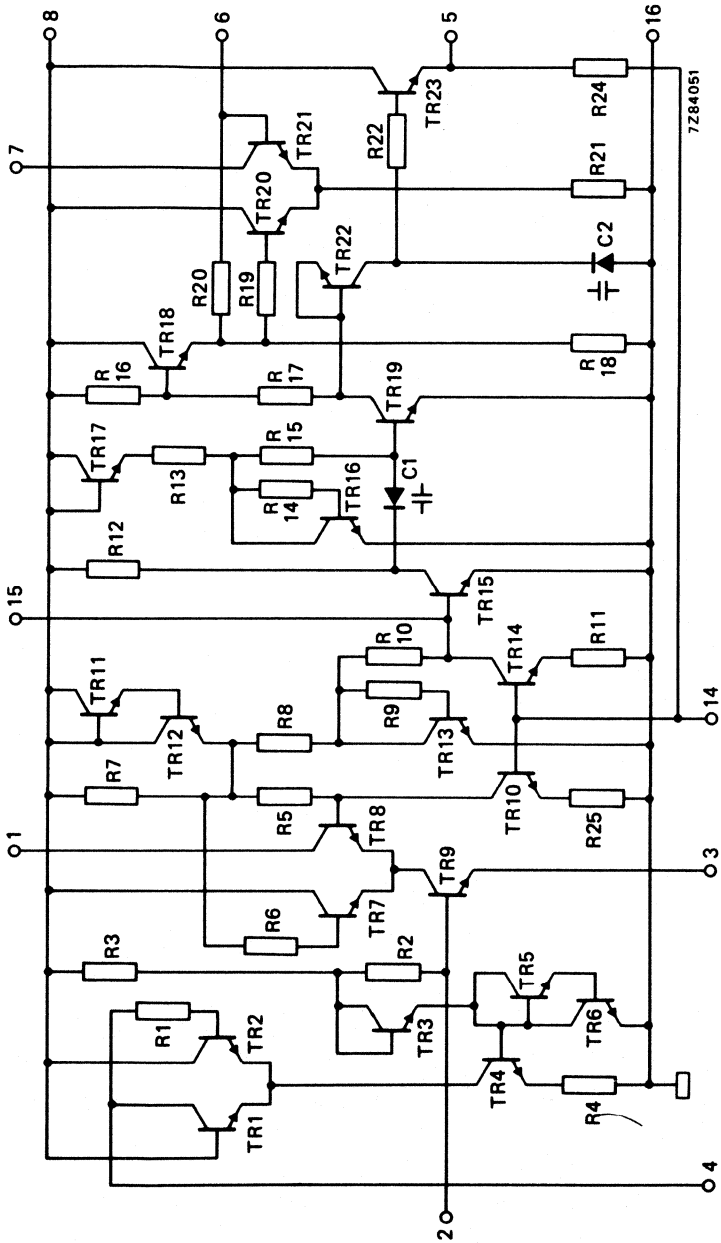


Fig. 1 Circuit diagram.



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA7000

# FM RADIO CIRCUIT

## GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

## QUICK REFERENCE DATA

Supply voltage range (pin 5)	$V_P$	2,7 to 10 V
Supply current at $V_P = 4,5$ V	$I_P$	typ. 8 mA
R.F. input frequency range	$f_{rf}$	1,5 to 110 MHz
Sensitivity for -3 dB limiting (e.m.f. voltage) (source impedance: 75 $\Omega$ ; mute disabled)	EMF	typ. 1,5 $\mu$ V
Signal handling (e.m.f. voltage) (source impedance: 75 $\Omega$ )	EMF	typ. 200 mV
A.F. output voltage at $R_L = 22$ k $\Omega$	$V_O$	typ. 75 mV

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

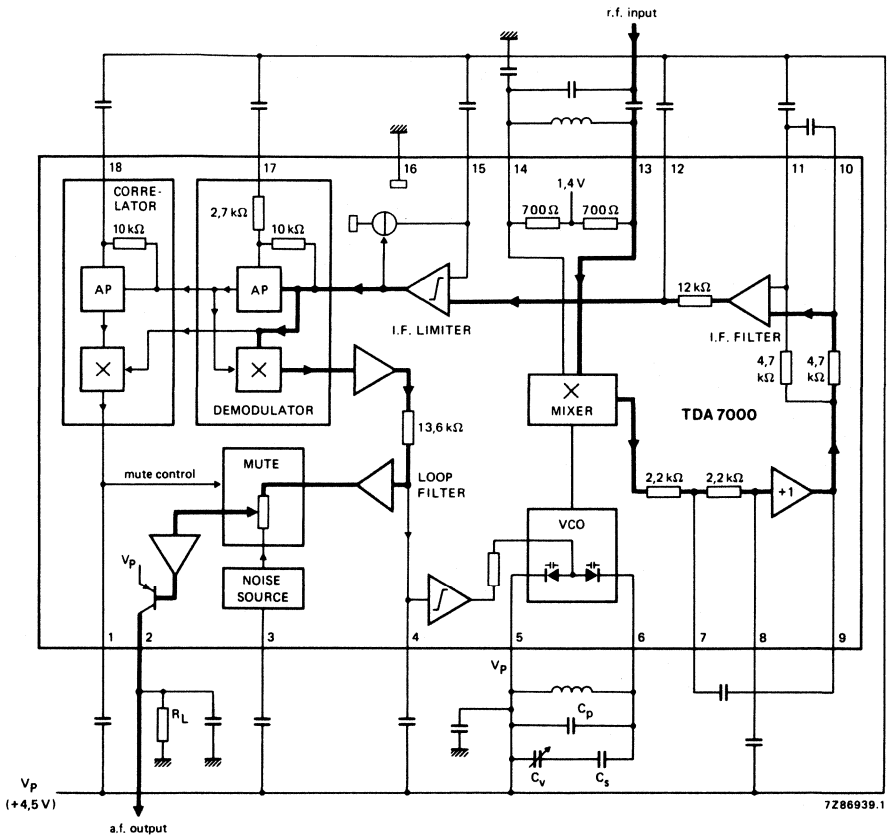


Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 5)	$V_p$	max.	12 V
Oscillator voltage (pin 6)	$V_{6-5}$	$V_p - 0,5$ to $V_p + 0,5$ V	
Total power dissipation		see derating curve Fig. 2	
Storage temperature range	$T_{stg}$	-55 to +150 °C	
Operating ambient temperature range	$T_{amb}$	0 to +60 °C	

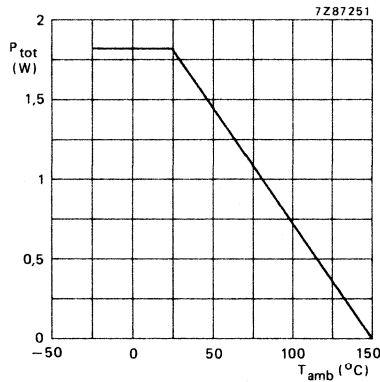


Fig. 2 Power derating curve.

**D.C. CHARACTERISTICS**

$V_p = 4,5$  V;  $T_{amb} = 25$  °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)	$V_p$	2,7	4,5	10	V
Supply current at $V_p = 4,5$ V	$I_p$	—	8	—	mA
Oscillator current (pin 6)	$I_6$	—	280	—	$\mu A$
Voltage at pin 14	$V_{14-16}$	—	1,35	—	V
Output current at pin 2	$I_2$	—	60	—	$\mu A$
Voltage at pin 2; $R_L = 22$ k $\Omega$	$V_{2-16}$	—	1,3	—	V



**A.C. CHARACTERISTICS**

$V_p = 4,5 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; measured in Fig. 4 (mute switch open, enabled);  $f_{rf} = 96 \text{ MHz}$  (tuned to max. signal at  $5 \text{ } \mu\text{V}$  e.m.f.) modulated with  $\Delta f = \pm 22,5 \text{ kHz}$ ;  $f_m = 1 \text{ kHz}$ ;  $EMF = 0,2 \text{ mV}$  (e.m.f. voltage at a source impedance of  $75 \text{ } \Omega$ ); r.m.s. noise voltage measured unweighted ( $f = 300 \text{ Hz}$  to  $20 \text{ kHz}$ ); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for -3 dB limiting; muting disabled	EMF	-	1,5	-	$\mu\text{V}$
for -3 dB muting	EMF	-	6	-	$\mu\text{V}$
for S/N = 26 dB	EMF	-	5,5	-	$\mu\text{V}$
Signal handling (e.m.f. voltage) for THD < 10%; $\Delta f = \pm 75 \text{ kHz}$	EMF	-	200	-	mV
Signal-to-noise ratio	S/N	-	60	-	dB
Total harmonic distortion					
at $\Delta f = \pm 22,5 \text{ kHz}$	THD	-	0,7	-	%
at $\Delta f = \pm 75 \text{ kHz}$	THD	-	2,3	-	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: $f_m = 1 \text{ kHz}$ ; $\Delta f = \pm 75 \text{ kHz}$ AM signal: $f_m = 1 \text{ kHz}$ ; $m = 80\%$	AMS	-	50	-	dB
Ripple rejection ( $\Delta V_p = 100 \text{ mV}$ ; $f = 1 \text{ kHz}$ )	RR	-	10	-	dB
Oscillator voltage (r.m.s. value) at pin 6	V6-5(rms)	-	250	-	mV
Variation of oscillator frequency with supply voltage ( $\Delta V_p = 1 \text{ V}$ )	$\Delta f_{osc}$	-	60	-	kHz/V
Selectivity					
	S+300	-	45	-	dB
	S-300	-	35	-	dB
A.F.C. range	$\Delta f_{rf}$	-	$\pm 300$	-	kHz
Audio bandwidth at $\Delta V_O = 3 \text{ dB}$ measured with pre-emphasis ( $t = 50 \text{ } \mu\text{s}$ )	B	-	10	-	kHz
A.F. output voltage (r.m.s. value) at $R_L = 22 \text{ k}\Omega$	$V_O(\text{rms})$	-	75	-	mV
Load resistance					
at $V_p = 4,5 \text{ V}$	$R_L$	-	-	22	$\text{k}\Omega$
at $V_p = 9,0 \text{ V}$	$R_L$	-	-	47	$\text{k}\Omega$

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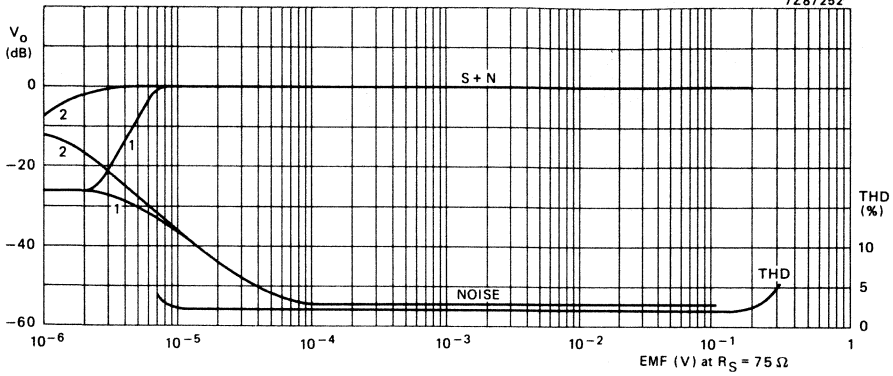


Fig. 3 A.F. output voltage ( $V_0$ ) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance ( $R_S$ ) of  $75 \Omega$ : (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV;  $f_{rf} = 96$  MHz.

for  $S + N$  curve:  $\Delta f = \pm 22,5$  kHz;  $f_m = 1$  kHz.

for THD curve:  $\Delta f = \pm 75$  kHz;  $f_m = 1$  kHz.

**Notes**

1. The muting system can be disabled by feeding a current of about  $20 \mu A$  into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.



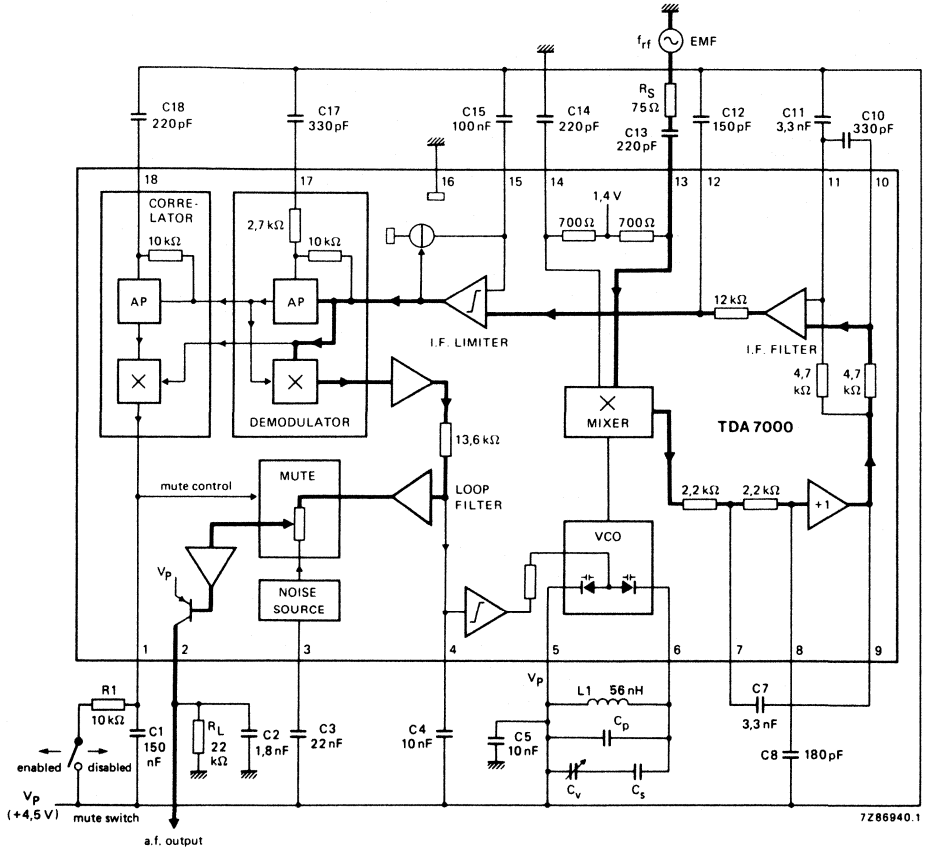
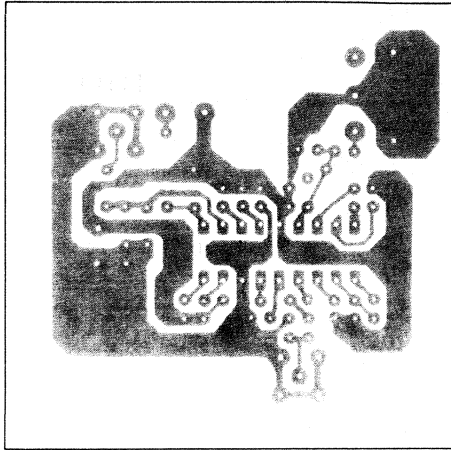
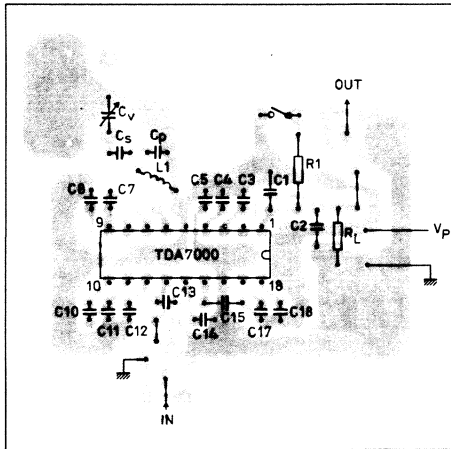


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.



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Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.



7286937.1

Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.





## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TDA7010T

# FM RADIO CIRCUIT

## GENERAL DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7010T includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

## QUICK REFERENCE DATA

Supply voltage range (pin 4)	$V_p$	2,7 to 10 V
Supply current at $V_p = 4,5$ V	$I_p$	typ. 8 mA
R.F. input frequency range	$f_{rf}$	1,5 to 110 MHz
Sensitivity for -3 dB limiting (e.m.f. voltage) (source impedance: 75 $\Omega$ ; mute disabled)	EMF	typ. 1,5 $\mu$ V
Signal handling (e.m.f. voltage) (source impedance: 75 $\Omega$ )	EMF	typ. 200 mV
A.F. output voltage at $R_L = 22$ k $\Omega$	$V_o$	typ. 75 mV

## PACKAGE OUTLINE

16-lead mini-pack; plastic (SO-16; SOT-109A).

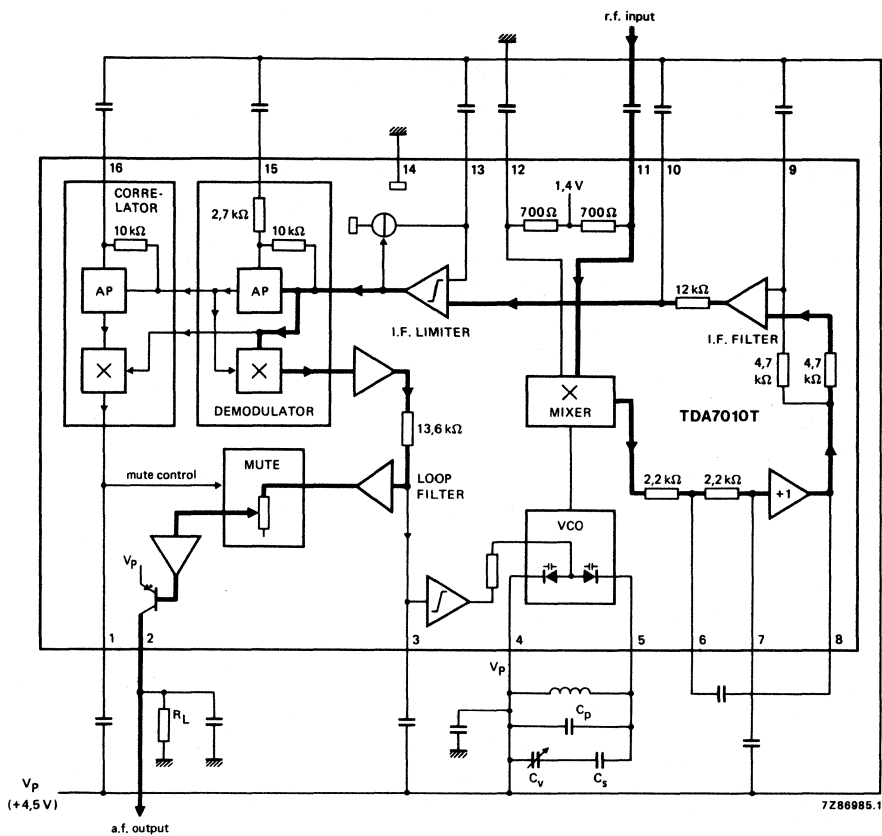


Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	$V_P$	max.	12 V
Oscillator voltage (pin 5)	$V_{6-5}$	$V_P - 0,5$ to $V_P + 0,5$	V
Total power dissipation			see derating curve Fig. 2
Storage temperature range	$T_{stg}$		-55 to +150 °C
Operating ambient temperature range	$T_{amb}$		0 to +60 °C

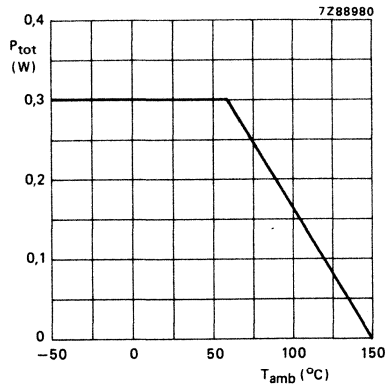


Fig. 2 Power derating curve.

**D.C. CHARACTERISTICS**

$V_P = 4,5$  V;  $T_{amb} = 25$  °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	$V_P$	2,7	4,5	10	V
Supply current at $V_P = 4,5$ V	$I_P$	—	8	—	mA
Oscillator current (pin 5)	$I_5$	—	280	—	μA
Voltage at pin 12	$V_{12-14}$	—	1,35	—	V
Output current at pin 2	$I_2$	—	60	—	μA
Voltage at pin 2; $R_L = 22$ kΩ	$V_{2-14}$	—	1,3	—	V



## A.C. CHARACTERISTICS

$V_p = 4,5 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; measured in Fig. 4 (mute switch open, enabled);  $f_{rf} = 96 \text{ MHz}$  (tuned to max. signal at  $5 \text{ } \mu\text{V}$  e.m.f.) modulated with  $\Delta f = \pm 22,5 \text{ kHz}$ ;  $f_m = 1 \text{ kHz}$ ;  $EMF = 0,2 \text{ mV}$  (e.m.f. voltage at a source impedance of  $75 \text{ } \Omega$ ); r.m.s. noise voltage measured unweighted ( $f = 300 \text{ Hz}$  to  $20 \text{ kHz}$ ); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for $-3 \text{ dB}$ limiting; muting disabled	EMF	—	1,5	—	$\mu\text{V}$
for $-3 \text{ dB}$ muting	EMF	—	6	—	$\mu\text{V}$
for $S/N = 26 \text{ dB}$	EMF	—	5,5	—	$\mu\text{V}$
Signal handling (e.m.f. voltage) for $THD < 10\%$ ; $\Delta f = \pm 75 \text{ kHz}$	EMF	—	200	—	mV
Signal-to-noise ratio	S/N	—	60	—	dB
Total harmonic distortion at $\Delta f = \pm 22,5 \text{ kHz}$	THD	—	0,7	—	%
at $\Delta f = \pm 75 \text{ kHz}$	THD	—	2,3	—	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: $f_m = 1 \text{ kHz}$ ; $\Delta f = \pm 75 \text{ kHz}$ AM signal: $f_m = 1 \text{ kHz}$ ; $m = 80\%$	AMS	—	50	—	dB
Ripple rejection ( $\Delta V_p = 100 \text{ mV}$ ; $f = 1 \text{ kHz}$ )	RR	—	10	—	dB
Oscillator voltage (r.m.s. value) at pin 5	V5-4(rms)	—	250	—	mV
Variation of oscillator frequency with supply voltage ( $\Delta V_p = 1 \text{ V}$ )	$\Delta f_{osc}$	—	60	—	kHz/V
Selectivity	S+300	—	43	—	dB
	S-300	—	28	—	dB
A.F.C. range	$\Delta f_{rf}$	—	$\pm 300$	—	kHz
Audio bandwidth at $\Delta V_o = 3 \text{ dB}$ measured with pre-emphasis ( $t = 50 \text{ } \mu\text{s}$ )	B	—	10	—	kHz
A.F. output voltage (r.m.s. value) at $R_L = 22 \text{ k}\Omega$	$V_o(\text{rms})$	—	75	—	mV
Load resistance at $V_p = 4,5 \text{ V}$	$R_L$	—	—	22	$\text{k}\Omega$
at $V_p = 9,0 \text{ V}$	$R_L$	—	—	47	$\text{k}\Omega$

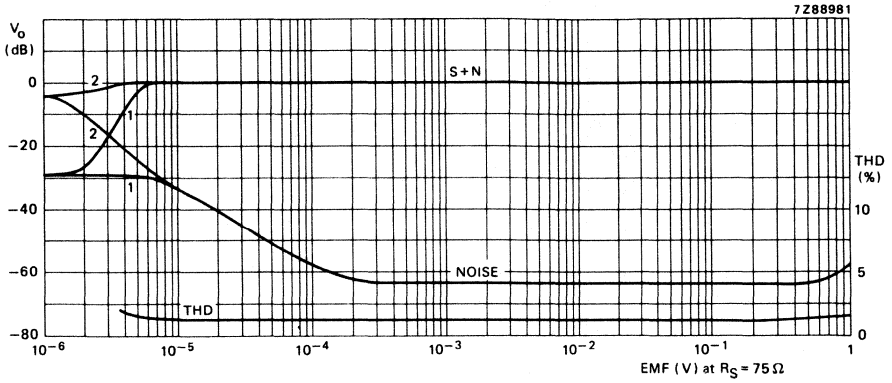


Fig. 3 A.F. output voltage ( $V_O$ ) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance ( $R_S$ ) of  $75 \Omega$ : (1) muting system enabled; (2) muting system disabled.

Conditions:  $0 \text{ dB} = 75 \text{ mV}$ ;  $f_{rf} = 96 \text{ MHz}$ .  
 for S + N curve:  $\Delta f = \pm 22,5 \text{ kHz}$ ;  $f_m = 1 \text{ kHz}$ .  
 for THD curve:  $\Delta f = \pm 75 \text{ kHz}$ ;  $f_m = 1 \text{ kHz}$ .

Notes

1. The muting system can be disabled by feeding a current of about  $20 \mu\text{A}$  into pin 1.

DEVELOPMENT SAMPLE DATA



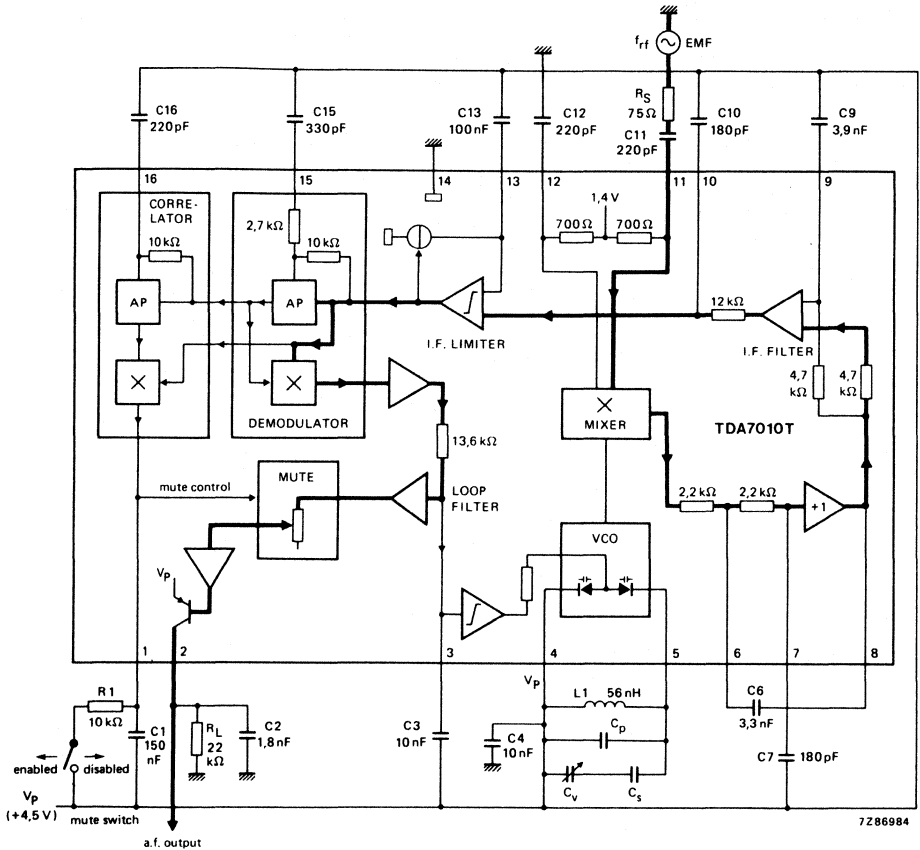


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

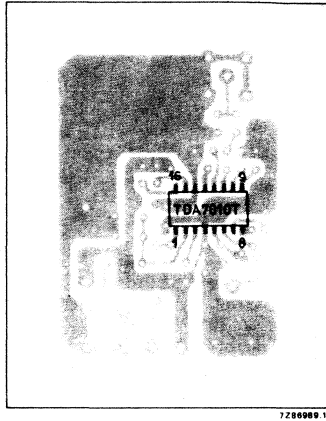


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

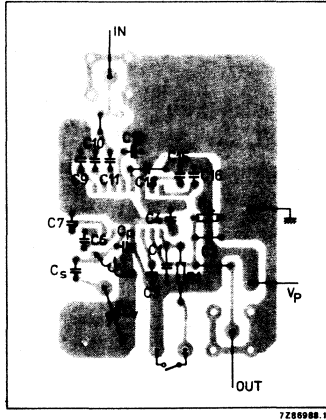


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.





## AM CAR RADIO RECEIVER CIRCUIT

The TEA5550 is an a.m. radio circuit, primarily intended for use in car radios. The IC can reduce the costs in a car radio due to the following features:

- minimum periphery
- no extra r.f.-prestage is necessary
- ceramic i.f. filter is used
- simple on/off switching method allows inexpensive band switching in a.m./f.m. radios

The TEA5550 incorporates the following functions:

- a double balanced mixer with large signal handling range and common mode rejection properties
- a 'one-pin' oscillator, permitting the use of variable capacitance diode tuning
- an i.f. amplifier, designed for ceramic filters
- an a.m. envelope detector
- a.g.c. stages
- a voltage stabilizer, for supplying the internal circuit current and an external current up to 20 mA
- a simple d.c. switch for a.m./f.m. radios

### QUICK REFERENCE DATA

Supply voltage range; unstabilized (pin 8)	$V_p$		10,2 to 18 V
Supply voltage; stabilized (pin 9)*	$V_{stab}$	typ.	7,5 to 9 V
Ambient temperature	$T_{amb}$	typ.	25 °C
Supply voltage (pin 8)	$V_p$	typ.	14,4 V
R.F. condition: $f_i = 1$ MHz; $m = 0,3$ ; $f_m = 1$ kHz			
-----			
R.F. input voltage (pin 1)			
$V_o = 30$ mV	$V_i$	typ.	4 $\mu$ V
S/N = 26 dB	$V_i$	typ.	16 $\mu$ V
S/N = 46 dB	$V_i$	typ.	160 $\mu$ V
A.F. output voltage (pin 10)			
$V_i = 10$ mV	$V_o$	typ.	180 mV
Total harmonic distortion over most of the a.g.c. range; $m = 0,8$	THD	typ.	1,2 %
R.F. signal handling			
THD = 10%; $m = 0,8$	$V_i$	typ.	400 mV
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference $V_{i1} = 200$ mV)	$V_{i1}/V_{i2}$	typ.	86 dB

\* Pins 8 and 9 have to be short-circuited externally.

### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

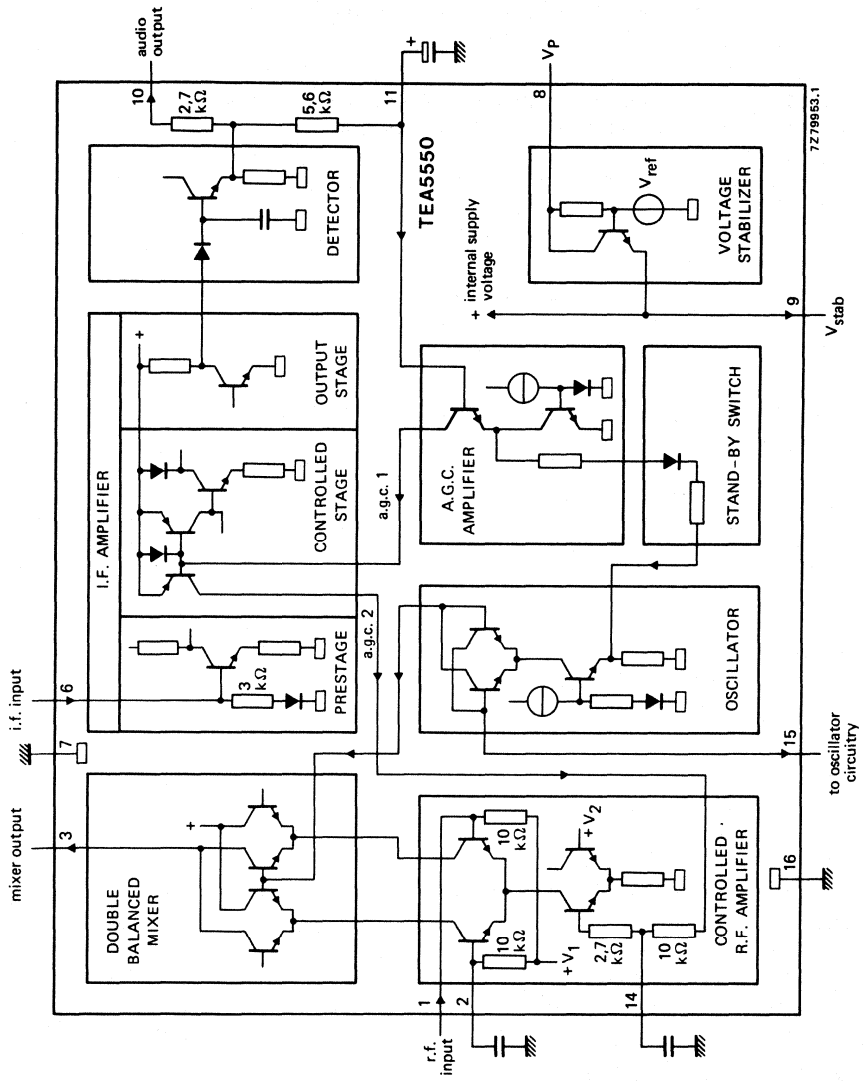


Fig. 1 Block diagram.

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages			
pin 8	$V_P = V_{8-16}$	max.	24 V
pin 3	$V_{3-16}$	max.	24 V
Non-repetitive peak output current (pin 9)	$I_{gSM}$	max.	100 mA
Total power dissipation	$P_{tot}$	max.	1100 mW
Storage temperature	$T_{stg}$		-65 to +150 °C
Operating ambient temperature	$T_{amb}$		-30 to +85 °C

**Note**

Pins 4, 5, 12 and 13 are not allowed to be connected.

**D.C. CHARACTERISTICS** at  $V_i = 0$  $V_P = 14,4$  V;  $T_{amb} = 25$  °C; measured in Fig. 2

Supply voltage range (unstabilized)*	$V_P$		10,2 to 18 V
Voltage at pin 9; $-I_g = 0$	$V_{9-16} = V_{stab}$	typ.	8,7 V 8 to 9,2 V
Change in stabilization voltage (pin 9)			
at $-I_g = 0$ to 20 mA	$\Delta V_{9-16} = \Delta V_{stab}$	typ.	50 mV
at $V_P = 10,2$ to 14,4 V	$\Delta V_{9-16} = \Delta V_{stab}$	typ.	300 mV
Voltage at pin 10	$V_{10-16}$	typ.	1,1 V
Voltage at pins 1 and 2	$V_{1-16} = V_{2-16}$	typ.	5,0 V
Voltage at pin 15	$V_{15-16}$	typ.	$V_{stab}$
Total supply current; $-I_g = 0$	$I_{tot}$	typ.	20 mA
Current drain			
pin 3	$I_3$	typ.	1 mA
pin 15	$I_{15}$	typ.	0,2 mA
Current supplied from pin 9	$-I_g$	<	20 mA
Power consumption; $-I_g = 0$	P	typ.	300 mW

\* A stabilized supply voltage of 7,5 to 9 V can also be applied at pin 9 (pin 8 short-circuited to pin 9).

## A.C. CHARACTERISTICS

$V_p = 14,4 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; r.f. condition:  $f_i = 1 \text{ MHz}$ ,  $m = 0,3$ ,  $f_m = 1 \text{ kHz}$ ; transfer impedance of the i.f. filter  $Z_{tr} = v_6/i_3 = 850 \text{ } \Omega$  (loaded with  $3 \text{ k}\Omega$ ); measured in Fig. 2; unless otherwise specified

R.F. input voltage; $V_o = 30 \text{ mV}$	$V_i$		1,5 to 6,5 $\mu\text{V}$
R.F. sensitivity at $R_S = 25 \text{ } \Omega$ for:			
$S + N/N = 6 \text{ dB}$	$V_i$	typ.	1,3 $\mu\text{V}$
$S + N/N = 20 \text{ dB}$	$V_i$	typ.	8 $\mu\text{V}$
$S + N/N = 26 \text{ dB}$	$V_i$	}	typ. 16 $\mu\text{V}$
$S + N/N = 46 \text{ dB}$	$V_i$		< 20 $\mu\text{V}$
$S + N/N = 50 \text{ dB}$	$V_i$	typ.	160 $\mu\text{V}$
	$V_i$	typ.	350 $\mu\text{V}$
Input conductance at pin 1			
$V_i = 0,1 \text{ mV}$	$g_{ie}$	typ.	0,2 mS
$V_i = 100 \text{ mV}$	$g_{ie}$	typ.	0,1 mS
Input conductance at pin 6	$g_{ie}$	typ.	0,3 mS
Output capacitance at pin 15	$C_{oe}$	typ.	20 pF
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference $V_{i1} = 200 \text{ mV}$ )	$V_{i1}/V_{i2}$	typ.	86 dB
A.F. output voltage			
$V_i = 10 \text{ mV}$	$V_o$	>	140 mV
		typ.	180 mV
Spread of a.f. output voltage	$\Delta V_o$	typ.	$\pm 2 \text{ dB}$
A.F. output impedance (pin 10)	$ Z_o $	typ.	2,7 k $\Omega$
Total harmonic distortion at $m = 0,8$			
$V_i = 16 \text{ } \mu\text{V}$	THD	<	2,5 %
over most of the a.g.c. range (see also Figs 3 and 10)	THD	typ.	1,2 %
$V_i = 25 \text{ mV}$	THD	typ.	3,5 %
R.F. signal handling capability			
THD = 10%; $m = 0,8$	$V_i$	>	350 mV
		typ.	400 mV
I.F. suppression at $V_o = 30 \text{ mV}$	$\alpha$	>	20 dB*
		typ.	35 dB*
Oscillator voltage			
$V_{9-16} = 8 \text{ V}$ ; $f_{osc} = 1468 \text{ kHz}$	$V_{15-8}$	typ.	250 mV
		<	300 mV

\*  $\alpha = 20 \log \frac{V_{ia}}{V_{ib}}$ , where:  $V_{ia}$  is input voltage at  $f = 468 \text{ kHz}$  and  $V_{ib}$  is input voltage at  $f = 1 \text{ MHz}$ .

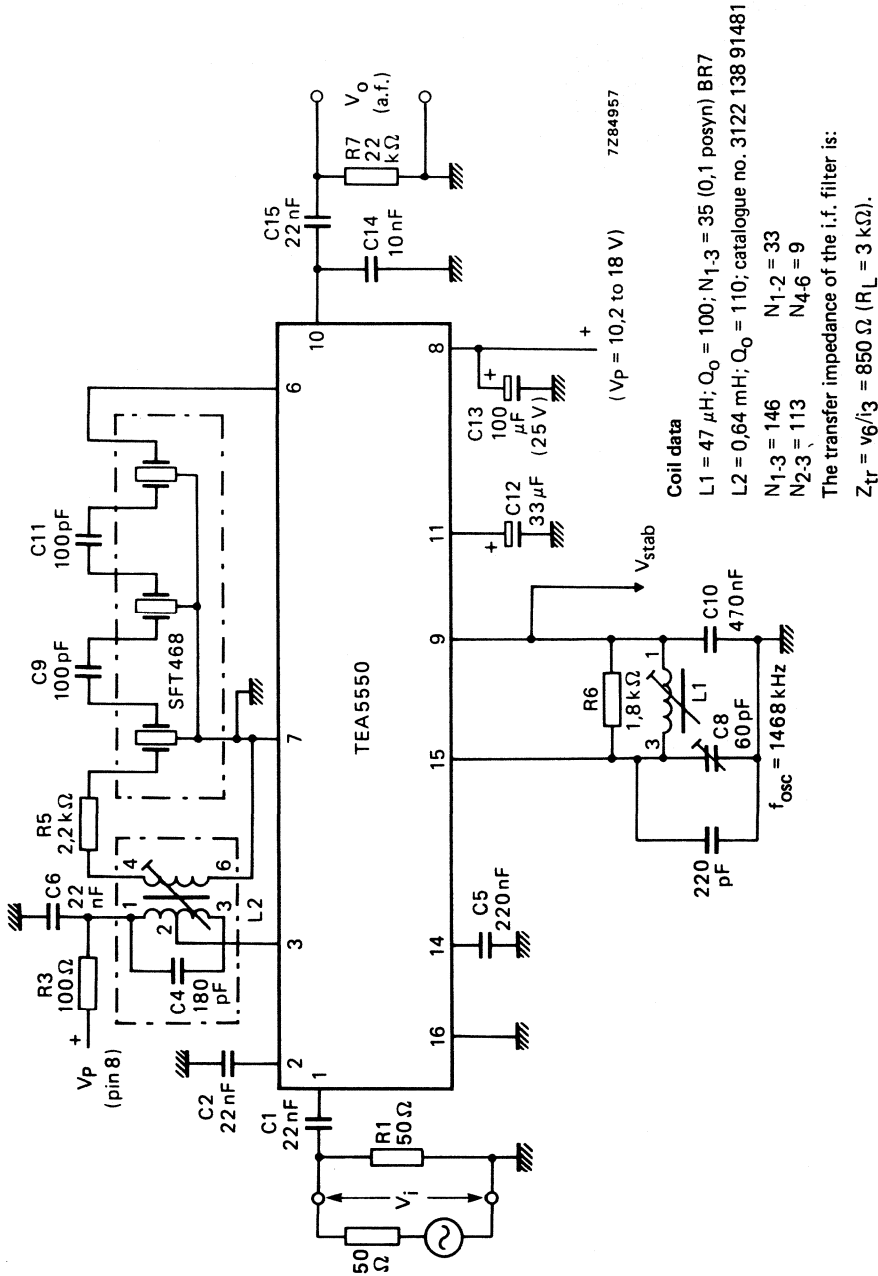


Fig. 2 AM test circuit.



## APPLICATION INFORMATION

Figures 4 and 7 show the circuit diagrams of single-tuned and double-tuned AM channels respectively, using the TEA5550 and an r.f.-tuning unit (type ALPS). The i.f. filter consists of a single-tuned coil in combination with a ceramic filter (type SFT468).

**Typical performance** (measured in Figs 4 and 7)

$V_P = 14,4 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; aerial signal conditions:  $f_o = 1 \text{ MHz}$ ;  $m = 0,3$ ;  $f_m = 1 \text{ kHz}$  (dummy aerial as shown in Figs 4 and 7)

		Fig. 4 single-tuning	Fig. 6 double-tuning	
R.F. input voltage for:				
S + N/N = 6 dB	$V_i$	4	4	$\mu\text{V}$
S + N/N = 26 dB	$V_i$	47	49	$\mu\text{V}$
A.F. output voltage ( $R_L = R_6 = 22 \text{ k}\Omega$ )				
$V_i = 1 \text{ mV}$	$V_o$	160	160	mV
Signal-to-noise ratio				
$V_i = 1 \text{ mV}$	S/N	> 50	> 50	dB
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference $V_{i1} = 200 \text{ mV}$ ); see Figs 3 and 10	$V_{i1}/V_{i2}$	88	88	dB
R.F. signal handling capability THD < 10%; $m = 0,8$ ; see Figs 3 and 10	$V_i$	1,5	1,5	V
Total harmonic distortion (over most of the a.g.c. range); $m = 0,8$ ; see Figs 3 and 10	THD	1,2	1,2	%
Oscillator voltage measured across the tank circuit	$V_{\text{osc}}$	250	250	mV
Total selectivity (r.f. and i.f.)	$S_g$	44	46	dB
Total bandwidth (r.f. and i.f.)	$B_{3\text{dB}}$	4,1	4,4	kHz
I.F. suppression at $V_i = 20 \mu\text{V}$ tuned frequency = 600 kHz	$\alpha$	55	75	dB
= 1600 kHz	$\alpha$	58	85	dB
Image rejection at $V_i = 20 \mu\text{V}$ tuned frequency = 600 kHz		50	72	dB
= 1000 kHz		46	68	dB
= 1400 kHz		42	64	dB
Whistle at $V_i = 5 \text{ mV}$				
2 x i.f.-tweet		-40	-40	dB
3 x i.f.-tweet		-48	-48	dB

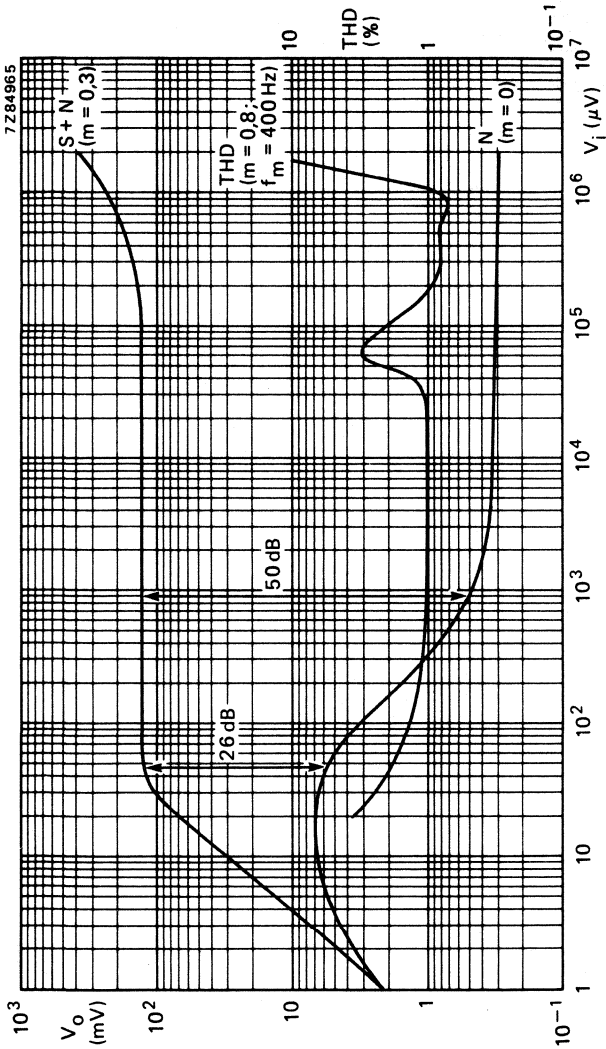
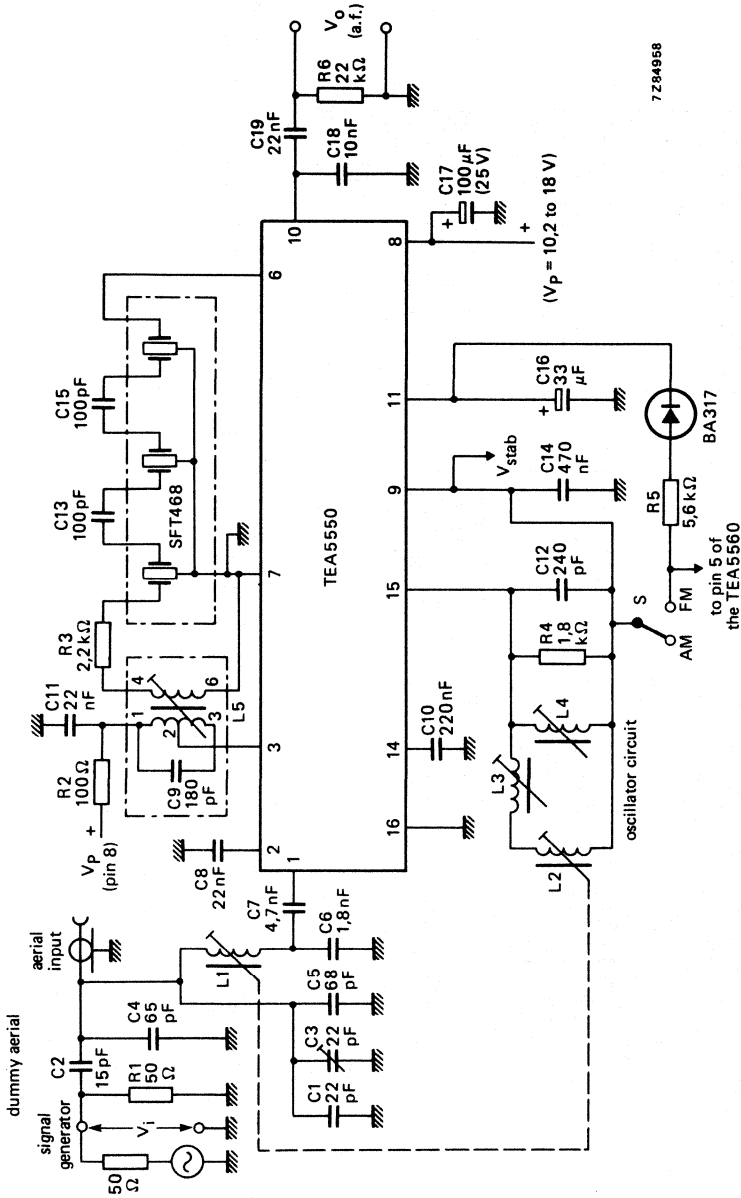


Fig. 3 Typical signal and noise output voltages ( $V_o$  is a.f. output voltage) as a function of the input voltage  $V_i$ . Also shown is the total harmonic distortion (THD). These curves are for a single-tuned AM channel; the dummy aerial is as shown in Fig. 4;  $f_o = 1$  MHz;  $f_m = 1$  kHz;  $m = 0,3$  (unless otherwise specified).





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Fig. 4 Typical application circuit diagram for a single-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Fig. 5 and 6.

- Coil data: L1, L2 = tuning coils, ALPS unit MMK IIE11 (for coil connections see Fig. 5)
- L3 = trimming coil (4,7 μH); catalogue number 3122 138 27460
- L4 = padding coil (200 μH); catalogue number 3111 118 23510
- L5 = i.f. coil; catalogue number 3122 138 91481



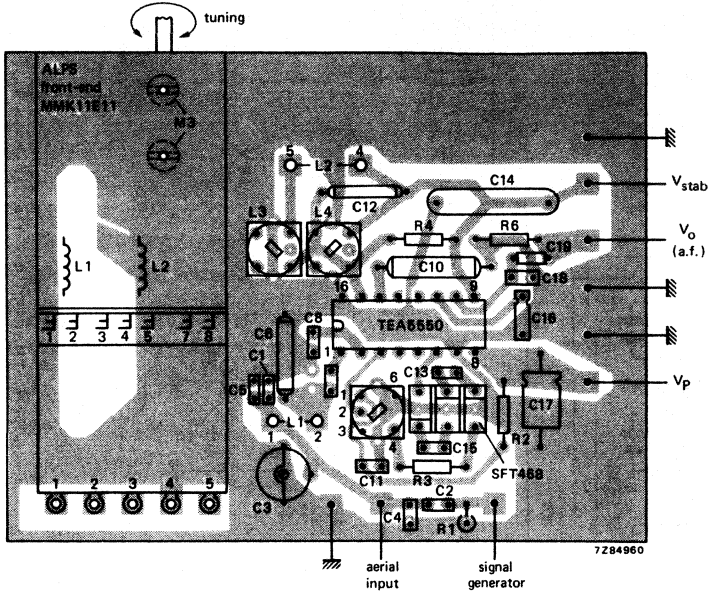


Fig. 5 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 4.

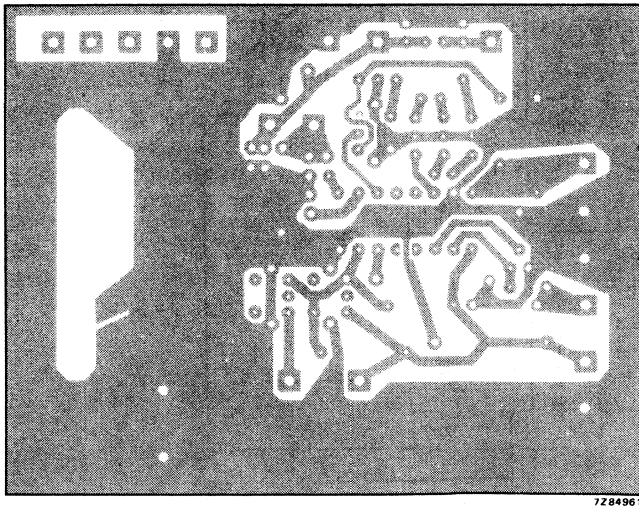


Fig. 6 Printed-circuit board showing track side.

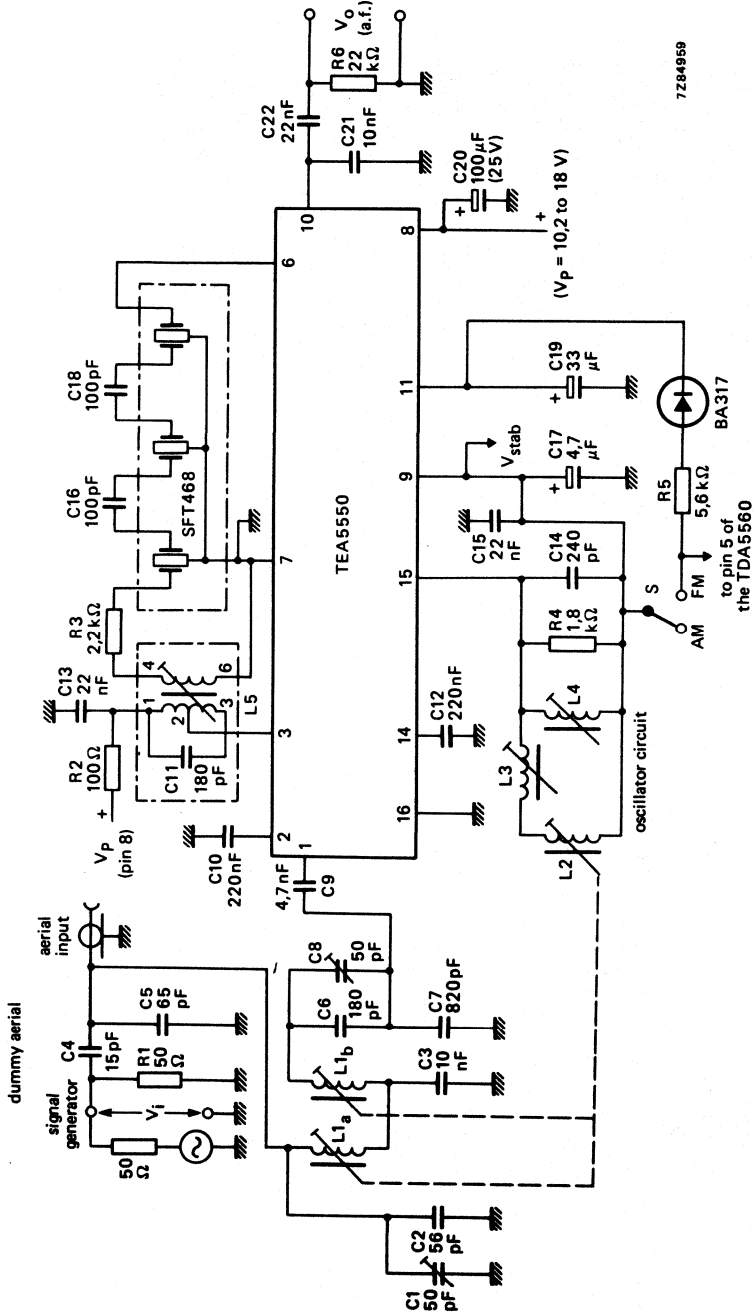


Fig. 7 Typical application circuit diagram for a double-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Figs 8 and 9.

- Coil data: L1<sub>a</sub>, L1<sub>b</sub>, L2 = tuning coils, ALPS unit MIMK IIEIII (for coil connections see Fig. 8)  
 L3 = trimming coil (4.7 μH); catalogue number 3122 138 27460  
 L4 = padding coil (200 μH); catalogue number 3111 118 23510  
 L5 = i.f. coil; catalogue number 3122 138 91481

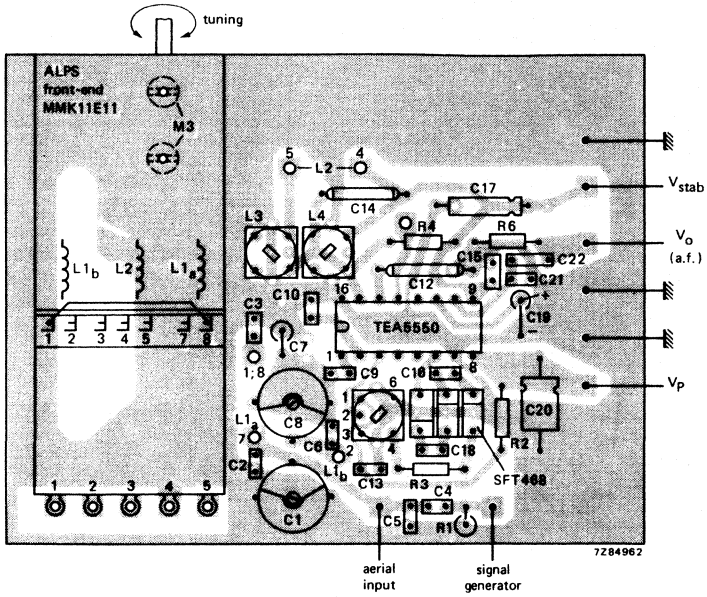


Fig. 8 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 7.

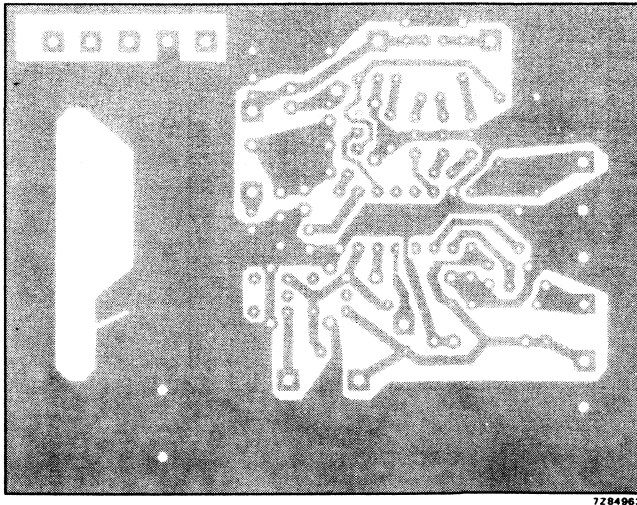


Fig. 9 Printed-circuit board showing track side.

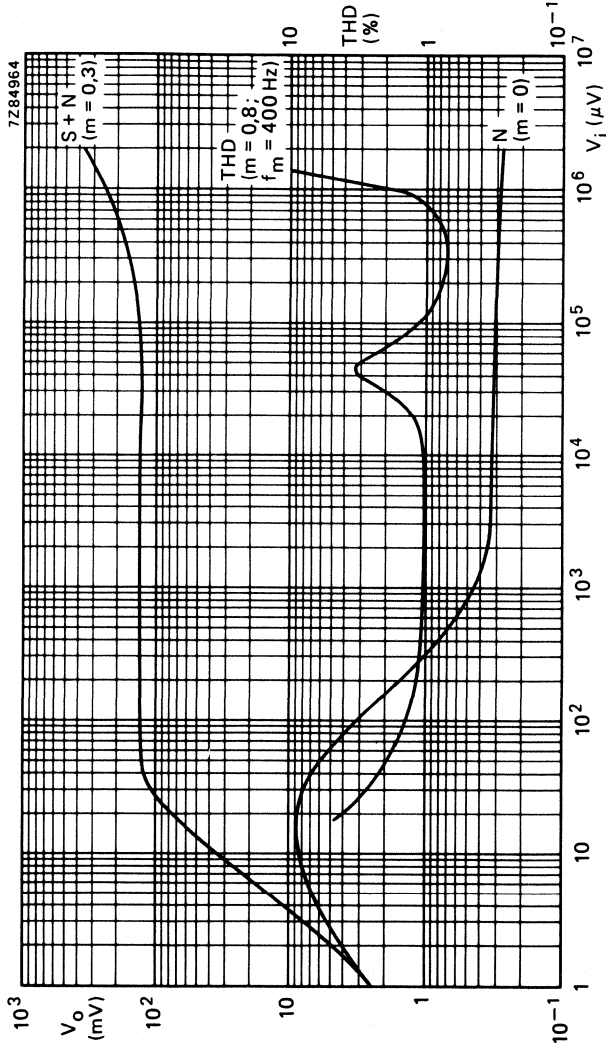


Fig. 10 Typical signal and noise output voltages ( $V_o$  is a.f. output voltage) as a function of the input voltage  $V_i$ . Also shown is the total harmonic distortion (THD). These curves are for a double-tuned AM channel; the dummy aerial is shown in Fig. 7;  $f_o = 1 \text{ MHz}$ ;  $f_m = 1 \text{ kHz}$ ;  $m = 0,3$  (unless otherwise specified).

## FM/IF SYSTEM

### GENERAL DESCRIPTION

The TEA5560 is a monolithic integrated FM/IF system circuit, intended for car radios and home-receivers equipped with a ratio detector.

The system incorporates the following functions:

- a three-stage i.f. limiting amplifier
- a 15 dB field-strength dependent muting circuit
- a field-strength dependent d.c. voltage for e.g.:  
mono/stereo switching  
channel separation control of a stereo decoder  
an indicator ( $I_{\max} \leq 1 \text{ mA}$ )
- standby ON/OFF switching circuit
- a voltage stabilizer, for the internal circuit current and an external current up to 15 mA
- adjustable gain ( $\Delta G = 15 \text{ dB}$ )

### QUICK REFERENCE DATA

Supply voltage range (pin 6)	$V_p$		10,2 to 18 V
Ambient temperature	$T_{\text{amb}}$	typ.	25 °C
Supply voltage (pin 6)	$V_p$	typ.	14,4 V
Frequency	$f_o$		10,7 MHz
-----			
Sensitivity (3 dB limiting)	$V_i$	typ.	150 $\mu\text{V}$
Signal-to-noise ratio for $V_i = 10 \text{ mV}$	S/N	typ.	80 dB
A.F. output voltage at $\Delta f = \pm 22,5 \text{ kHz}$	$V_o$	typ.	200 mV
Total harmonic distortion; $\Delta f = \pm 22,5 \text{ kHz}$	THD	typ.	0,3 %
A.M. suppression			
AM signal: $m = 0,3$ ; $f_m = 1 \text{ kHz}$			
FM signal: $\Delta f = \pm 22,5 \text{ kHz}$ ; $f_m = 70 \text{ Hz}$ for $V_i = 1 \text{ mV}$	AMS	typ.	50 dB

### PACKAGE OUTLINE

9-lead SiL; plastic (SOT-142). The tab (on top of the package) is connected to pin 9.

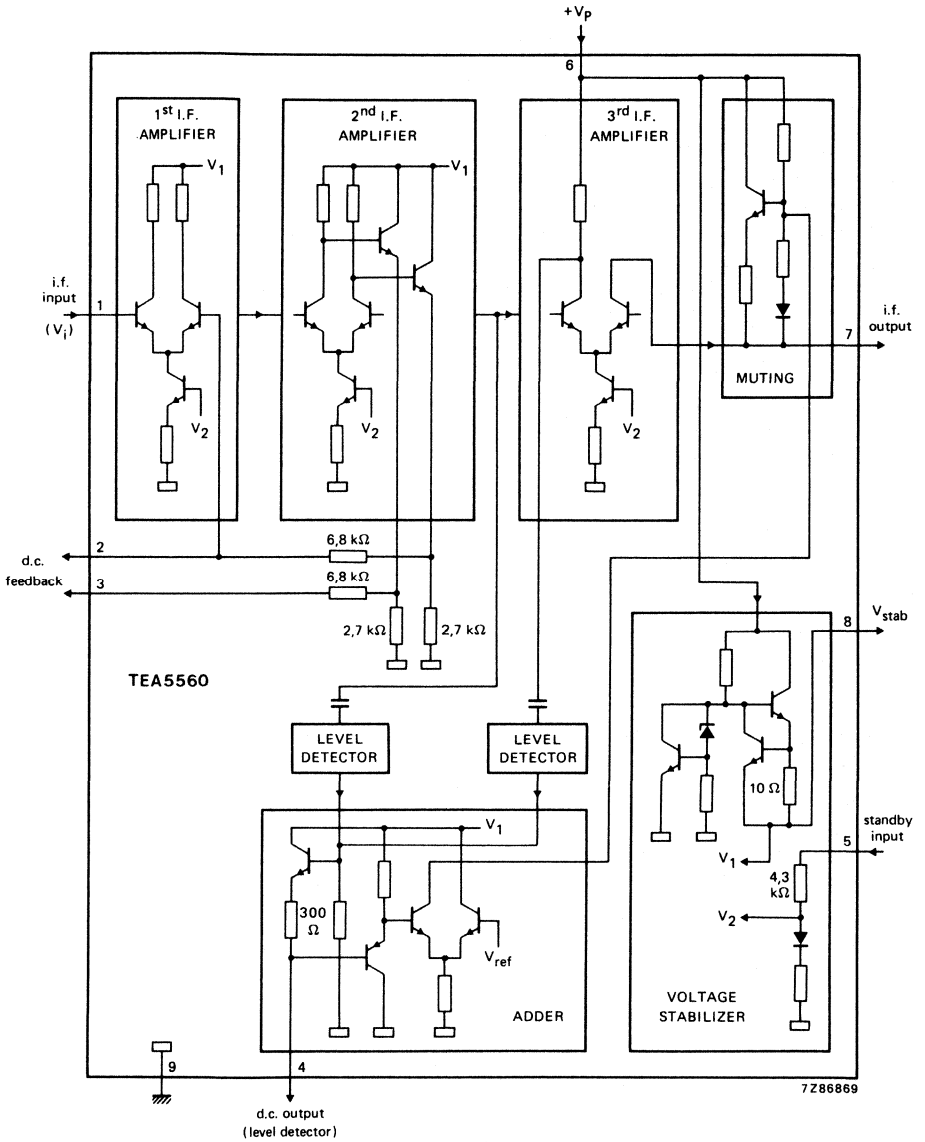


Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages			
pin 6	$V_P = V_{6-9}$	max.	24 V
pin 7	$V_{7-9}$	max.	24 V
Voltage at pin 4	$V_{4-9}$	max.	6 V
Voltage at pin 5	$V_{5-9}$	max.	9 V
Non-repetitive peak output current (pin 8)	$-I_{8SM}$	max.	100 mA
Total power dissipation	$P_{tot}$	max.	1000 mW
Storage temperature range	$T_{stg}$		-55 to +150 °C
Operating ambient temperature range	$T_{amb}$		-30 to +85 °C

**THERMAL RESISTANCE**

From junction to ambient (in free air)	$R_{th\ j-amb}$	=	75 K/W
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## D.C. CHARACTERISTICS

$V_p = 14,4 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; measured in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 6)</b>					
Supply voltage *	$V_p = V_{6-9}$	10,2	14,4	18,0	V
<b>Voltages</b>					
at pin 8; $-I_g = 0$ **	$V_{8-9}$	7,5	8,0	8,5	V
at pin 8 when $-I_g$ increases from 0 to 15 mA	$\Delta V_{8-9}$	—	200	300	mV
at pin 8 when $V_p$ reduces from 14,4 V to 10,2 V	$\Delta V_{8-9}$	—	—	1,0	V
at pin 8 when $V_p$ increases from 14,4 V to 18,0 V	$\Delta V_{8-9}$	—	—	200	mV
at pin 4 (level detector)	$V_{4-9}$	—	—	100	mV
at pins 1, 2 and 3	$V_{1,2,3-9}$	—	2,4	—	V
<b>Currents</b>					
Total supply current; $-I_g = 0$	$I_{tot}$	15	20	30	mA
Current supplied from pin 8	$-I_g$	—	—	15	mA
Stand-by current; $V_{5-9} = 0$	$I_{sb}$	8	11	14	mA
Current into pin 5	$I_5$	1,0	1,5	2,0	mA
Current into pin 7	$I_7$	—	3,0	—	mA
<b>Power consumption</b>					
at $-I_g = 0$	P	—	300	—	mW

\* A stabilized supply voltage of 7 to 9 V can also be applied at pin 5 and 6 (linked); for this application pin 8 must not be connected.

\*\* The temperature coefficient of the stabilized voltage at pin 8 is typical  $-2,3 \text{ mV/K}$ .



## A.C. CHARACTERISTICS

$V_P = 14,4 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ;  $V_i = 1 \text{ mV}$ ;  $f_o = 10,7 \text{ MHz}$ ;  $\Delta f = \pm 22,5 \text{ kHz}$ ;  $f_m = 1 \text{ kHz}$ ; measured in Fig. 2; unless otherwise specified

parameter	symlpl	min.	typ.	max.	unit
<b>I.F. part and ratio detector</b>					
Sensitivity					
at $-3 \text{ dB}$ before limiting (pin 1); (without muting) *	$V_i$	105	150	210	$\mu\text{V}$
Signal-to-noise S + N/S measured in a bandwidth of 60 Hz to 15 kHz					
at $V_i = 20 \mu\text{V}$	S/N	40	45	—	dB
at $V_i = 150 \mu\text{V}$	S/N	—	65	—	dB
at $V_i = 1 \text{ mV}$	S/N	—	78	—	dB
at $V_i = 10 \text{ mV}$	S/N	—	80	—	dB
<b>A.F. output voltage</b>					
$\Delta f = \pm 22,5 \text{ kHz}$	$V_o$	—	200	—	mV
$\Delta f = \pm 75 \text{ kHz}$	$V_o$	—	600	—	mV
<b>Total harmonic distortion</b>					
$\Delta f = \pm 22,5 \text{ kHz}$	THD	—	0,3	—	%
$\Delta f = \pm 75 \text{ kHz}$	THD	—	2,0	—	%
<b>AM suppression</b>					
$f_m = 1 \text{ kHz}$ ; $m = 0,3$ (for AM)					
$f_m = 70 \text{ kHz}$ ; $\Delta f = \pm 22,5 \text{ kHz}$ (for FM)					
at $V_i = 150 \mu\text{V}$	AMS	—	40	—	dB
at $V_i = 1 \text{ mV}$	AMS	—	50	—	dB
at $V_i = 10 \text{ mV}$	AMS	—	55	—	dB
<b>Level detector circuit</b>					
<b>D.C. output voltage (pin 4)</b>					
at $V_i = 200 \mu\text{V}$	$V_{4.9}$	—	1,9	—	V
at $V_i = 500 \mu\text{V}$	$V_{4.9}$	—	2,8	—	V
at $V_i = 1 \text{ mV}$	$V_{4.9}$	—	3,5	—	V
at $V_i = 3 \text{ mV}$	$V_{4.9}$	—	5,0	—	V
at $V_i = 10 \text{ mV}$	$V_{4.9}$	—	5,7	—	V
<b>Muting circuit (see also Fig. 5)</b>					
Change in output voltage at $V_i = 3 \mu\text{V}$ (with and without muting) *					
	$\alpha_{VO}$	10	15	—	dB
Input voltage at a change in output voltage of $\leq 1 \text{ dB}$ *					
( $V_i$ at $\alpha_{VO} \leq 1 \text{ dB}$ )	$V_i$	—	—	250	$\mu\text{V}$

\* With muting  $V_{4.9} < 0,3 \text{ V}$ ; without muting  $V_{4.9} = 1,2 \text{ to } 6 \text{ V}$ .

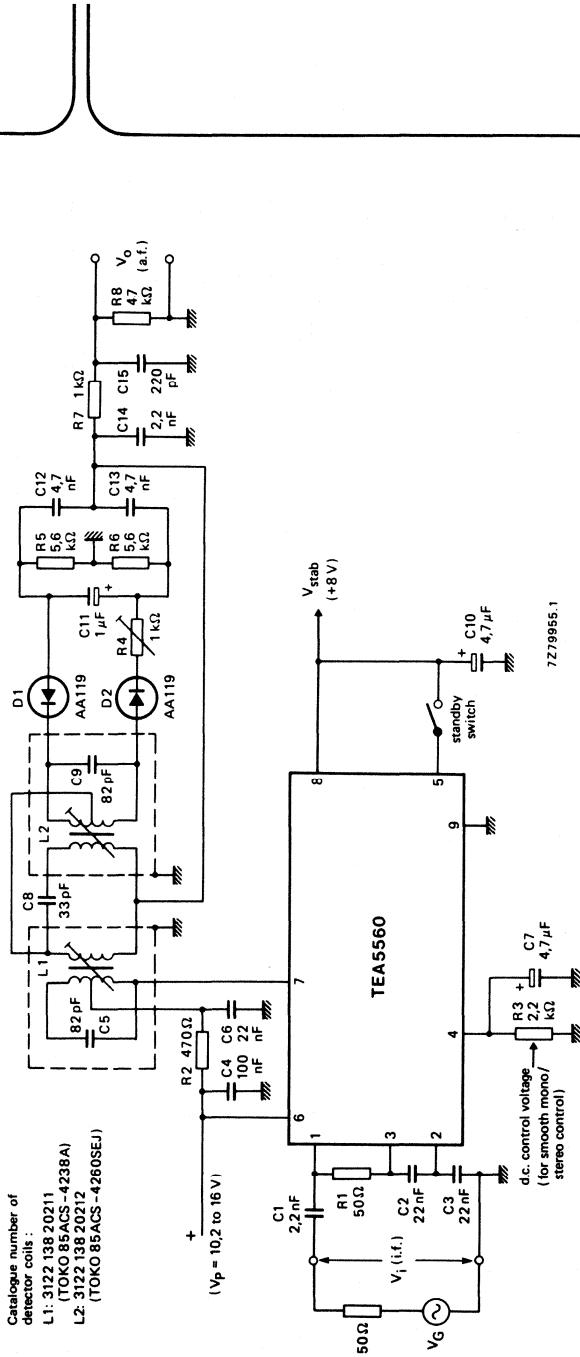


Fig. 2 FM test circuit.

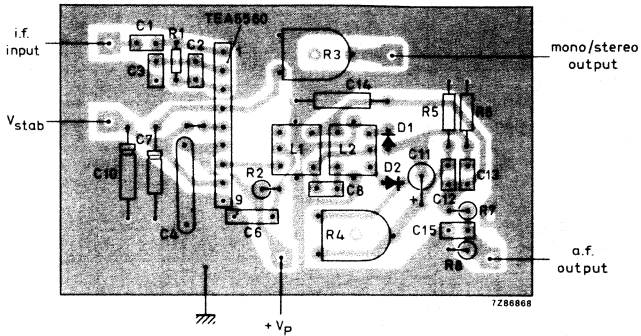


Fig. 3 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 2.

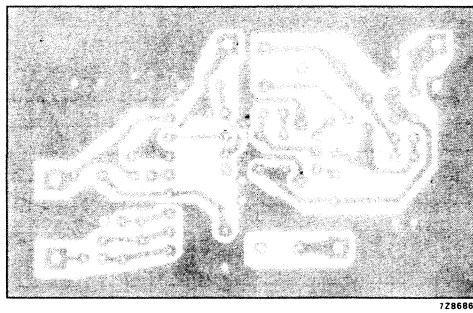
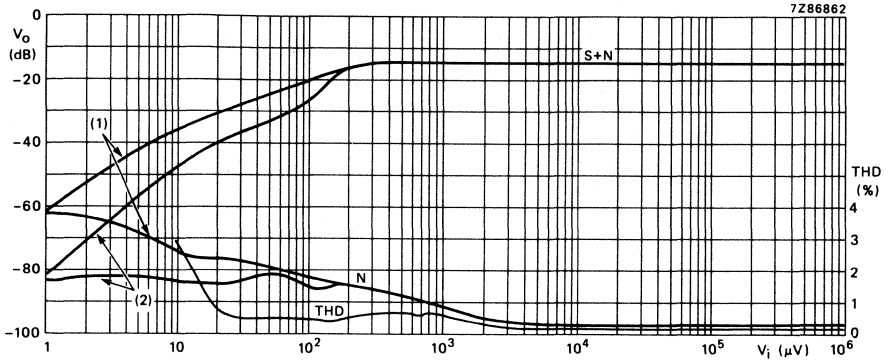


Fig. 4 Printed-circuit board showing track side.



- (1) Without muting.
- (2) With muting.

Fig. 5 A.F. output voltage ( $V_o$ ); reference level 0 dB = 1 V, and the total harmonic distortion (THD) as a function of the i.f. input voltage ( $V_i$ ). Measured in the test circuit Fig. 2 at  $\Delta f = \pm 22,5$  kHz;  $f_m = 1$  kHz.

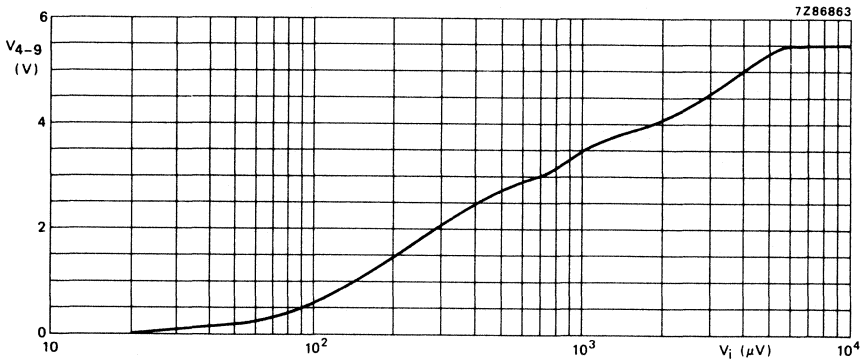
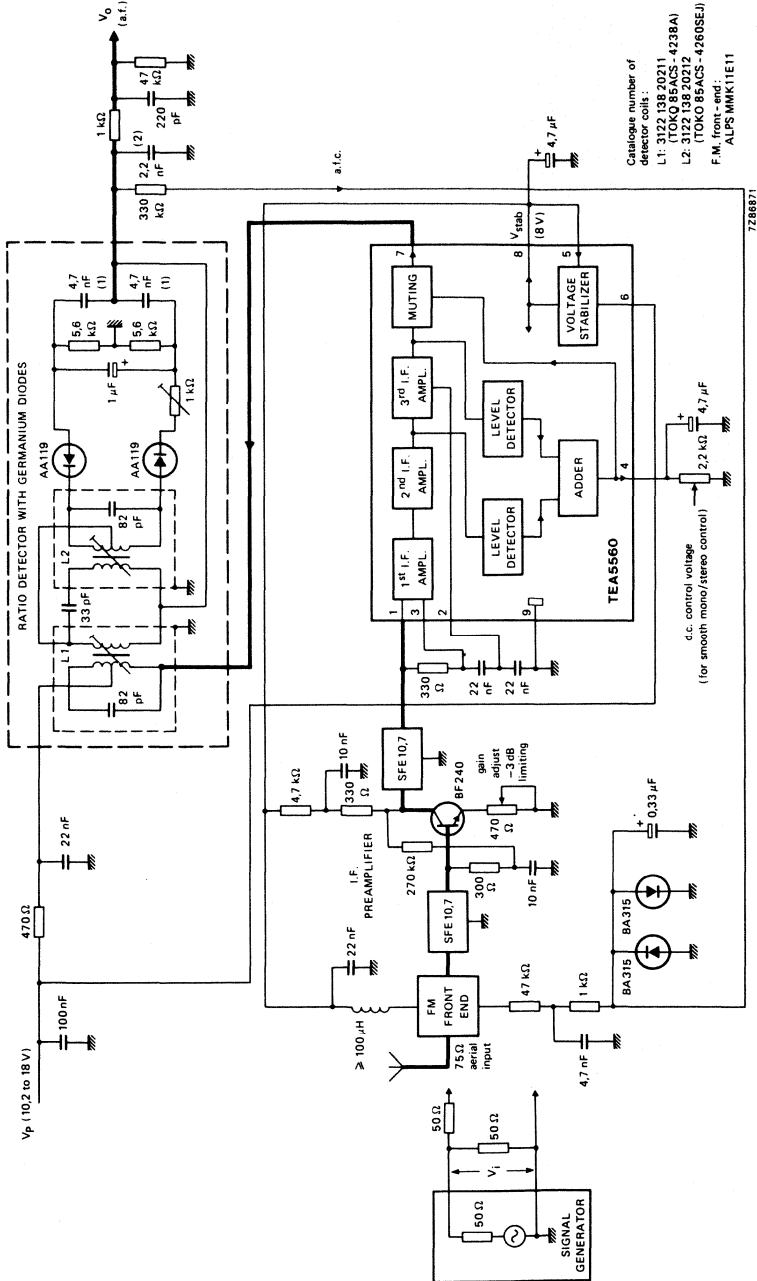


Fig. 6 Level detector d.c. output voltage (pin 4) as a function of the i.f. input voltage. Measured in test circuit Fig. 2.

APPLICATION INFORMATION



Catalogue number of detector coils:  
 L1: 3122 138 20211 (TOKO 85ACS-4238A)  
 L2: 3122 138 20212 (TOKO 85ACS-4260SEJ)  
 F.M. front-end: ALPS MINK11E11

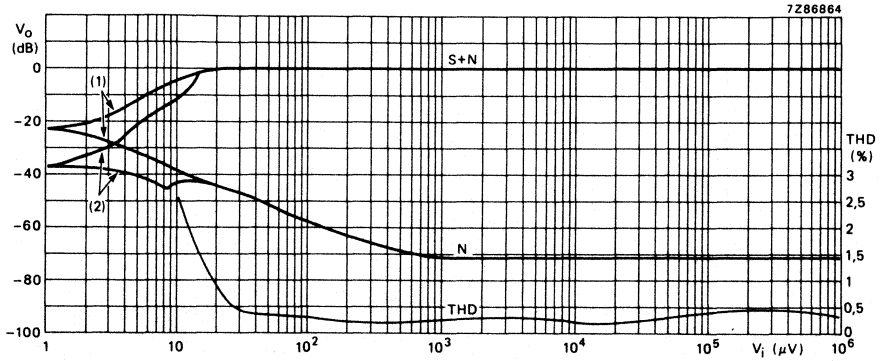
7288871

- (1) Stereo application 220 pF.
- (2) Stereo application 390 pF.

Fig. 7 FM channel for (car) radios using the TEA5560 and a ratio detector with AA119 germanium diodes.



APPLICATION INFORMATION (continued)



- (1) Without muting.
- (2) With muting.

Fig. 8 Signal and noise (S + N) and noise (N); reference level 0 dB = 200 mV, and the total harmonic distortion (THD) as a function of the aerial input voltage ( $V_i$ ). Measured in application circuit Fig. 7 at  $\Delta f = \pm 22,5$  kHz;  $f_m = 1$  kHz.

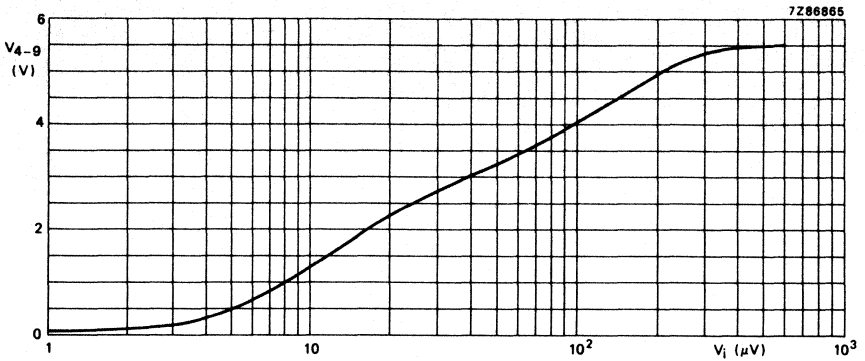
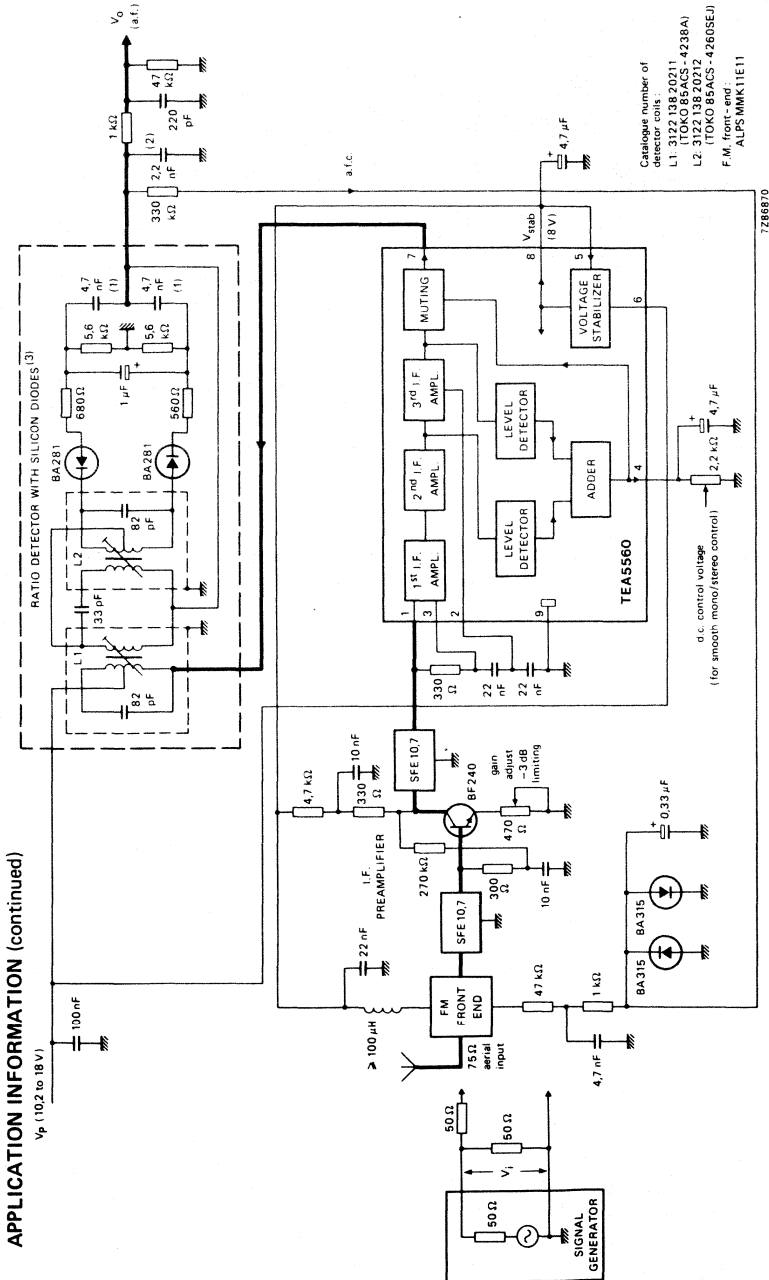


Fig. 9 Level detector d.c. output voltage (pin 4) as a function of the aerial input voltage. Measured in application circuit Fig. 7.



Catalogue number of detector ICs:  
 L1: TOKO 138 20211  
 L2: TOKO 85ACS - 4238A  
 L3: TOKO 138 20212  
 (TOKO 85ACS - 4260SEJ)  
 F.M. front-end:  
 ALP5MMK11E1

- (1) Stereo application 220 pF.
  - (2) Stereo application 390 pF.
  - (3) Further detailed information of using silicon diodes is available on request.
- Fig. 10 FM channel for (car) radios using the TEA5560 and a ratio detector with BA281 silicon diodes.



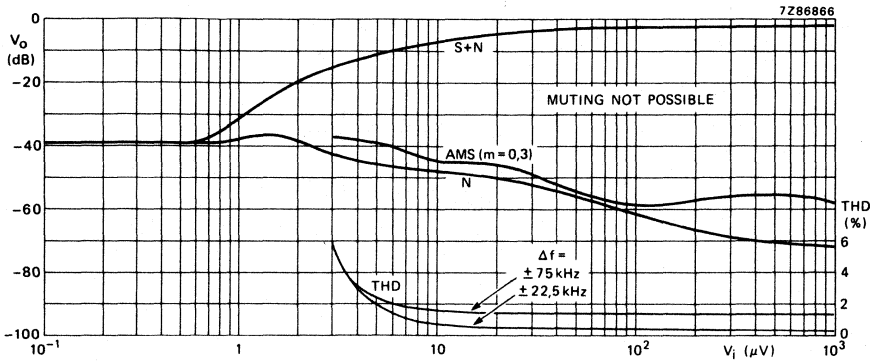


Fig. 11 Signal and noise (S + N) and noise (N); reference level 0 dB = 245 mV, AM suppression (AMS) and total harmonic distortion (THD) as a function of the aerial input voltage ( $V_i$ ). Measured in application circuit Fig. 10 at  $\Delta f = \pm 22,5$  kHz;  $f_m = 1$  kHz; for AM suppression  $m = 0,3$ ;  $\Delta f = \pm 22,5$  kHz.





## AM/FM RADIO RECEIVER CIRCUIT

### GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

### Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption ( $I_{TOT} = 6 \text{ mA}$ )
- Low voltage operation ( $V_P = 2,7$  to  $9 \text{ V}$ )
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to  $30 \text{ MHz}$
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

### QUICK REFERENCE DATA (at $T_{amb} = 25 \text{ }^\circ\text{C}$ )

Supply voltage	$V_P = V_{7-16}$	typ.	5,4 V
Supply current	$I_7$	typ.	6,2 mA
<b>AM performance (pin 2) for <math>m = 0,3</math></b>			
Sensitivity			
at $V_O = 10 \text{ mV}$	$V_i$	typ.	1,7 $\mu\text{V}$
at $S/N = 26 \text{ dB}$	$V_i$	typ.	16 $\mu\text{V}$
A.F. output voltage at $V_i = 1 \text{ mV}$	$V_O$	typ.	100 mV
Total harmonic distortion at $V_i = 1 \text{ mV}$	THD	typ.	0,5 %
<b>FM performance (pin 1) for <math>\Delta f = \pm 22,5 \text{ kHz}</math></b>			
limiting sensitivity, $-3 \text{ dB}$	$V_i$	typ.	110 $\mu\text{V}$
Signal-to-noise ratio for $V_i = 1 \text{ mV}$	S/N	typ.	65 dB
A.F. output voltage at $V_i = 1 \text{ mV}$	$V_O$	typ.	100 mV
Total harmonic distortion at $V_i = 1 \text{ mV}$	THD	typ.	0,3 %
AM suppression at $V_i = 10 \text{ mV}$	AMS	typ.	50 dB

### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

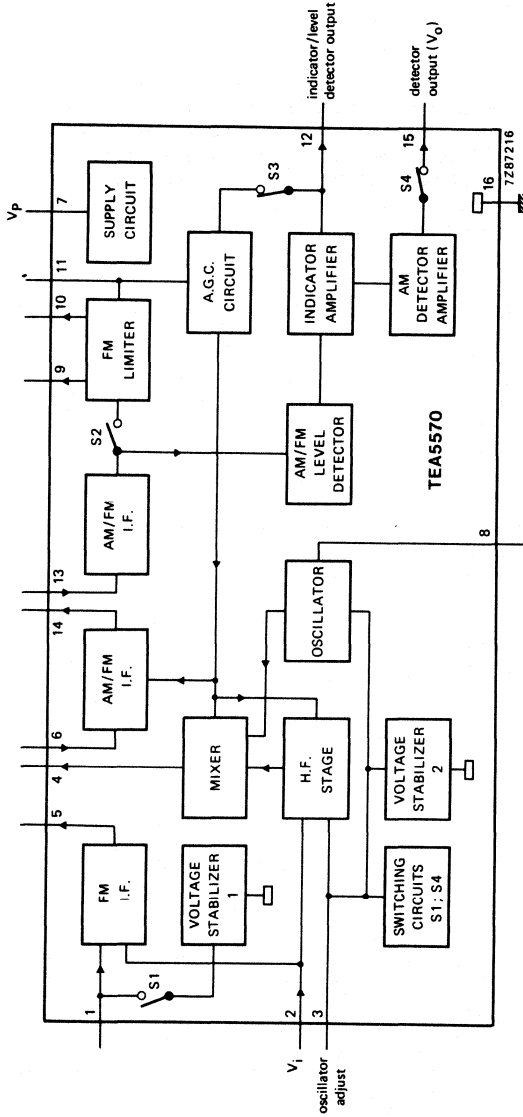


Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-16}$	max.	12 V
Voltage at pins 4, 5, 9 and 10 to pin 16 (ground)	$V_{n-16}$	max.	12 V
Voltage range at pin 8	$V_{8-16}$		$V_P \pm 0,5 V$
Current into pin 5	$I_5$	max.	3 mA
Total power dissipation	$P_{tot}$		see Fig. 2
Storage temperature range	$T_{stg}$		-55 to +150 °C
Operating ambient temperature range	$T_{amb}$		-30 to +85 °C

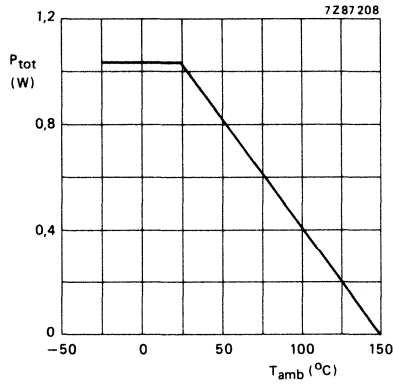


Fig. 2 Power derating curve.



## D.C. CHARACTERISTICS

$V_P = 6\text{ V}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply (pin 7)</b>					
Supply voltage (note 1)	$V_P = V_{7-16}$	2,4	5,4	9,0	V
<b>Voltages</b>					
at pin 1 (FM)	$V_{1-16}$	—	1,42	—	V
at pin 1; $-I_1 = 50\text{ }\mu\text{A}$ (FM)	$V_{1-16}$	—	1,28	—	V
at pins 2 and 3 (AM)	$V_{2,3-16}$	—	1,42	—	V
at pin 6	$V_{6-16}$	—	0,7	—	V
at pin 11	$V_{11-16}$	—	1,4	—	V
at pin 13	$V_{13-16}$	—	0,7	—	V
at pin 14	$V_{14-16}$	—	4,3	—	V
<b>Currents</b>					
Supply current	$I_7$	4,2	6,2	8,2	mA
Current supplied from pin 1 (FM)	$-I_1$	—	—	50	$\mu\text{A}$
Current supplied from pin 12	$-I_{12}$	—	—	20	$\mu\text{A}$
Current supplied from pin 15	$-I_{15}$	—	30	—	$\mu\text{A}$
Current into pin 4 (AM)	$I_4$	—	0,6	—	mA
Current into pin 5 (FM) (note 4)	$I_5$	—	0,35	—	mA
Current into pin 8 (AM)	$I_8$	—	0,3	—	mA
Current into pins 9, 10 (FM)	$I_{9,10}$	—	0,65	—	mA
Current into pin 14	$I_{14}$	—	0,4	—	mA
Power consumption	P	—	40	—	mW



## A.C. CHARACTERISTICS

## AM performance

$V_P = 6 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; r.f. condition:  $f_i = 1 \text{ MHz}$ ,  $m = 0,3$ ,  $f_m = 1 \text{ kHz}$ ; transfer impedance of the i.f. filter  $|Z_{\text{tr}}| = v_6/14 = 2,7 \text{ k}\Omega$ ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity (pin 2)					
at $V_O = 30 \text{ mV}$	$V_i$	3,5	5,0	7,0	$\mu\text{V}$
at $S + N/N = 6 \text{ dB}$	$V_i$	—	1,3	—	$\mu\text{V}$
at $S + N/N = 26 \text{ dB}$	$V_i$	—	16	20	$\mu\text{V}$
at $S + N/N = 50 \text{ dB}$	$V_i$	—	1	—	$\text{mV}$
Signal handling (THD $\leq 10\%$ at $m = 0,8$ )	$V_i$	200	—	—	$\text{mV}$
A.F. output voltage at $V_i = 1 \text{ mV}$	$V_O$	80	100	125	$\text{mV}$
Total harmonic distortion					
at $V_i = 100 \mu\text{V}$ to $100 \text{ mV}$ ( $m = 0,3$ )	THD	—	0,5	—	%
at $V_i = 2 \text{ mV}$ ( $m = 0,8$ )	THD	—	1,0	2,5	%
at $V_i = 200 \text{ mV}$ ( $m = 0,8$ )	THD	—	4,0	10	%
I.F. suppression at $V_O = 30 \text{ mV}$ (note 2)	$\alpha$	26	35	—	$\text{dB}$
Oscillator voltage (pin 8; note 3)					
at $f_{\text{osc}} = 1455 \text{ kHz}$	$V_{8-16}$	120	160	200	$\text{mV}$
Indicator current (pin 12) at $V_i = 1 \text{ mV}$	$I_{12}$	—	200	230	$\mu\text{A}$

## FM performance

$V_P = 6 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; i.f. condition:  $f_i = 10,7 \text{ MHz}$ ,  $\Delta f = \pm 22,5 \text{ kHz}$ ,  $f_m = 1 \text{ kHz}$ ; transfer impedance of the i.f. filter  $|Z_{\text{tr}}| = v_6/15 = 275 \Omega$ ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I.F. part					
I.F. sensitivity (adjustable; note 4)					
Input voltage					
at $-3 \text{ dB}$ before limiting	$V_i$	90	110	130	$\mu\text{V}$
at $S + N/N = 26 \text{ dB}$	$V_i$	—	6	—	$\mu\text{V}$
at $S + N/N = 65 \text{ dB}$	$V_i$	—	1	—	$\text{mV}$
A.F. output voltage at $V_i = 1 \text{ mV}$	$V_O$	80	100	125	$\text{mV}$
Total harmonic distortion at $V_i = 1 \text{ mV}$	THD	—	0,3	—	%
AM suppression (note 5)	AMS	—	50	—	$\text{dB}$
Indicator/level detector (pin 12)					
Indicator current	$I_{12}$	—	250	325	$\mu\text{A}$
D.C. output voltage					
at $V_i = 300 \mu\text{V}$	$V_{12-16}$	—	0,25	—	$\text{V}$
at $V_i = 2 \text{ mV}$	$V_{12-16}$	—	1,0	—	$\text{V}$
AM to FM switch					
Switching current at $V_{3-16} < 1 \text{ V}$	$-I_3$	—	—	400	$\mu\text{A}$

**Notes to characteristics**

- Oscillator operates at  $V_{7-16} > 2,25 \text{ V}$ .
- I.F. suppression is defined as the ratio  $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$  where:  $V_{i1}$  is the input voltage at  $f = 455 \text{ kHz}$  and  $V_{i2}$  is the input voltage at  $f = 1 \text{ MHz}$ .
- Oscillator voltage at pin 8 can be preset by  $R_{osc}$  (see Fig. 10).
- Maximum current into pin 5 can be adjusted by R1 (see Fig. 10);  

$$I_5 = \frac{V_{3-16}}{R1} - I_3 \text{ when } V_{3-16} = 800 \text{ mV}; I_3 = 400 \mu\text{A}.$$
- AM suppression is measured with  $f_m = 1 \text{ kHz}$ ,  $m = 0,3$  for AM;  $f_m = 400 \text{ Hz}$ ,  $\Delta f = \pm 22,5 \text{ kHz}$  for FM.

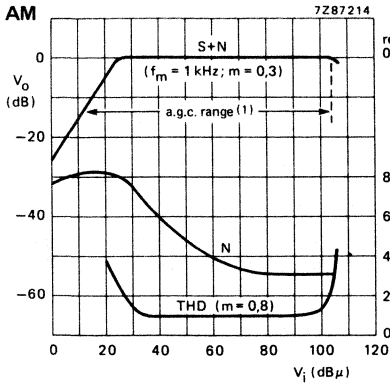
**Facility adaptation**

Facility adaptation is achieved as follows (see Fig. 10):

Facility	Component
FM sensitivity	R1 fixes the current at pin 5 ( $I_5 = \frac{V_{3-16}}{R1} - 400 \mu\text{A}$ ) (gain adjustable $\pm 10 \text{ dB}$ ; see note 4)
AM sensitivity	R11 and coil tapping
AM oscillator biasing	$R_{osc}$
AM output voltage	R7, R11
AM a.g.c. setting	R7



Typical graphs



(1) A.G.C. range (figure of merit, FOM).

Fig. 3 Signal, noise and distortion as a function of input voltage ( $V_i$ ). Measured at  $f_i = 1 \text{ MHz}$  in test circuit Fig. 10.

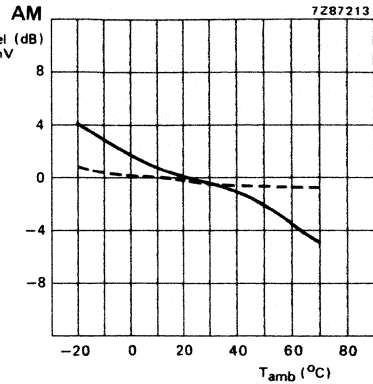


Fig. 4 Sensitivity ( $V_i$ ), output voltage ( $V_o$ ) as a function of temperature behaviour ( $T_{amb}$ ). Measured at  $f_i = 1 \text{ MHz}$  in test circuit Fig. 10.

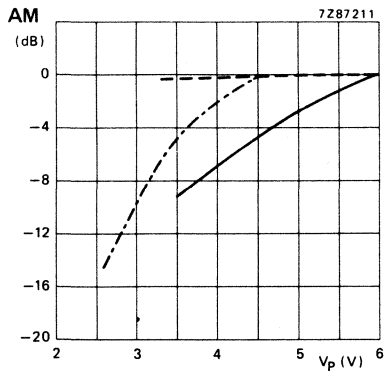


Fig. 5 Sensitivity ( $V_i$ ) and output voltage ( $V_o$ ) as a function of supply voltage ( $V_p$ ). Measured at  $f_i = 1 \text{ MHz}$  in test circuit Fig. 10, for application  $V_p = 6 \text{ V}$ . Also shown is the sensitivity for  $V_p = 4,5 \text{ V}$  application (Fig. 16).

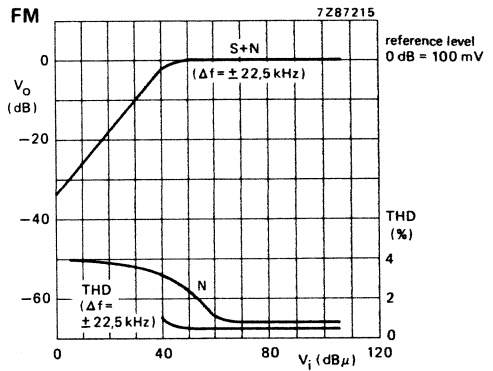
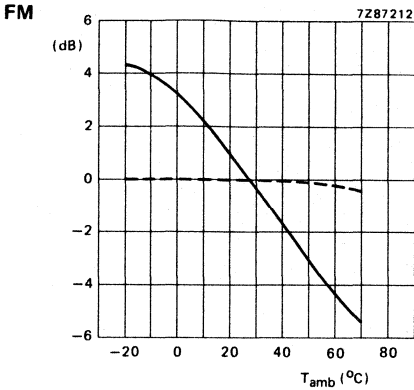
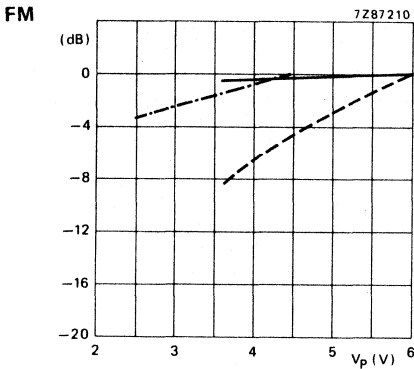


Fig. 6 Signal, noise and distortion as a function of input voltage ( $V_i$ ). Measured at  $f_i = 10,7 \text{ MHz}$  in test circuit Fig. 10.



— sensitivity at  $-3$  dB limiting.  
 - - - output voltage ( $V_O$ ) at  $V_i = 1$  mV;  
 $\Delta f = \pm 22$  kHz.

Fig. 7 Sensitivity ( $V_i$ ), output voltage ( $V_O$ ) as a function of temperature behaviour ( $T_{amb}$ ). Measured at  $f_i = 10,7$  MHz in test circuit Fig. 10.



— sensitivity at  $-3$  dB limiting:  $V_p = 6,0$  V application.  
 - · - · sensitivity at  $-3$  dB limiting:  $V_p = 4,5$  V application.  
 - - - output voltage ( $V_O$ ) at  $V_i = 1$  mV;  
 $\Delta f = \pm 22,5$  kHz.

Fig. 8 Sensitivity ( $V_i$ ) and output voltage ( $V_O$ ) as a function of supply voltage ( $V_p$ ). Measured at  $f_i = 10,7$  MHz in test circuit Fig. 10.

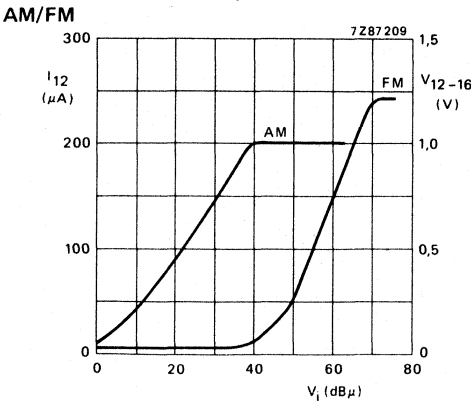
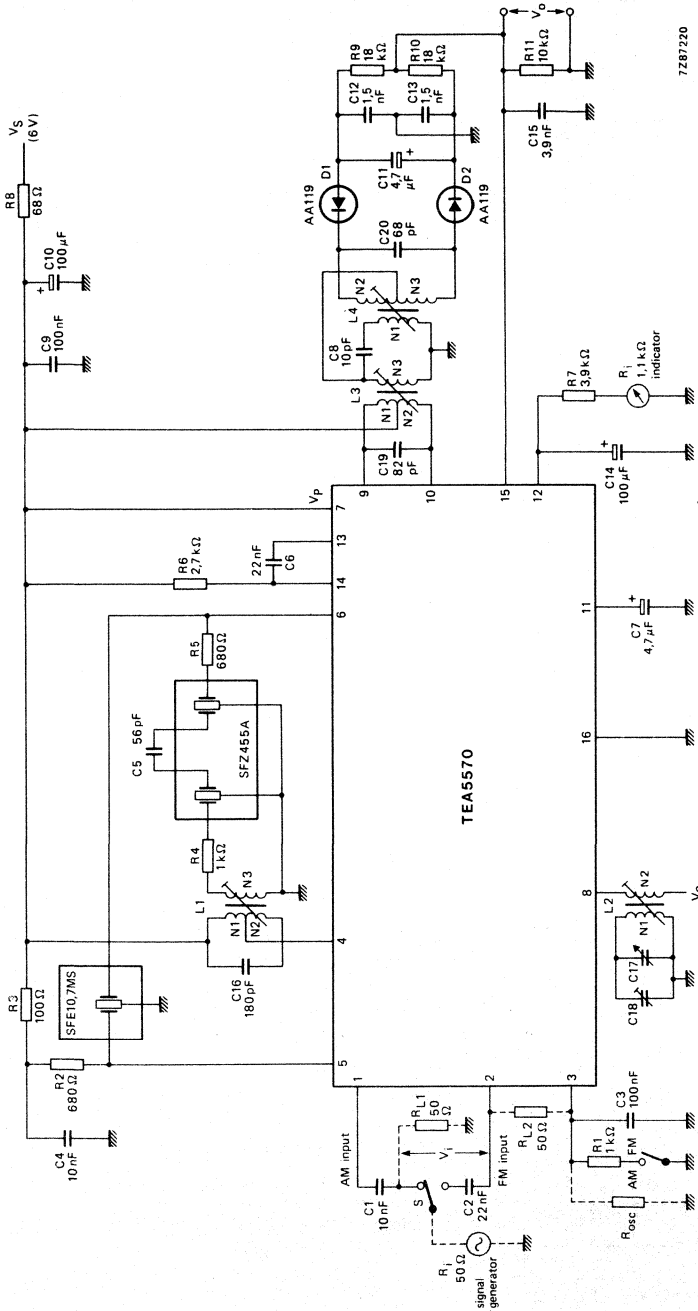


Fig. 9 Indicator output current ( $I_{12}$ ) and d.c. output voltage ( $V_{12-16}$ ): AM  $f_i = 1$  MHz; FM  $f_i = 10,7$  MHz as a function of input voltage ( $V_i$ ). Measured in Fig. 10;  $V_p = 6$  V;  $R_{12-16} = 5$  k $\Omega$ .





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**Coil data**

The transfer impedance of the i.f. filter is:  
 AM:  $|Z_{tr}| = v_6/i_4 = 2,7 \text{ k}\Omega$  (SFZ 455A).  
 FM:  $|Z_{tr}| = v_6/i_5 = 275 \Omega$  (SFE 10,7 MS).  
 See also Figs 11, 12, 13 and 14.

Fig. 10 Test circuit.



COIL DATA

AM i.f. coils (Fig. 10)

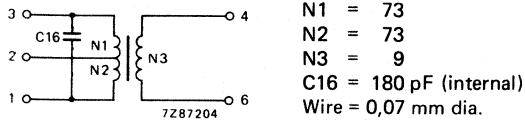


Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.

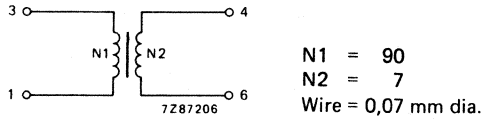


Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

FM i.f. coils (Fig. 10)

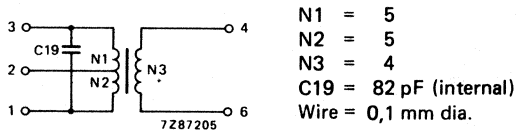


Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

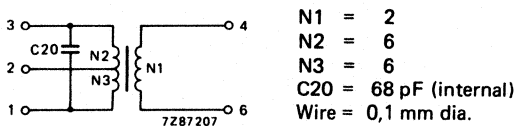
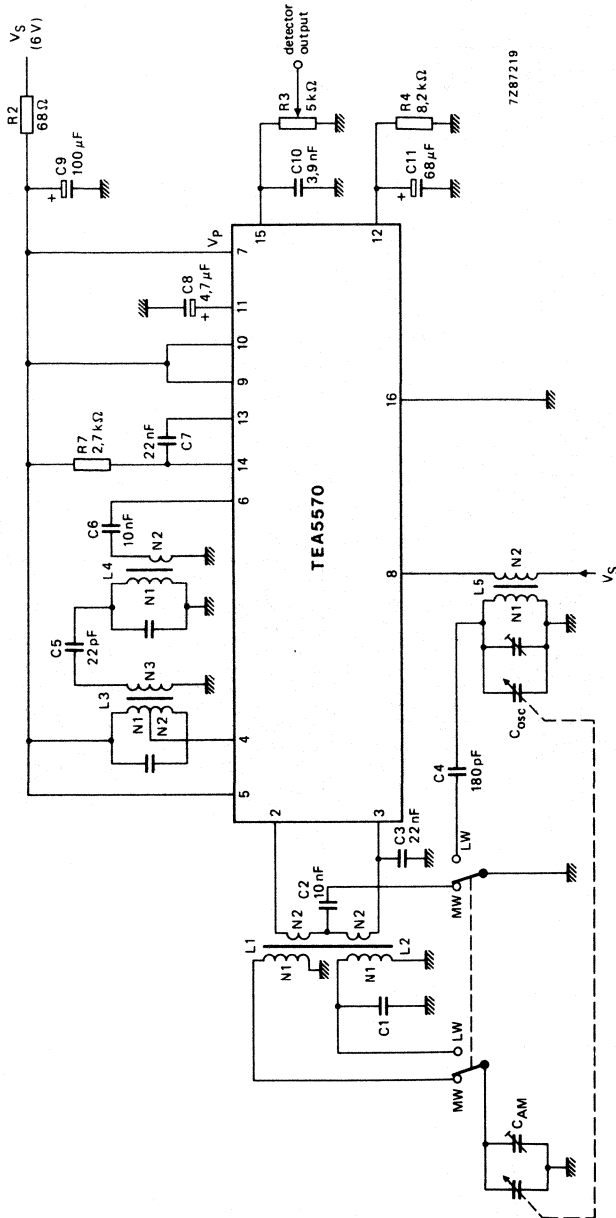


Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

**APPLICATION INFORMATION**

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4.5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.



7Z87219

**Coil data**

- L3 N1 = 73      L4 N1 = 146      L5 N1 = 90
- N2 = 73           N2 = 9                N2 = 6
- N3 = 9        C = 180 pF
- C = 180 pF

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.



APPLICATION INFORMATION (continued)

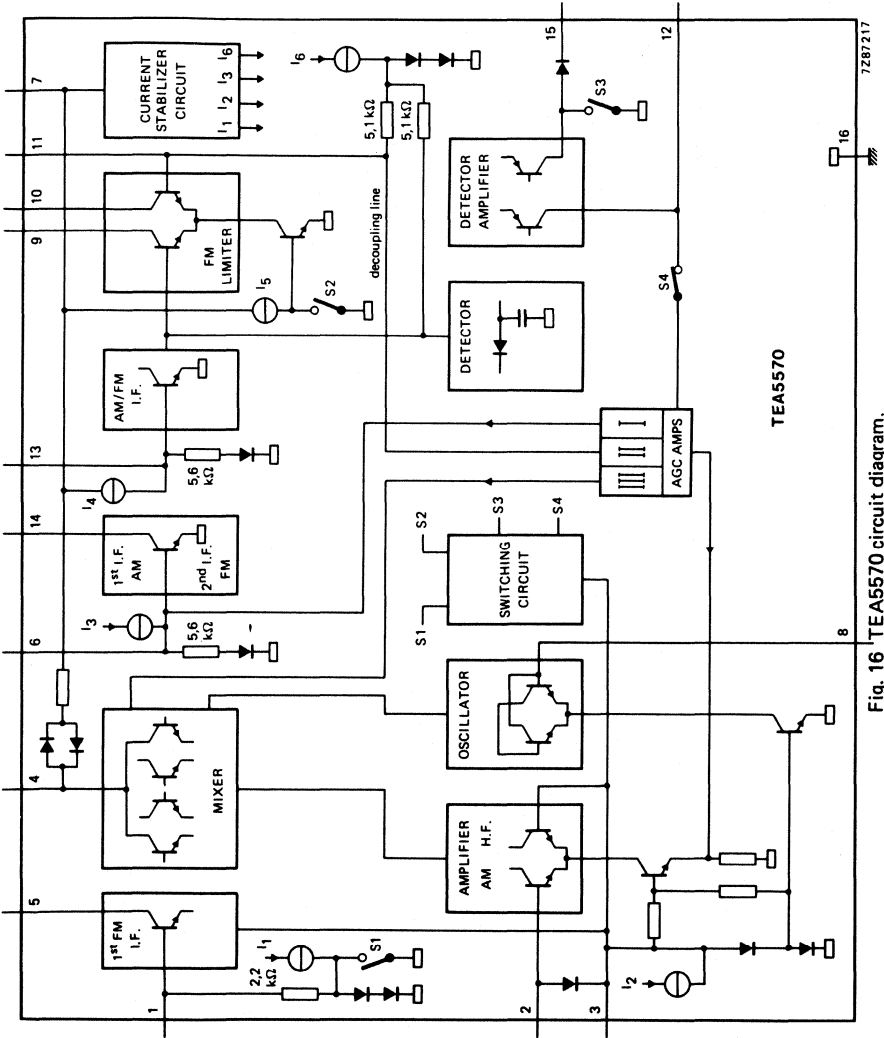
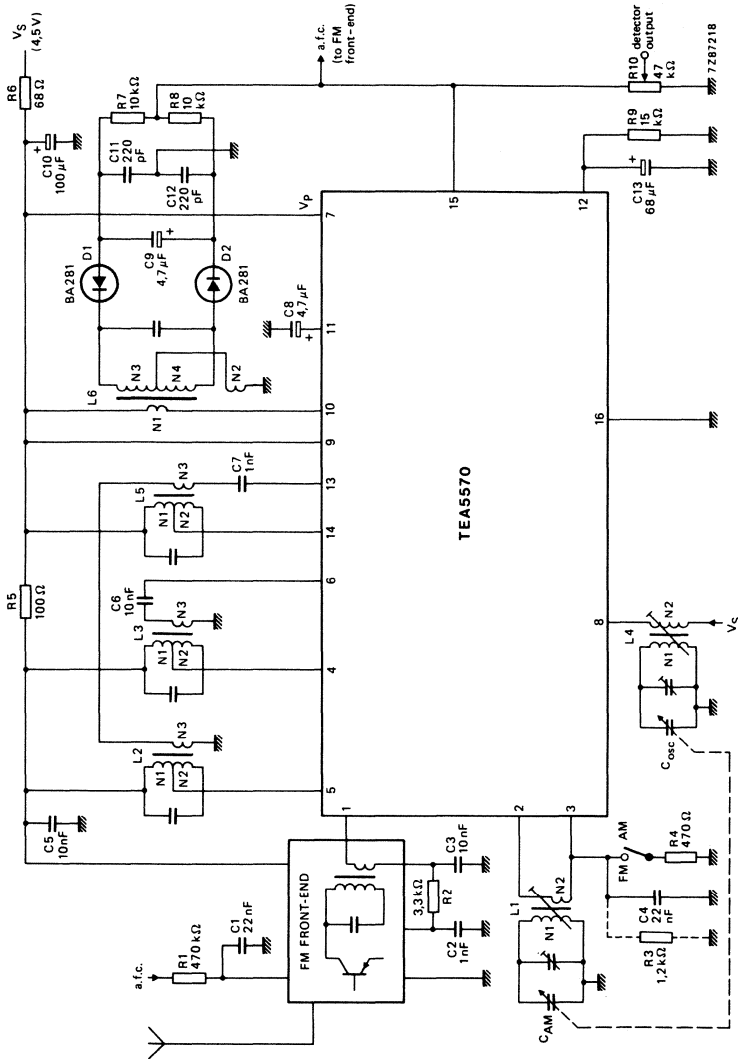


Fig. 16 TEA5570 circuit diagram.

7Z87217



Coil data

- L2 N1 = 3    L3 N1 = 33    L4 N1 = 90    L5 N1 = 33    L6 N1 = 50
- N2 = 8    N2 = 113    N2 = 6    N2 = 50
- N3 = 1    N3 = 9    N3 = 9    N3 = 4,5
- N4 = 6,5    C = 82 pF    C = 180 pF    C = 82 pF

Fig. 17 Typical application circuit for 4.5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

DETAILED APPLICATION INFORMATION WILL BE SUPPLIED ON REQUEST.





## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

TEA5580

## PLL STEREO DECODER

The TEA5580 is a PLL stereo decoder. It is suitable for portable radios, radio recorders, medium-fi and car radio receivers. The circuit incorporates the following functions.

- A **voltage-controlled oscillator** ( $f = 228$  kHz) from which the 19, 38, 57 and 114 kHz signals are obtained via  $I^2L$  logic.
- A **phase-locked-loop system** to lock the VCO to the 19 kHz pilot tone in the stereo signal. The phase detector in the loop system also suppresses phase distortion due to the 57 kHz pilot signal from VHF transmitters (traffic warning system in Germany).
- A **pilot presence detector and an automatic mono/stereo switch**.
- **Two demodulators**, one driven by the 38 kHz decoding signal for the stereo matrix, the second driven by a 114 kHz signal which suppresses the third harmonic of the multiplex signal (MUX). These prevent distortion caused by strong adjacent transmitters.
- A **matrix and two output buffers**, for the left and right output signals.
- An **input amplifier**, the gain of which can be adjusted by the external input resistor.
- A **pilot cancelling circuit**, for extra suppression of the pilot signal.
- An **SDS circuit (signal dependent stereo)** for a smooth changeover from stereo to mono on weak signals.
- A **driver output stage** for a stereo LED indicator.
- A **stabilizer**, for operation over a wide supply voltage range.

The stereo decoder is compensated for a typical i.f. filter with a roll-off frequency of 50 kHz (2 dB down at 38 kHz).

### QUICK REFERENCE DATA

Applicable supply voltage range	$V_S$	3,6 to 16 V	
Supply voltage (pin 9)	$V_P$	nom.	6 V
Ambient temperature	$T_{amb}$	typ.	25 °C
Total quiescent current	$I_{tot}$	typ.	10 mA
Measured at $V_{i(p-p)} = 1$ V (MUX with 27 mV pilot)			
Overall gain	$G_o$	typ.	0 to 20 dB
Output channel unbalance	$V_{1.5}/V_{2.5}$	<	$\pm 1$ dB
Output voltage (r.m.s. value)	$V_{1.5}/V_{2.5}$	typ.	0,4 V
Total harmonic distortion (300 Hz to 20 kHz)	THD	typ.	0,2 %
Signal-to-noise ratio, DIN A-curve	S/N	typ.	80 dB
Channel separation	$\alpha$	typ.	40 dB
Carrier suppression at: f = 19 kHz (adjusted)	$\alpha_{19}$	typ.	50 dB

### PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

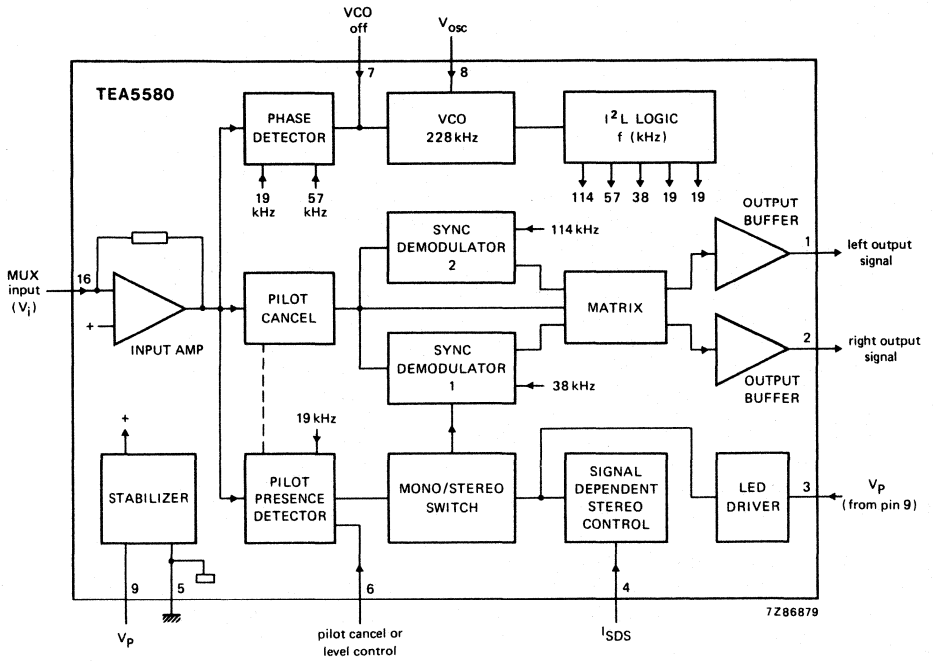


Fig. 1 Block diagram.



## A.C. CHARACTERISTICS

Measured in circuit of Fig. 2 at  $V_P = 6\text{ V}$ ,  $V_{i(p-p)} = 1\text{ V}$  (MUX with 27 mV pilot)

Input impedance (external)	$ Z_i $	typ.	47 k $\Omega$
Output impedance (external)	$ Z_o $	typ.	5,1 k $\Omega$
Output voltage (r.m.s. value)	$V_{o(rms)}$	typ.	400 mV
Total harmonic distortion (300 Hz to 10 kHz) (mono, stereo and mono + pilot)	THD	typ.	0,2 %
Total harmonic distortion at $V_{o(rms)} = 0,6\text{ V}$	THD	<	1 %
Signal-to-noise ratio (DIN A-curve)	S/N	typ.	80 dB
Channel separation (for L = 1 and R = 0)	$\alpha$	typ.	40 dB
SDS control			
10 dB channel separation	$I_4$	typ.	50 $\mu\text{A}$
full stereo (channel separation $\geq 26\text{ dB}$ )	$I_4$	>	100 $\mu\text{A}$
full mono (channel separation $\leq 1\text{ dB}$ )	$I_4$	<	10 $\mu\text{A}$
Stereo/mono switch (for $R2 = \blacktriangle\text{k}\Omega$ )			
for switching to stereo	$V_i$	<	18 mV
for switching to mono	$V_i$	>	5 mV
hysteresis	$\Delta V_i$	typ.	13 mV
VCO frequency (adjustable)	$f_{VCO}$	typ.	2,5 dB
Capture range (deviation from 228 kHz centre frequency) $V_{pilot} = 32\text{ mV}$	$f_{VCO}$	typ.	228 kHz
Temperature coefficient (uncompensated)	TC	typ.	3,5 %
VCO off switching voltage (pin 7)	$V_{off}$	>	$\blacktriangle\text{ kHz/K}$
Carrier suppression (adjusted by R2) at:			
$f = 19\text{ kHz}$	$\alpha_{19}$	typ.	3 V
$f = 38\text{ kHz}$	$\alpha_{38}$	typ.	50 dB
$f = 228\text{ kHz}$	$\alpha_{228}$	typ.	50 dB
ACI suppression at: *			70 dB
$f = 114\text{ kHz}$	$\alpha_{114}$	typ.	80 dB
$f = 190\text{ kHz}$	$\alpha_{190}$	typ.	60 dB
SCA suppression at $f = 67\text{ kHz}$	$\alpha_{67}$	typ.	66 dB
VWF suppression**	$\alpha_{VWF}$	typ.	70 dB
Ripple rejection at $f = 100\text{ Hz}$			
$V_S = 3,6\text{ V}$	RR	typ.	20 dB
$V_S = 8\text{ V}$	RR	typ.	26 dB

$$* \text{ ACI suppression: } \alpha_{114} = 20 \log \frac{V_o \text{ (at 1 kHz)}}{V_o \text{ (at 4 kHz)}}$$

90% S-signal (L = -R,  $f_m = 1\text{ kHz}$ ); 9% pilot signal; 1% spurious signal ( $f = 110\text{ kHz}$ ).

$$** \text{ VWF suppression: } \alpha_{VWF} = 20 \log \frac{V_o \text{ (at 1 kHz + 23 Hz)}}{V_o \text{ (at 1 kHz)}}$$

90% S-signal (L = -R,  $f_m = 1\text{ kHz}$ ); 9% pilot signal; 5% VWF signal ( $f = 57\text{ kHz}$ ,  $f_m = 23\text{ Hz AM}$ ,  $m = 60\%$ ). $\blacktriangle$  Value to be established.

APPLICATION INFORMATION

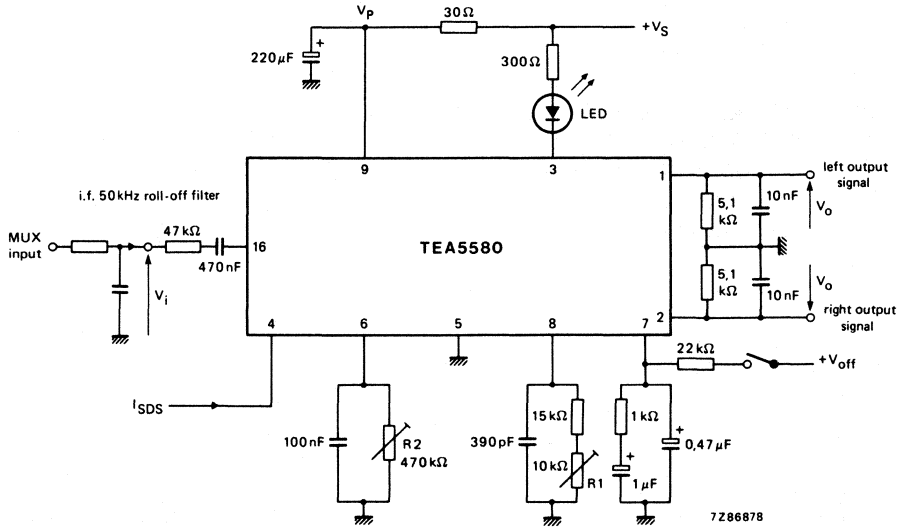


Fig. 2 Test and application diagram.

Notes

- R1: VCO frequency adjustment;  $f = 228 \text{ kHz}$ .
- R2: pilot cancelling and pilot level.



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.



TEA6000

# FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

## GENERAL DESCRIPTION

The TEA6000 is an FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes an AM/FM-IF counter and an analogue-to-digital interface. The i.f. counter generates AM/FM precision tuning and accurate stop information.

## Features

- 3-stage IF limiter for driving a ratio detector
- 2-stage level detector with current output
- operational amplifier for active filtering (e.g. multipath detector)
- high resolution frequency counter for FM and AM IF-signals
- time base reference from crystal oscillator or external source (SAA1057)
- serial two wire bidirectional computer interface (I<sup>2</sup>C-bus)
- multiplexed 3 bit A/D converter for two input signals
- software controlled sensitivity for both ADC inputs

## QUICK REFERENCE DATA

Supply voltages ( $V_{P1}$ and $V_{P2}$ )	$V_P$	typ.	8,4 V
Supply current; ( $I_{P1}$ + $I_{P2}$ )	$I_P$	typ.	36 mA
FM/IF sensitivity			
at -3 dB before limiting	$V_i$	typ.	150 $\mu$ V
Signal to noise ratio for $V_i = 10$ mV	S/N	typ.	80 dB
Audio output voltage			
$\Delta f = 22,5$ kHz; $V_i = 1$ mV	$V_O$	typ.	170 mV
$\Delta f = 75$ kHz; $V_i = 1$ mV	$V_O$	typ.	520 mV
AM suppression at $V_i = 10$ mV	AMS	typ.	58 dB
Frequency counter sensitivity			
AM (pin 18)	$V_{i(am)}$	typ.	60 $\mu$ V
FM (pin 16)	$V_{i(fm)}$	typ.	80 $\mu$ V
Resolution frequency counter			
AM	$f_s(am)$	typ.	+250 Hz
FM	$f_s(fm)$	typ.	6,4 kHz
Power dissipation	$P_{tot}$	max.	1300 mW
Storage temperature	$T_{stg}$		-55 to + 150 $^{\circ}$ C
Operating ambient temperature	$T_{amb}$		-30 to + 85 $^{\circ}$ C

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



## FUNCTIONAL DESCRIPTION

The IF SECTION consists of three balanced differential stages with separated FM and AM inputs, directly coupled by emitter followers. The last stage also has separated outputs, which are intended for driving a ratio detector and the frequency measuring system respectively.

The last two stages are coupled via low-value capacitors to two LEVEL DETECTORS which generate a signal-dependent d.c. current for controlling channel separation and frequency response of a stereo decoder, multipath detector circuitry, AGC and the internal ADC.

The IF MUTING circuit has been incorporated to decrease the interstation noise by about 15 dB.

The 3-bit A/D CONVERTER has two inputs, which are selected via two multiplexed analogue switches. One of these switches is internally connected to the level detector output but can also serve as an external input, as the level detector output can be switched off. The outputs of the ADC are converted to a Gray code, latched and reconverted to a binary code to obtain glitch-free output data. The sensitivity of both inputs can be selected independently via software on two levels.

The reference for the ADC is derived from a BAND-GAP STABILIZER circuit. Multipath distortion on FM will generate an AM modulation on the d.c. voltage from the level detectors. This AM modulation can be filtered and rectified to obtain a multipath-dependent d.c. voltage. This voltage can be applied to the other input of the ADC.

To facilitate filtering an OPERATIONAL AMPLIFIER (OPA) is incorporated on the chip. The typical circuit diagram for a multipath filter is given in Fig. 4.

The FREQUENCY COUNTER is preceded by a 7-stage prescaler for FM, and FM/AM selector stage and a divider by 1 or 2. The actual counter is a presetable and resetable 8-stage counter with a 3-stage data disable overflow counter, which can be switched off. The eight significant output bits are situated symmetrically around 10,7 MHz and 460 kHz, when the external timebase source is used (e.g. SAA1057). See Table 1.

The reference for the TIMEBASE is primarily thought to be the SAA1057. This circuit generates from its 4 MHz crystal oscillator a 32 or 40 kHz signal. This signal is buffered and applied to the timebase circuitry (mode I). The circuit diagram for this mode I is given in Fig. 5a.

In the timebase, the selection is made for reference frequency (32 to 40 kHz), FM or AM mode and the width of the measuring window, all under software control. Accuracy  $\pm \frac{1}{2}$  bit when the window is set to wide (see Fig. 2) and  $\pm 1$  bit when set to narrow. A special feature is the synchronization of the measuring cycle with the input DATA of the I<sup>2</sup>C-bus, meaning the measuring cycle starts immediately after a "WRITE" instruction via the I<sup>2</sup>C-bus.

For those who do not use the SAA1057 as reference, a 2<sup>15</sup> Hz crystal (32 768 Hz) can be connected to the reference inputs directly, obtaining a quartz-oscillator reference. See Fig. 5b for the circuit diagram for this mode II.

When the circuit is used in mode II a correction has to be made to the values of window width and resolution as the cheap watch crystals differ by about 2,4% from the frequency generated by the SAA1057 (32 768 and 32 000 kHz respectively) See Table 2.

Communication between MUST1 and the microcomputer is accomplished via the two-wire bidirectional I<sup>2</sup>C-bus (slave transceiver version); the SDA (serial data) and SCL (serial clock).

To prevent crosstalk between the digital and analogue parts of the circuit the power supply lines are fully isolated.



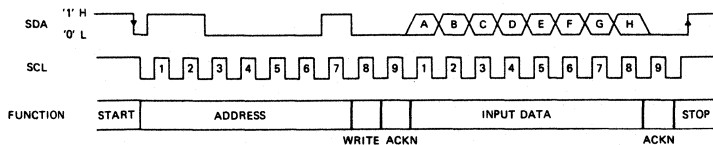


Fig. 2 Input data format waveforms.

Input bits

bit	function	"0"	"1"	reference to Fig. 2
1	reference frequency	32 kHz	40 kHz	A
2	sensitivity ADC2	LOW	HIGH	B
3	sensitivity ADC1	LOW	HIGH	C
4	level detector output	off	on	D
5	AM/FM	AM	FM	E
6	overflow counter	off	on	F
7	measuring window	narrow	wide	G
8	test mode	off	on	H

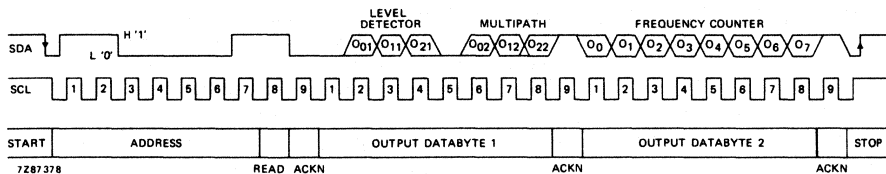


Fig. 3 Output data format waveforms.

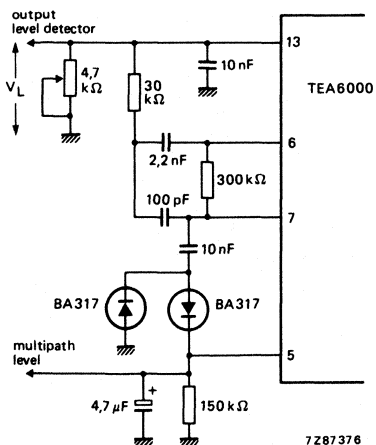


Fig. 4 Multipath detector circuit.

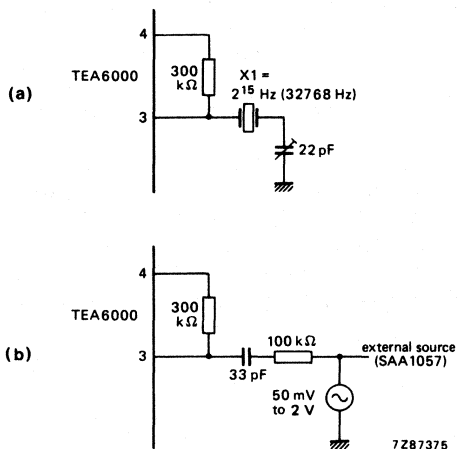


Fig. 5 Oscillator/buffer circuits.  
X1 = 2<sup>15</sup> Hz (32 768 Hz).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage					
pin 2	V <sub>p1</sub>	max.	13,2 V		
pin 12	V <sub>p2</sub>	max.	13,2 V		
Power dissipation	P <sub>tot</sub>	max.	1300 mW		
Storage temperature	T <sub>stg</sub>		-55 to + 150 °C		
Operating ambient temperature	T <sub>amb</sub>		-30 to + 85 °C		

**THERMAL RESISTANCE**

From crystal to ambient R<sub>th c-a</sub> = 50 K/W

**D.C. CHARACTERISTICS**

V<sub>p1</sub> = V<sub>p2</sub> = 8,4 V; T<sub>amb</sub> = 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
(pin 2)	V <sub>p1</sub>	7,6	8,4	9,2	V
(pin 12)	V <sub>p2</sub>	7,6	8,4	9,2	V
Supply current AM mode					
pin 2	I <sub>p1</sub>	—	18,5	—	mA
pin 12	I <sub>p2</sub>	—	17,4	—	mA
Supply current FM mode					
pin 2	I <sub>p1</sub>	—	19,2	—	mA
pin 12	I <sub>p2</sub>	—	16,4	—	mA
Power dissipation	P <sub>tot</sub>	—	350	—	mW

**A.C. CHARACTERISTICS** (see Fig. 6)

V<sub>p1</sub> = V<sub>p2</sub> = 8,4 V; V<sub>16-10</sub> = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f<sub>m</sub> = 1 kHz; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity					
at -3 dB before limiting	V <sub>I(FM)</sub>	—	150	—	μV
Signal-to-noise ratio, FM input					
V <sub>i</sub> = 20 μV	S/N	40	46	—	dB
V <sub>i</sub> = 150 μV	S/N	—	64	—	dB
V <sub>i</sub> = 1 mV	S/N	—	76	—	dB
V <sub>i</sub> = 10 mV	S/N	—	80	—	dB
Noise output voltage					
V <sub>i</sub> = 0 V; with muting, switch S1 on	V <sub>no</sub>	—	55	—	μV
V <sub>i</sub> = 0 V; without muting, S1 off	V <sub>no</sub>	—	420	—	μV
Audio output voltage					
Δf = 22,5 kHz	V <sub>O</sub>	—	170	—	mV
Δf = 75 kHz	V <sub>O</sub>	—	520	—	mV

DEVELOPMENT SAMPLE DATA



## A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
<b>AM suppression</b>					
ratio of the AM output signal referred to the FM signal ( $m = 0,3$ )					
$V_i = 150 \mu\text{V}$	AMS	—	46	—	dB
$V_i = 1 \text{ mV}$	AMS	—	62	—	dB
$V_i = 10 \text{ mV}$	AMS	—	58	—	dB
$V_i = 100 \text{ mV}$	AMS	—	60	—	dB
<b>Level detector output voltage (Fig. 4)</b>					
$R_{13-10} = 4,7 \text{ k}\Omega$ ; $V_i = 10 \text{ mV}$ , FM mode	$V_L$	—	6,2	—	V
<b>Level detector output voltage slope</b>					
$R_{13-10}$ adjusted in FM mode for					
$V_L = 5,5 \text{ V}$ at $V_i = 10 \text{ mV}$ ; $f = 10,7 \text{ MHz}$					
$V_i = 0 \text{ V}$ (pin 16)	$V_L(\text{FM})$	—	130	—	mV
$V_i = 140 \mu\text{V}$	$V_L(\text{FM})$	—	1,3	—	V
$V_i = 1 \text{ mV}$	$V_L(\text{FM})$	—	2,7	—	V
$V_i = 3 \text{ mV}$	$V_L(\text{FM})$	—	4,4	—	V
$R_{13-10}$ adjusted in FM mode (see above)					
$V_i = 0 \text{ V}$ , $f = 460 \text{ kHz}$ (pin 18)	$V_L(\text{AM})$	—	200	—	mV
$V_i = 1 \text{ mV}$ , $f = 460 \text{ kHz}$ (pin 18)	$V_L(\text{AM})$	—	1,4	—	V
$V_i = 10 \text{ mV}$ , $f = 460 \text{ kHz}$ (pin 18)	$V_L(\text{AM})$	—	2,7	—	V
<b>Frequency counter sensitivity</b>					
AM input voltage (pin 18)	$V_{I(\text{AM})}$	—	60	—	$\mu\text{V}$
FM input voltage (pin 16)	$V_{I(\text{FM})}$	—	80	—	$\mu\text{V}$
AM input impedance	$R_i$	—	30	—	$\text{k}\Omega$
<b>BUS inputs</b>					
SDA and SCL (pins 9 and 8)					
input voltage HIGH	$V_{IH}$	3,0	—	$V_{P1}$	V
input voltage LOW	$V_{IL}$	-0,3	—	1,5	V
input current HIGH	$I_{IH}$	—	—	10	$\mu\text{A}$
input current LOW	$I_{IL}$	—	—	10	$\mu\text{A}$
acknowledge sink current	$I_{ack}$	—	—	2	$\text{mA}$
maximum input frequency	$f_{i \text{ max}}$	100	—	—	$\text{kHz}$
<b>Output voltage SDA</b>					
HIGH; $4 \text{ k}\Omega$ to $8,4 \text{ V}$	$V_{OH}$	8,0	—	—	V
LOW; $I = 2 \text{ mA}$	$V_{OL}$	—	—	0,4	V



DEVELOPMENT SAMPLE DATA

parameter	symbol	min.	typ.	max.	unit
A/D converter (pin 5 and 13)					
input resistance	$R_i$		t.b.f.		k $\Omega$
input capacitance	$C_i$		t.b.f.		pF
Trip levels, sensitivity bit HIGH					
level 1	$V_T$	—	0,6	—	V
level 2	$V_T$	—	1,06	—	V
level 3	$V_T$	—	1,38	—	V
level 4	$V_T$	—	1,84	—	V
level 5	$V_T$	—	2,14	—	V
level 6	$V_T$	—	2,55	—	V
level 7	$V_T$	—	2,97	—	V
Trip levels, sensitivity bit LOW					
level 1	$V_T$	—	0,96	—	V
level 2	$V_T$	—	1,78	—	V
level 3	$V_T$	—	2,44	—	V
level 4	$V_T$	—	3,26	—	V
level 5	$V_T$	—	3,92	—	V
level 6	$V_T$	—	4,63	—	V
level 7	$V_T$	—	5,38	—	V
Crystal oscillator (see Fig. 5)					
reference frequency	$f_{ref}$	32	32,768	40	kHz
temperature coefficient	TC		t.b.f.		10 <sup>-6</sup>
input resistance	$R_i$		t.b.f.		k $\Omega$
input capacitance	$C_i$		t.b.f.		pF
Operational amplifier (pins 6 and 7)					
voltage gain	$G_V$	—	10 <sup>4</sup>	—	
input bias current	$I_{bias}$	—	30	100	nA
output sink current at $V_o = 1$ V	$I_o$	—	0,2	—	mA
output source current at $V_o = 7,4$ V	$I_o$	5,5	10	—	mA
output voltage swing	$V_{7(p-p)}$	—	5,5	—	V
Frequency measuring system (see pages 8 and 9)					
measuring windows; $f_{ref} = 32$ or 40 kHz					
AM					
window "0" (LOW)	$t_{gate}$	—	4	—	ms
window "1" (HIGH)	$t_{gate}$	—	8	—	ms
FM					
window "0" (LOW)	$t_{gate}$	—	20	—	ms
window "1" (HIGH)	$t_{gate}$	—	40	—	ms
resolution frequency counter					
AM	$f_s(am)$	—	250	—	Hz
FM	$f_s(fm)$	—	6,4	—	kHz

$t_{gate}$  has to be multiplied by 32 000/32 768 for a  $f_{ref}$  of 2<sup>15</sup> Hz.  
 $f_s$  has to be multiplied by 32 768/32 000 for a  $f_{ref}$  of 2<sup>15</sup> Hz.



TABLE 1 REFERENCE FREQUENCY 32 000 Hz (SAA1057)

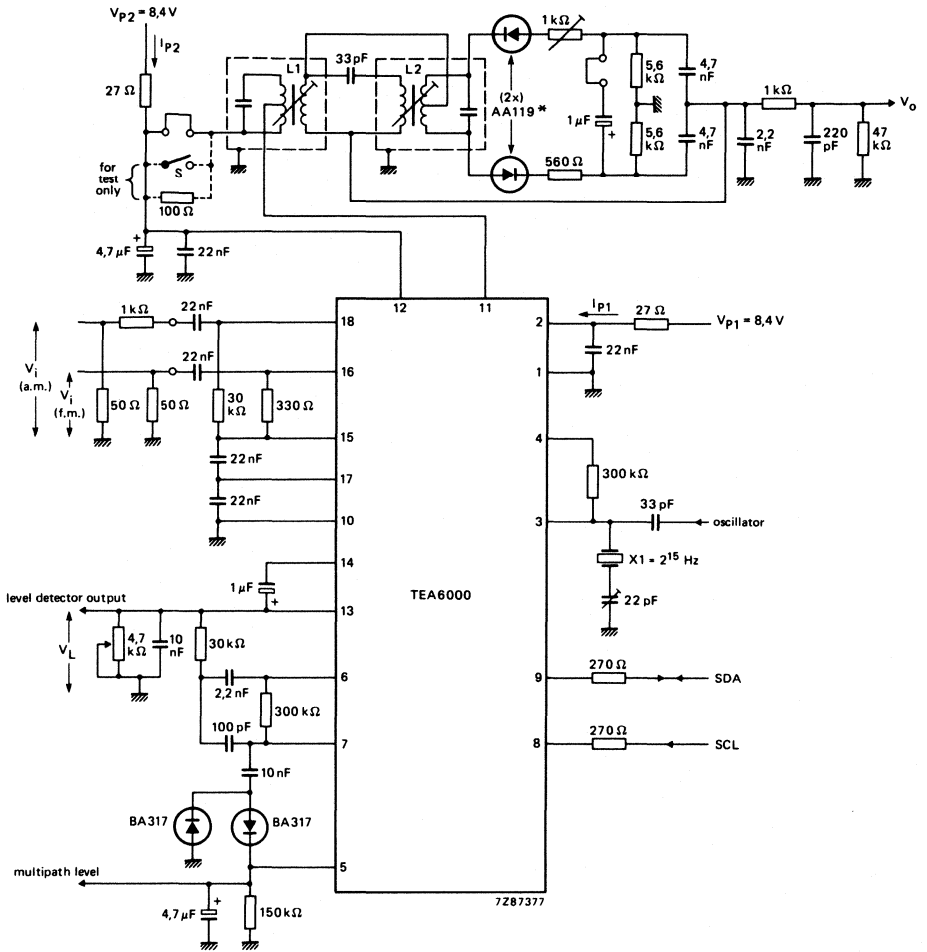
AM (kHz)		FM (MHz)		AM (kHz)		FM (MHz)		AM (kHz)		FM (MHz)		AM (kHz)		FM (MHz)	
IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT
428.25	001	5.888	10.214	453.0	166	10.541	466.50	199	10.867	479.25	194	11.204	479.25	194	11.204
428.50	001	5.894	10.221	454.0	167	10.547	466.75	19A	10.874	479.50	194	11.209	479.50	194	11.209
428.75	001	5.901	10.227	454.25	168	10.554	467.00	19B	10.880	480.00	194	11.213	480.00	194	11.213
428.50	004	5.914	10.240	454.50	169	10.560	467.25	19C	10.886	480.25	194	11.218	480.25	194	11.218
428.75	004	5.920	10.246	454.75	16A	10.566	467.50	19D	10.893	480.50	194	11.224	480.50	194	11.224
428.75	006	5.925	10.253	455.00	16B	10.573	467.75	19E	10.900	480.75	194	11.229	480.75	194	11.229
430.00	001	5.933	10.259	455.25	16C	10.579	468.00	19F	10.912	481.00	194	11.238	481.00	194	11.238
430.25	001	5.939	10.265	455.50	16E	10.586	468.25	19A	10.918	481.25	194	11.243	481.25	194	11.243
430.50	001	5.945	10.271	455.75	16E	10.592	468.50	19A	10.924	481.50	194	11.248	481.50	194	11.248
430.75	001	5.951	10.277	456.00	16E	10.598	468.75	19A	10.930	481.75	194	11.253	481.75	194	11.253
431.00	001	5.957	10.283	456.25	16E	10.604	469.00	19A	10.936	482.00	194	11.258	482.00	194	11.258
431.25	001	5.963	10.289	456.50	16E	10.610	469.25	19A	10.942	482.25	194	11.263	482.25	194	11.263
431.50	001	5.969	10.295	456.75	16E	10.616	469.50	19A	10.948	482.50	194	11.268	482.50	194	11.268
431.75	001	5.975	10.301	457.00	16E	10.622	469.75	19A	10.954	482.75	194	11.273	482.75	194	11.273
432.00	001	5.981	10.307	457.25	16E	10.628	470.00	19A	10.960	483.00	194	11.278	483.00	194	11.278
432.25	001	5.987	10.313	457.50	16E	10.634	470.25	19A	10.966	483.25	194	11.283	483.25	194	11.283
432.50	001	5.993	10.319	457.75	16E	10.640	470.50	19A	10.972	483.50	194	11.288	483.50	194	11.288
432.75	001	5.999	10.325	458.00	16E	10.646	470.75	19A	10.978	483.75	194	11.293	483.75	194	11.293
433.00	001	6.005	10.331	458.25	16E	10.652	471.00	19A	10.984	484.00	194	11.298	484.00	194	11.298
433.25	001	6.011	10.337	458.50	16E	10.658	471.25	19A	10.990	484.25	194	11.303	484.25	194	11.303
433.50	001	6.017	10.343	458.75	16E	10.664	471.50	19A	10.996	484.50	194	11.308	484.50	194	11.308
433.75	001	6.023	10.349	459.00	16E	10.670	471.75	19A	11.002	484.75	194	11.313	484.75	194	11.313
434.00	001	6.029	10.355	459.25	16E	10.676	472.00	19A	11.008	485.00	194	11.318	485.00	194	11.318
434.25	001	6.035	10.361	459.50	16E	10.682	472.25	19A	11.014	485.25	194	11.323	485.25	194	11.323
434.50	001	6.041	10.367	459.75	16E	10.688	472.50	19A	11.020	485.50	194	11.328	485.50	194	11.328
434.75	001	6.047	10.373	460.00	16E	10.694	472.75	19A	11.026	485.75	194	11.333	485.75	194	11.333
435.00	001	6.053	10.379	460.25	16E	10.700	473.00	19A	11.032	486.00	194	11.338	486.00	194	11.338
435.25	001	6.059	10.385	460.50	16E	10.706	473.25	19A	11.038	486.25	194	11.343	486.25	194	11.343
435.50	001	6.065	10.391	460.75	16E	10.712	473.50	19A	11.044	486.50	194	11.348	486.50	194	11.348
435.75	001	6.071	10.397	461.00	16E	10.718	473.75	19A	11.050	486.75	194	11.353	486.75	194	11.353
436.00	001	6.077	10.403	461.25	16E	10.724	474.00	19A	11.056	487.00	194	11.358	487.00	194	11.358
436.25	001	6.083	10.409	461.50	16E	10.730	474.25	19A	11.062	487.25	194	11.363	487.25	194	11.363
436.50	001	6.089	10.415	461.75	16E	10.736	474.50	19A	11.068	487.50	194	11.368	487.50	194	11.368
436.75	001	6.095	10.421	462.00	16E	10.742	474.75	19A	11.074	487.75	194	11.373	487.75	194	11.373
437.00	001	6.101	10.427	462.25	16E	10.748	475.00	19A	11.080	488.00	194	11.378	488.00	194	11.378
437.25	001	6.107	10.433	462.50	16E	10.754	475.25	19A	11.086	488.25	194	11.383	488.25	194	11.383
437.50	001	6.113	10.439	462.75	16E	10.760	475.50	19A	11.092	488.50	194	11.388	488.50	194	11.388
437.75	001	6.119	10.445	463.00	16E	10.766	475.75	19A	11.098	488.75	194	11.393	488.75	194	11.393
438.00	001	6.125	10.451	463.25	16E	10.772	476.00	19A	11.104	489.00	194	11.398	489.00	194	11.398
438.25	001	6.131	10.457	463.50	16E	10.778	476.25	19A	11.110	489.25	194	11.403	489.25	194	11.403
438.50	001	6.137	10.463	463.75	16E	10.784	476.50	19A	11.116	489.50	194	11.408	489.50	194	11.408
438.75	001	6.143	10.469	464.00	16E	10.790	476.75	19A	11.122	489.75	194	11.413	489.75	194	11.413
439.00	001	6.149	10.475	464.25	16E	10.796	477.00	19A	11.128	490.00	194	11.418	490.00	194	11.418
439.25	001	6.155	10.481	464.50	16E	10.802	477.25	19A	11.134	490.25	194	11.423	490.25	194	11.423
439.50	001	6.161	10.487	464.75	16E	10.808	477.50	19A	11.140	490.50	194	11.428	490.50	194	11.428
439.75	001	6.167	10.493	465.00	16E	10.814	477.75	19A	11.146	490.75	194	11.433	490.75	194	11.433
440.00	001	6.173	10.499	465.25	16E	10.820	478.00	19A	11.152	491.00	194	11.438	491.00	194	11.438
440.25	001	6.179	10.505	465.50	16E	10.826	478.25	19A	11.158	491.25	194	11.443	491.25	194	11.443
440.50	001	6.185	10.511	465.75	16E	10.832	478.50	19A	11.164	491.50	194	11.448	491.50	194	11.448
440.75	001	6.191	10.517	466.00	16E	10.838	478.75	19A	11.170	491.75	194	11.453	491.75	194	11.453
441.00	001	6.197	10.523	466.25	16E	10.844	479.00	19A	11.176	492.00	194	11.458	492.00	194	11.458
441.25	001	6.203	10.529	466.50	16E	10.850	479.25	19A	11.182	492.25	194	11.463	492.25	194	11.463
441.50	001	6.209	10.535	466.75	16E	10.856	479.50	19A	11.188	492.50	194	11.468	492.50	194	11.468
441.75	001	6.215	10.541	467.00	16E	10.862	479.75	19A	11.194	492.75	194	11.473	492.75	194	11.473
442.00	001	6.221	10.547	467.25	16E	10.868	480.00	19A	11.200	493.00	194	11.478	493.00	194	11.478
442.25	001	6.227	10.553	467.50	16E	10.874	480.25	19A	11.206	493.25	194	11.483	493.25	194	11.483
442.50	001	6.233	10.559	467.75	16E	10.880	480.50	19A	11.212	493.50	194	11.488	493.50	194	11.488
442.75	001	6.239	10.565	468.00	16E	10.886	480.75	19A	11.218	493.75	194	11.493	493.75	194	11.493
443.00	001	6.245	10.571	468.25	16E	10.892	481.00	19A	11.224	494.00	194	11.498	494.00	194	11.498
443.25	001	6.251	10.577	468.50	16E	10.898	481.25	19A	11.230	494.25	194	11.503	494.25	194	11.503
443.50	001	6.257	10.583	468.75	16E	10.904	481.50	19A	11.236	494.50	194	11.508	494.50	194	11.508
443.75	001	6.263	10.589	469.00	16E	10.910	481.75	19A	11.242	494.75	194	11.513	494.75	194	11.513
444.00	001	6.269	10.595	469.25	16E	10.916	482.00	19A	11.248	495.00	194	11.518	495.00	194	11.518
444.25	001	6.275	10.601	469.50	16E	10.922	482.25	19A	11.254	495.25	194	11.523	495.25	194	11.523
444.50	001	6.281	10.607	469.75	16E	10.928	482.50	19A	11.260	495.50	194	11.528	495.50	194	11.528
444.75	001	6.287	10.613	470.00	16E	10.934	482.75	19A	11.266	495.75	194	11.533	495.75	194	11.533
445.00	001	6.293	10.619	470.25	16E	10.940	483.00	19A	11.272	496.00	194	11.538	496.00	194	11.538
445.25	001	6.299	10.625	470.50	16E	10.946	483.25	19A	11.278	496.25	194	11.543	496.25	194	11.543
445.50	001	6.305	10.631	470.75	16E	10.952	483.50	19A	11.284	496.50	194	11.548	496.50	194	11.548
445.75	001	6.311	10.637	471.00	16E	10.958	483.75	19A	11.290	496.75	194	11.553	496.75	194	11.553
446.00	001	6.317	10.643	471.25	16E	10.964	484.00	19A	11.296	497.00	194	11.558	497.00	194	11.558
446.25	001	6.323	10.649	471.50	16E	10.970	484.25	19A	11.302	497.25	194	11.563	497.25	194	11.563
446.50	001	6.329	10.655	471.75	16E	10.976	484.50	19A	11.308	497.50	194	11.568	49		

DEVELOPMENT SAMPLE DATA

TABLE 2 REFERENCE FREQUENCY 32 768 Hz (2<sup>15</sup> Hz)

FM (MHz)		AM (kHz)		FM (MHz)		AM (kHz)		FM (MHz)		AM (kHz)		FM (MHz)		AM (kHz)	
READ	OUT	READ	OUT	READ	OUT	READ	OUT	READ	OUT	READ	OUT	READ	OUT	READ	OUT
438.78	001	10.132	451.54	133	10.460	468.04	166	10.794	477.70	199	11.128	490.75	222	11.462	
439.57	002	10.132	451.94	134	10.466	468.90	167	10.800	478.55	200	11.135	491.01	223	11.469	
439.30	003	10.138	452.10	135	10.473	469.15	168	10.807	478.21	198	11.141	491.26	224	11.475	
439.55	004	10.145	452.35	136	10.479	469.41	169	10.813	478.76	197	11.144	491.52	225	11.481	
439.81	005	10.152	452.61	137	10.486	469.65	170	10.820	478.72	190	11.154	491.78	226	11.488	
440.06	006	10.159	452.86	138	10.492	469.92	171	10.827	478.98	191	11.161	492.03	227	11.495	
440.32	007	10.167	453.12	139	10.499	470.18	172	10.834	479.23	191	11.167	492.29	228	11.502	
440.58	008	10.174	453.38	140	10.505	470.43	173	10.840	479.59	191	11.174	492.54	229	11.508	
440.83	009	10.181	453.63	141	10.512	470.69	174	10.846	479.74	191	11.180	492.80	230	11.515	
441.09	008	10.187	453.89	142	10.519	470.94	175	10.852	479.90	191	11.187	493.06	231	11.521	
441.34	006	10.193	454.14	143	10.525	471.20	176	10.858	480.06	191	11.194	493.31	232	11.528	
441.59	006	10.200	454.40	144	10.532	471.45	177	10.865	480.21	191	11.200	493.57	233	11.534	
441.84	006	10.206	454.66	145	10.538	471.71	178	10.871	480.36	191	11.207	493.82	234	11.541	
442.09	005	10.213	454.91	146	10.545	471.97	179	10.877	481.02	191	11.213	494.08	235	11.547	
442.34	005	10.220	455.17	147	10.551	472.23	180	10.883	481.28	191	11.220	494.34	236	11.554	
442.59	005	10.227	455.42	148	10.558	472.49	181	10.889	481.54	191	11.226	494.60	237	11.561	
442.84	005	10.234	455.68	149	10.564	472.75	182	10.895	481.80	191	11.233	494.86	238	11.567	
443.09	005	10.241	455.94	150	10.571	473.01	183	10.901	482.06	191	11.239	495.12	239	11.574	
443.34	005	10.248	456.20	151	10.578	473.27	184	10.907	482.32	191	11.246	495.38	240	11.581	
443.59	005	10.255	456.45	152	10.584	473.53	185	10.913	482.58	191	11.253	495.64	241	11.588	
443.84	005	10.262	456.71	153	10.591	473.79	186	10.919	482.84	191	11.260	495.90	242	11.595	
444.09	005	10.269	456.96	154	10.598	474.05	187	10.925	483.10	191	11.267	496.16	243	11.602	
444.34	005	10.276	457.22	155	10.604	474.31	188	10.931	483.36	191	11.274	496.42	244	11.609	
444.59	005	10.283	457.47	156	10.611	474.57	189	10.937	483.62	191	11.281	496.68	245	11.616	
444.84	005	10.290	457.73	157	10.617	474.83	190	10.943	483.88	191	11.288	496.94	246	11.623	
445.09	005	10.297	457.99	158	10.624	475.09	191	10.949	484.14	191	11.295	497.20	247	11.630	
445.34	005	10.304	458.24	159	10.631	475.35	192	10.955	484.40	191	11.302	497.46	248	11.637	
445.59	005	10.311	458.50	160	10.638	475.61	193	10.961	484.66	191	11.309	497.72	249	11.644	
445.84	005	10.318	458.75	161	10.645	475.87	194	10.967	484.92	191	11.316	497.98	250	11.651	
446.09	005	10.325	459.01	162	10.652	476.13	195	10.973	485.18	191	11.323	498.24	251	11.658	
446.34	005	10.332	459.26	163	10.659	476.39	196	10.979	485.44	191	11.330	498.50	252	11.665	
446.59	005	10.339	459.52	164	10.666	476.65	197	10.985	485.70	191	11.337	498.76	253	11.672	
446.84	005	10.346	459.78	165	10.673	476.91	198	10.991	485.96	191	11.344	499.02	254	11.679	
447.09	005	10.353	460.03	166	10.680	477.17	199	11.000	486.22	191	11.351	499.28	255	11.686	
447.34	005	10.360	460.29	167	10.687	477.43	200	11.007	486.48	191	11.358	499.54	256	11.693	
447.59	005	10.367	460.54	168	10.694	477.69	201	11.014	486.74	191	11.365	499.80	257	11.700	
447.84	005	10.374	460.80	169	10.701	477.95	202	11.021	487.00	191	11.372	500.06	258	11.707	
448.09	005	10.381	461.06	170	10.708	478.21	203	11.028	487.26	191	11.379	500.32	259	11.714	
448.34	005	10.388	461.32	171	10.715	478.47	204	11.035	487.52	191	11.386	500.58	260	11.721	
448.59	005	10.395	461.57	172	10.722	478.73	205	11.042	487.78	191	11.393	500.84	261	11.728	
448.84	005	10.402	461.83	173	10.729	478.99	206	11.049	488.04	191	11.400	501.10	262	11.735	
449.09	005	10.409	462.08	174	10.736	479.25	207	11.056	488.30	191	11.407	501.36	263	11.742	
449.34	005	10.416	462.34	175	10.743	479.51	208	11.063	488.56	191	11.414	501.62	264	11.749	
449.59	005	10.423	462.59	176	10.750	479.77	209	11.070	488.82	191	11.421	501.88	265	11.756	
449.84	005	10.430	462.85	177	10.757	480.03	210	11.077	489.08	191	11.428	502.14	266	11.763	
450.09	005	10.437	463.10	178	10.764	480.29	211	11.084	489.34	191	11.435	502.40	267	11.770	
450.34	005	10.444	463.36	179	10.771	480.55	212	11.091	489.60	191	11.442	502.66	268	11.777	
450.59	005	10.451	463.62	180	10.778	480.81	213	11.098	489.86	191	11.449	502.92	269	11.784	
450.84	005	10.458	463.87	181	10.785	481.07	214	11.105	490.12	191	11.456	503.18	270	11.791	
451.09	005	10.465	464.13	182	10.792	481.33	215	11.112	490.38	191	11.463	503.44	271	11.798	
451.34	005	10.472	464.38	183	10.799	481.59	216	11.119	490.64	191	11.470	503.70	272	11.805	





L1 = 3122 138 2021/TOKO 85 ACS-4238 A  
 L2 = 3122 138 2022/TOKO 85 ACS-4260 SEJ

Fig. 6 MUSTI test and application circuit.

Germanium diodes AA119 are required in the test circuit only.

In a complete FM channel (inclusive FM front end) the silicon diodes BA281 are recommended.

S open = without muting  
 S closed = with muting } for measuring purpose only.



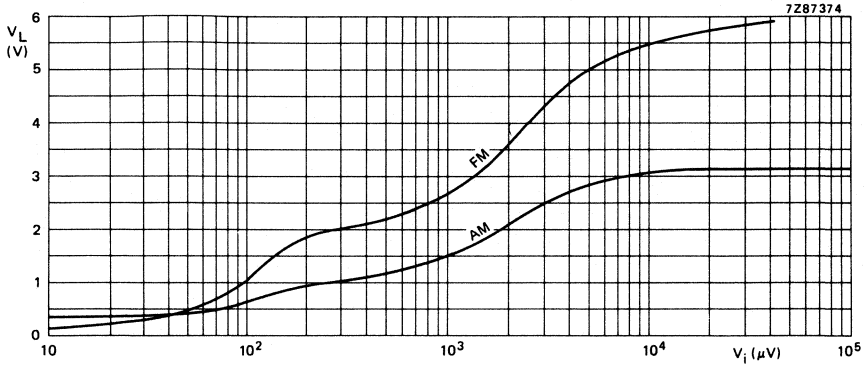


Fig. 9 Level detector output as a function of input voltage.

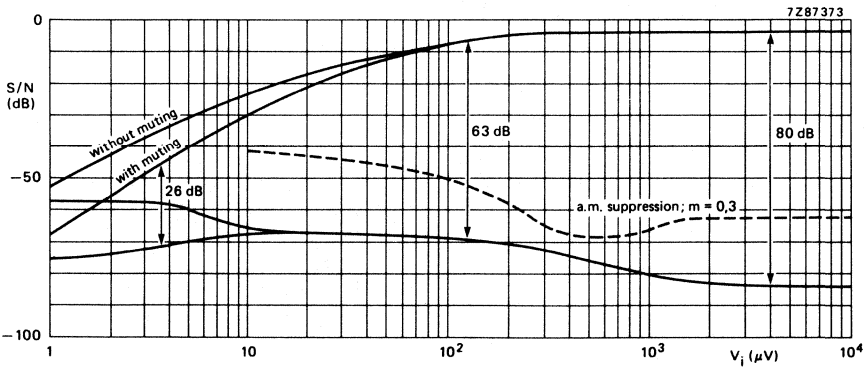



Fig. 10 Signal-to-noise ratio as a function of FM input voltage.  
 $f_i = 10,7$  MHz;  $\Delta f = 22,5$  kHz;  $f_{mod} = 1$  kHz; 0 dB = 245 mV.



Purchase of Philips' I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C-system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips.



# BIPOLAR ICs FOR RADIO AND AUDIO EQUIPMENT



FUNCTIONAL AND NUMERICAL INDEX  
MAINTENANCE TYPE LIST



GENERAL



PACKAGE OUTLINES



DEVICE DATA





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